EM78F724N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2017/06/30

1 General Description

EM78F724N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It has an on-chip 4K×13-bit Electrical Flash Memory and 128×8-bit in system programmable EEPROM.

2 Features

- CPU configuration
  - 4K×13 bits Flash memory
  - 272×8 bits on chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM
  - 8-level stacks for subroutine nesting
- I/O port configuration
  - 8 bidirectional I/O ports
  - 6 programmable pull-high I/O ports.
  - 8 programmable pull-low I/O ports.
- Operating voltage range:
  - 2.5V~3.6V at -40°C ~85°C (Industrial)
- Operating frequency range (base on two clocks):
  - IRC Drift Rate (Vdd @3.3V)

Internal RC Frequency	Drift Rate				
	Temperature (-40°C~+85°C)		Process	Total	
	Vdd	Internal Vref.		Vdd	Internal Vref.
500kHz	±2%	±1%	±1%	±3%	±2%
1 MHz	±2%	±1%	±1%	±3%	±2%
8 MHz	±2%	±1%	±1%	±3%	±2%

*Internal Vref.:UWTR total ±2%,NUWTR total ±2%

  - Sub IRC Drift Rate

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage 3.3V±5%	Process	Total
128kHz	±6.5%	±1%	±2%	±9.5 %
16kHz	±6.5%	±1%	±2%	±9.5 %

- Two 16-bit Timer/Counter
  - TM1: Timer/Counter/ Capture
  - TM2: Timer/Counter Peripheral configuration
- Peripheral configuration
  - Universal asynchronous receiver / transmitter (UART) available
  - Four operation modes: Normal, Green, Idle, Sleep
  - Power On Reset (POR): 2.2V/2.0V ±0.3V
  - 2 clocks per instruction cycle
  - High EFT immunity: 4KV/400V
  - There are two sub-frequency 128kHz and 16kHz,
    the 16kHz is provided by dividing 128kHz.
  - Single instruction cycle commands
  - Programmable free running watchdog timer
- Package Type
  - 10-pin MSOP 118mil: EM78F724NAMS10

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

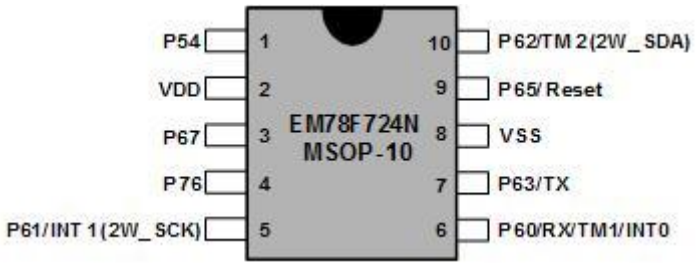


Figure 3-1 EM78F724NAMS10

4 Pin Description

Table 1 EM78F724N Pin Description

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *Analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal / resonator*

Name	Function	Input Type	Output Type	Description
–	VDD	Power	–	Power
–	VSS	Power	–	Ground
P54	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pull-high.
P60/RX/TM1/INT0	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	RX	ST	-	RX of UART
	TM1	ST	–	16 bits Timer/Counter 1
	INT0	ST	–	External Interrupt 0
P61/INT1(2W_SCK)	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wake-up
	INT1	ST	–	External Interrupt 1
	2W_SCL	ST	CMOS	On Chip Debug System clock pin
P62/TM2(2W_SDA)	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wake-up
	TM2	ST	–	16 bits Timer/Counter 2
	2W_SDA	ST	CMOS	On Chip Debug System data pin
P63/TX	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wakeup
	TX	-	CMOS	TX of UART
P65/RESET	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wake-up
	RESET	ST	-	
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wake-up
P76	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-down, and pull-high

5 Block Diagram

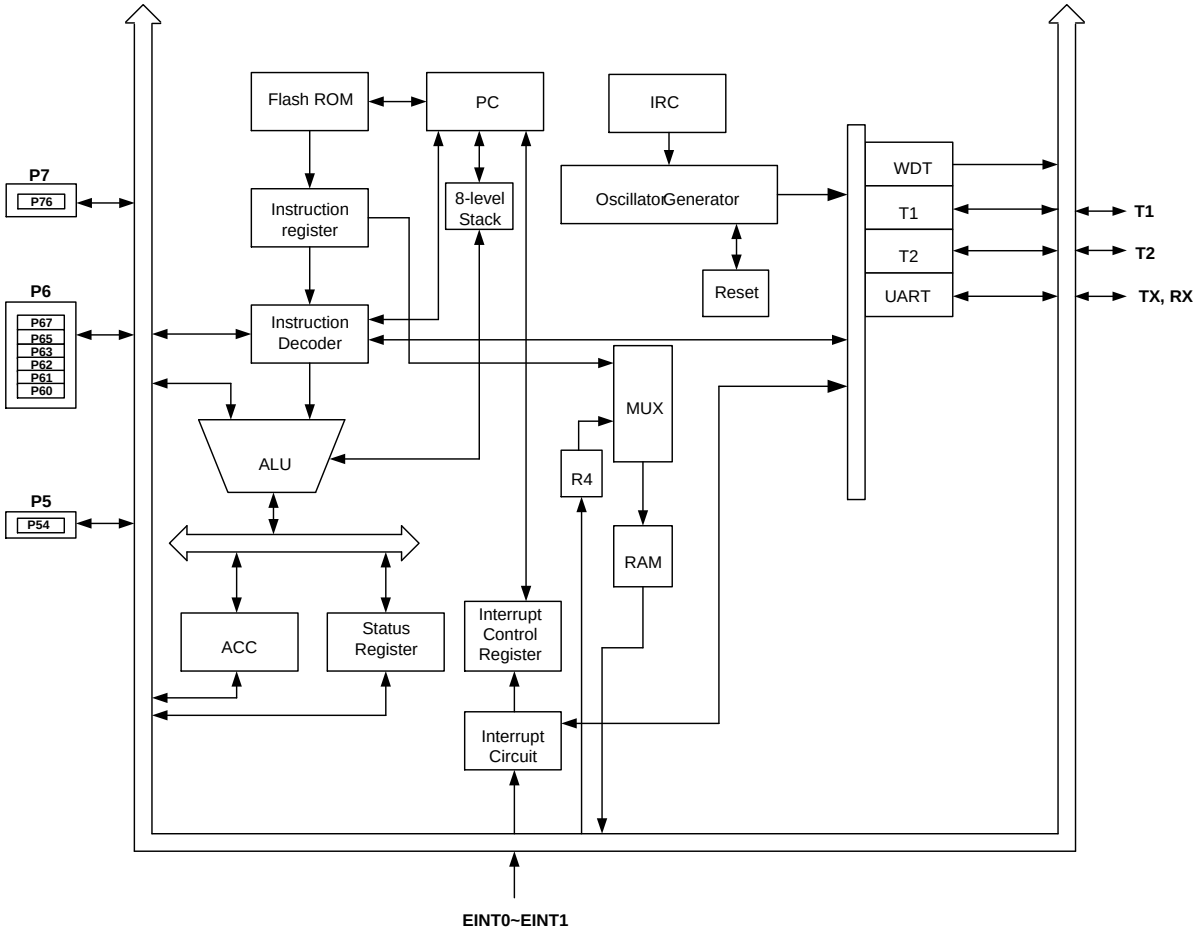


Figure 5-1 EM78F724N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	SBS2	SBS1	SBS0	-	GBS2	GBS1(IGBS1)	GBS0(IGBS0)
0	R/W	R/W	R/W	0	R/W	R/W	R/W

Bit 7: not used bits, fixed to “0” all the time.

Bits 6~4 (SBS2~SBS0): special register bank select bit. It is used to select Banks 0~7 of Special Registers **R5~RF**.

SBS2	SBS1	SBS0	Special Register Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bit 3: not used bit, fixed to “0” all the time.

Bits 2~0 (GBS2~GBS0): General register bank select bit. It is used to select Banks 0~7 of general register R20~R3F.

GBS2	GBS1(IGBS1)	GBS0(IGBS0)	RAM Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

6.1.3 R2 (Program Counter and Stack)

Depending on the device type, R2 and hardware stack are 12-bit wide. The structure is depicted in Figure 6-1. The configuration structure generates 4K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all “0”s when under a reset condition.

“JMP” instruction allows direct loading of the lower 10 program counter bits. Thus, “JMP” allows PC to go to any location within a page (1K).

“CALL” instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

“LJMP” instruction allows direct loading of the program counter bits (A0~A11). Thus, “LJMP” allows the PC to go to any location within 4K (2^{12}).

“LCALL” instruction loads the program counter bits (A0~A11), and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).

“RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents of the top-level stack.

“ADD R2, A” allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

“MOV R2, A” allows loading an address from the “A” register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except “ADD R2,A” that is written to R2 (e.g. “MOV R2, A”, “BC R2, 6”) will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2) except for the instructions that would change the contents of R2 and “LCALL”, “LJMP”, “TBRD” instruction. The “LCALL”, “LJMP” and “TBRD” instructions need two instruction cycles.

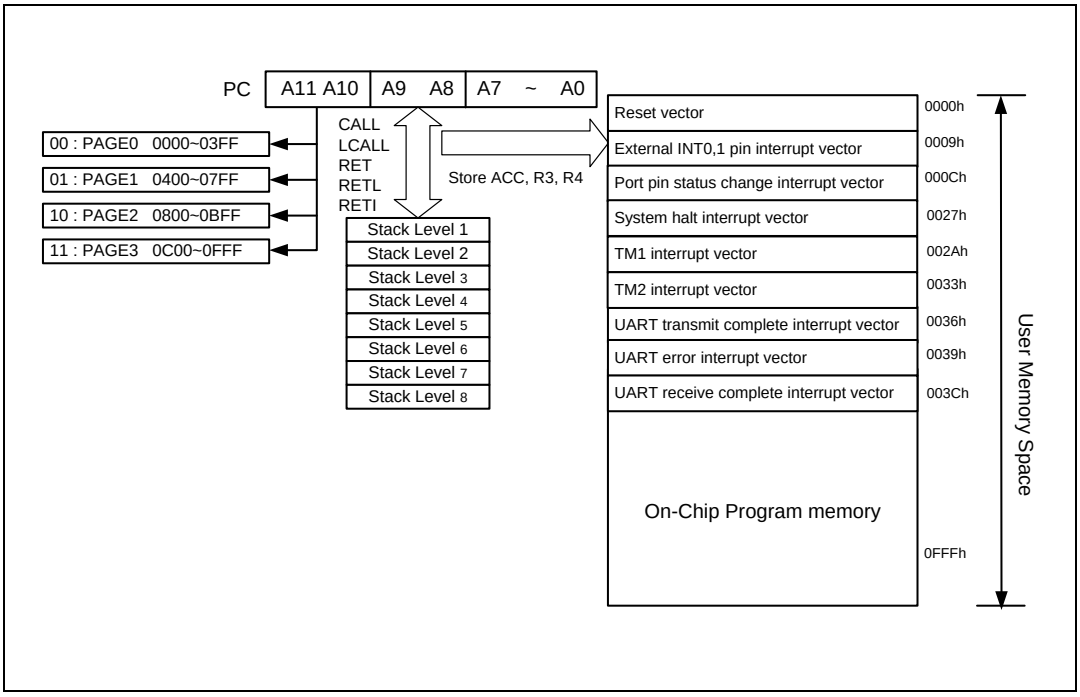


Figure 6-1 Program Counter Organization

Address	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
0X00	IAR (Indirect Addressing Reg.)							
0X01	BSR (Bank Selection Control Register)							
0X02	PCL (Program Counter Low)							
0X03	SR (Status Reg.)							
0X04	RSR (RAM Selection Register)							
0X05	Port 5	TM1CR1	URCR1	TM2CR1	P6PHCR	Reserve	Reserve	Reserve
0X06	Port 6	TM1CR2	URS	TM2CR2	P6PLCR	Reserve	Reserve	Reserve
0X07	Port 7	TM1DBH	URTD	TM2DBH	P57PHCR	Reserve	Reserve	Reserve
0X08	IOCR5	TM1DBL	URRDL	TM2DBL	P57PLCR	Reserve	Reserve	Reserve
0X09	IOCR6	TM1DAH	Reserve	TM2DAH	P6HDSCR	Reserve	Reserve	Reserve
0X0A	IOCR7	TM1DAL	URCR2	TM2DAL	Reserve	Reserve	Reserve	Reserve
0x0B	WKCR	EIESCR	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve
0X0C	OMCR	STKMON	Reserve	EECR1	MFCR	Reserve	Reserve	TBWCR
0X0D	WDTCR	Reserve	Reserve	EECR2	SFCR	Reserve	Reserve	FLKR
0X0E	SFR1	IMR1	Reserve	EEAR	Reserve	Reserve	Reserve	TBTPL
0X0F	SFR2	IMR2	Reserve	EEDA	Reserve	Reserve	Reserve	TBTPH
0X10 ~ 0X1F	16 Bytes common Register							
0X20	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6 IAP BUF	Bank 7 IAP BUF
0X21								
.								
.								
.								
0X3E								
0X3F								

Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	INT	T	P	Z	DC	C

Bits 7~6: Not used, set to "0" all the time

Bit 5 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

C is set when a carry occurs and cleared when a borrow occurs during an arithmetic operation. The Carry Flag bit is set or cleared, depending on the operation that is performed

For ADD, INC, INCA instruction

0: No carry occurs.

1: Carry occurs.

For SUB, DEC, DECA instruction

0: Borrow occurs.

1: No borrow occurs.

For RLC, RRC, RLCA, RRCA instruction

The Carry flag is used as a link between the least significant bit (LSB) and most significant bit (MSB).

6.1.5 R4 (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IGBS1 (GBS1)	IGBS0 (BGS0)	RS5	RS4	RS3	RS2	RS1	RS0

Bits 7~6 (IGBS1~IGBS0): general register bank select bit. It is used to select Banks 0~7 of general register R20~R3F.

GBS2	IGBS1 (GBS1)	IGBS0 (GBS0)	RAM Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bits 5~0 (RS5~RS0): are used to select registers (Address: 00~3F) in the indirect address mode.

See the data memory configuration in Fig 4.

6.1.6 Bank 0 R5 ~ R7 (Port 5 ~ Port 7)

R5 ~ R7 are I/O registers.

6.1.7 Bank 0 R8: IOCR5 (I/O Port 5 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.8 Bank 0 R9: IOCR6 (I/O Port 6 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.9 Bank 0 RA: IOCR7 (I/O Port 7 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

6.1.10 Bank 0 RB: WUCR (Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URWE	-	-	-	-	EX2WE	EX1WE	ICWE

Bit 7(URWE): UART wake up enable bit.

0: Disable UART wake up.

1: Enable UART wake up.

Bits 6~3: Not used, set to "0" all the time

Bit 2 (EX2WE): External wake up enable bit.

0: Disable External /INT2 pin wake up

1: Enable External /INT2 pin wake up

Bit 1 (EX1WE): External wake up enable bit.

0: Disable External /INT1 pin wake up

1: Enable External /INT1 pin wake up

Bit 0 (ICWE): Port input status change wake up enable bit

0: Disable Port input status change wake up.

1: Enable Port input status change wake up.

6.1.11 Bank 0 RC: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	PERCS	CLK1	CLK0	SFS	RCM1	RCM0

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator (default)

When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will decide SLEP instruction which mode to go.

0: “IDLE=0”+SLEP instruction → sleep mode

1: “IDLE=1”+SLEP instruction → idle mode (default)

Bit 5 (PERCS): Periphery Clock Source for Green and Idle mode.

0: Periphery Clock Source is Fs. Fm will be Stop into Green and Idle mode (default)

1: Periphery Clock Source is Fm. Fm will be oscillation into Green and Idle mode.

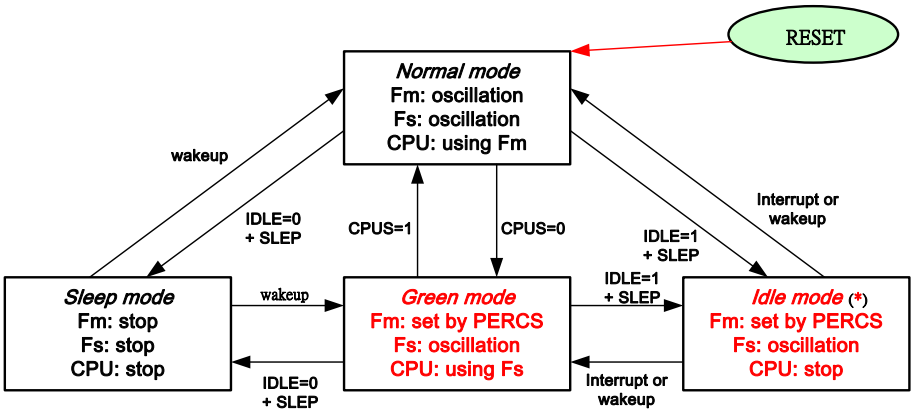


Figure 6-3 CPU operation mode

Note

(*) Switching Operation Mode from Idle → Normal, Idle → Green

If the clock source of the timer is Fs or Fm, the timer/counter will continue to count in Idle mode. When the matching condition of the timer/counter occurs during Idle mode, the interrupt flag of the timer/counter will be active. The MCU will jump to the interrupt vector when the corresponding interrupt is enabled.

Clock Number for Mode Change

Normal

Fmain	Fsub	Power-on	Pin-Reset / WDT	
			N	G / I /S
IRC 500K, 1M,8M	IRC	16ms + WSTO + *SST*+ (1~8)*1/Fmain	*SST* + (1~8)*1/Fmain	WSTO + *SST*+ (1~8)*1/Fmain

PERCS=0

Fmain	Fsub	G → N	I → N	S → N
IRC 500K, 1M,8M	IRC	WSTO + *SST*+ (1~8)*1/Fmain	WSTO + *SST*+ (1~8)*1/Fmain	WSTO + *SST*+ (1~8)*1/Fmain

PERCS=0

Fmain	Fsub	I → G	S → G
IRC	IRC	*SST*+1*1/Fsub	WSTO + *SST*+1*1/Fsub (WDT disable) *SST*+1*1/Fsub (WDT enable)

PERCS=1

Fmain	Fsub	G → N	I → N	S → N
IRC 500K, 1M,8M	IRC	*SST*+ (1~8)*1/Fmain	*SST*+ (1~8)*1/Fmain	WSTO + *SST*+ (1~8)*1/Fmain

PERCS=1

Fmain	Fsub	I → G	S → G
IRC	IRC	*SST*+1*1/Fsub	WSTO + *SST*+1*1/Fsub (WDT disable) *SST*+1*1/Fsub (WDT enable)

N: Normal mode WSTO: Waiting Time from Start-to-Oscillation

G: Green modeI: Idle mode S: Sleep mode

*SST: S*ynchronous *Stable Time:*

Bit 5: Not used, set to "0" all the time

Bit 4~3 (CLK1~CLK0): Instruction period option bits

*Default value corresponding Code Option Word 1 **CLK1~CLK0**

*CLK1	*CLK0	Scale of Main Clock
0	0	/2 (Default)
0	1	/4
1	0	/8
1	1	/16

Bit 2 (SFS): Sub-frequency select (Default by Code Option)

We must take Bank 0 RD OMCR Bit2 into consideration.

Bits 1~0 (RCM1~RCM0): Internal RC mode selection bits

*RCM1	*RCM0	Frequency
0	0	Reserved
0	1	500kHz(Default)
1	0	1 MHz
1	1	8MHz

6.1.12 Bank 0 RD: WDTCR (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS1	EIS0	SFSS	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

Bit 6 (EIS1): Control bit used to define the function of P61 (/INT1) pin

0: P61, bidirectional I/O pin

1: /INT1, external interrupt pin.

Bit 5 (EIS0): Control bit used to define the function of P60 (/INT0) pin

0: P60, bidirectional I/O pin

1: /INT0, external interrupt pin.

Bit 4: (SFSS)**:** Sub-frequency Sub select.

We must take Bank 0 RC OMCR Bit2 into consideration.

SFS	SFSS	Frequency
0	**0**	16kHz
0	**1**	No Use
1	**0**	128kHz
1	**1**	Reserved

Bit 3 (PSWE): Pre-scaler enable bit for WDT

0: Pre-scaler disable bit, WDT rate is 1:1

1: Pre-scaler enable bit, WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT pre-scaler bits

PST2	PST1	PST0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.13 Bank 0 RE: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHSF	-	-	TM2SF	TM1SF	EXSF1	EXSF0	ICSF

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bit 7 (SHSF): SHSF Interrupt status Flag. Reset by software.

Bits 6~5: Not used, set to “0” at all time

Bit 4 (TM2SF): 16-bit Timer/Counter 2 status flag. Clear by software.

Bit 3 (TM1SF): 16bit Timer/Counter 1 Status flag. Clear by software.

Bit 2 (EXSF1) : External Interrupt 1 Status flag

Bit 1 (EXSF0) : External Interrupt 0 Status flag

Bit 0 (ICSF): Port interrupt flag.

6.1.14 Bank 0 RF: SFR2 (Status Flag Register2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UERRSF	URSF	UTSF	-	-	-	-	-

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bit 7 (UERRSF): UART Receiving Error status Flag. Flag is cleared by software or UART disabled.

Bit 6 (URSF): UART Receive Mode Data Buffer Full status Flag. Flag is cleared by software.

Bit 5 (UTSF): UART Transmit Mode Data Buffer Empty status Flag. Flag is cleared by software.

Bits 4~0: Not used, set to “0” at all time

6.1.15 Bank1 R5: TM1CR1 (Timer 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1S	TM1RC	TM1SS1	-	-	TM1MOS	-	-

Bit 7 (TM1S): Timer/counter 1 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM1RC): Timer 1 Read Control Bit

0: When this bit is set to 0, can’t read data from TM1DB (default).

1: When this bit is set to 1, data read from TM1DB is a number of counting.

Bit 5 (TM1SS1): Timer/counter 1 Clock Source Select Bit 1

0: Internal clock as count source (Fc)- Fs/Fm (default)

1: External TM1 pin as count source (Fc). It is used only for timer/counter mode.

Bits 4 ~ 3: Fixed to “0” all the time.(only Read)

Bit 2 (TM1MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0: Fixed to “0” all the time (Read only)

6.1.16 Bank1 R6: TM1CR2 (Timer 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TM1M1	TM1M0	TM1SS0	TM1CK3	TM1CK2	TM1CK1	TM1CK0

Bit 7: Fixed to “0” all the time.(only Read)

Bits 6~5 (TM1M1~TM1M0): Timer 1 operation mode select.

TM1M1	TM1M0	Operating Mode Select
0	0	Timer/Counter Rising Edge
0	1	Timer/Counter Falling Edge
1	0	Capture Mode Rising Edge
1	1	Capture Mode Falling Edge

Bit 4 (TM1SS0): Timer 1 clock source selection bit

0 : The Fs is used as count source (Fc) (default)

1 : The Fm is used as count source (Fc)

Bits 3~0 (TM1CK3~TM1CK0): Timer 1 clock source pre-scaler select.

TM1CK3	TM1CK2	TM1CK1	TM1CK0	Clock Source	Resolution 1 MHz	Max. Time 1 MHz	Resolution 16kHz	Max Time 16kHz
				Normal	F_C=1M	F_C=1M	F_C=16K	F_C=16K
0	0	0	0	F_C	1μs	65.536ms	62.5μs	4.096s
0	0	0	1	$F_C/2$	2μs	131.072ms	125μs	8.192s
0	0	1	0	$F_C/2^2$	4μs	262.144ms	250μs	16.384s
0	0	1	1	$F_C/2^3$	8μs	524.288ms	500μs	32.768s
0	1	0	0	$F_C/2^4$	16μs	1.048576s	1ms	65.536s
0	1	0	1	$F_C/2^5$	32μs	2.097152s	2ms	131.072s
0	1	1	0	$F_C/2^6$	64μs	4.194304s	4ms	262.144s
0	1	1	1	$F_C/2^7$	128μs	8.388608s	8ms	524.288s
1	0	0	0	$F_C/2^8$	256μs	16.777216s	16ms	1048.58s
1	0	0	1	$F_C/2^9$	512μs	33.554432s	32ms	2097.15s
1	0	1	0	$F_C/2^{10}$	1024μs	67.108864s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	2048μs	134.217728s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	4096μs	268.435456s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	8.192ms	536.870912s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	16.384ms	1073.741824s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	32.768ms	2147.483648s	2.048s	134217s

6.1.17 Bank 1 R7: TM1DBH (High byte of Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DB15	TM1DB14	TM1DB13	TM1DB12	TM1DB11	TM1DB10	TM1DB9	TM1DB8

Bits 7~0 (TM1DB7~TM1DB0): Data Buffer B of 16 bit Timer 1

6.1.18 Bank 1 R8: TM1DBL (Low byte of Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DB7	TM1DB6	TM1DB5	TM1DB4	TM1DB3	TM1DB2	TM1DB1	TM1DB0

Bits 7~0 (TM1DB7~TM1DB0): Data buffer B of 16 bit Timer 1

6.1.19 Bank 1 R9: TM1DAH (High bytes of Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DA15	TM1DA14	TM1DA13	TM1DA12	TM1DA11	TM1DA10	TM1DA9	TM1DA8

Bits 7~0 (TM1DA15~TM1DA8): Data Buffer A of 16 bit Timer 1

6.1.20 Bank 1 RA: TM1DAL (Low bytes of Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DA7	TM1DA6	TM1DA5	TM1DA4	TM1DA3	TM1DA2	TM1DA1	TM1DA0

Bits 7~0 (TM1DA7~TM1DA0): Data buffer A of 16 bit Timer 1

6.1.21 Bank 1 RB: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIES1	EI1NRE	EI1NR1	EI1NR0	EIES0	EI0NRE	EI0NR1	EI0NR0

Bit 7 (EIES1): external interrupt edge select bit

0: falling edge interrupt

1: rising edge interrupt

Bit 6 (EI1NRE): Noise rejection enable of External Interrupt 1

0: Noise rejection Disable

1: Noise rejection Enable

Bits 5~4 (EI1NR1~ EI1NR0): Delay time selection for noise rejection of External Interrupt 1

EI1NR1	EI1NR0	Function Description
0	0	Noise Rejection Disable
0	1	3 x (1/ F_m or 1/ Fs by SFS bit)
1	0	7 x (1/ F_m or 1/ Fs by SFS bit)
1	1	15 x (1/ F_m or 1/ Fs by SFS bit)

Bit 3 (EIES0): external interrupt edge select bit

0: falling edge interrupt

1: rising edge interrupt

Bit 2 (EI0NRE): Noise rejection enable of External Interrupt 0

0: Noise rejection Disable

1: Noise rejection Enable

Bit 1~0 (EI0NR1~ EI0NR0): Delay time selection for noise rejection of External Interrupt 0

EI1NR1	EI1NR0	Function Description
0	0	Noise rejection Disable
0	1	3 x (1/ F_m or 1/ Fs by SFS bit)
1	0	7 x (1/ F_m or 1/ Fs by SFS bit)
1	1	15 x (1/ F_m or 1/ Fs by SFS bit)

6.1.22 Bank1 RC: STKMON (Stack point)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV					STL2	STL1	STL0

Bit 7(STOV): Stack pointer overflow indication bit. Only read.

Bits 2~0(STL2~0): Stack pointer number. Only read.

6.1.23 Bank 1 RD (Reserved)

6.1.24 Bank 1 RE: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE	-	-	TM2IE	TM1IE	EXIE1	EXIE0	ICIE

Bit 7 (SHIE): SHSF interrupt enable bit.

0: Disable SHSF interrupt

1: Enable SHSF interrupt

Bits 6~5: Not used, set to “0” at all time

Bit 4 (TM2IE): TM2SF interrupt enable bit.

0: Disable TM2SF interrupt

1: Enable TM2SF interrupt

Bit 3 (TM1IE): TM1SF interrupt enable bit.

0: Disable TM1SF interrupt

1: Enable TM1SF interrupt

Bit 2 (EXIE1): EXSF1 interrupt enable and **/**INT1 function enable bit.

0: P61/INT1 is P61 pin, EX1SF always equals 0.

1: Enable EXSF1 interrupt and P61/INT1 is /INT1 pin

Bit 1 (EXIE0): EXSF0 interrupt enable and **/**INT0 function enable bit.

0: P60/RX/TM1/INT0 is P60 pin, EX1SF always equals 0.

1: Enable EXSF0 interrupt and P60/RX/TM1/INT0 is /INT0 pin

Bit 0 (ICIE): ICIF interrupt enable bit.

0: Disable ICIF interrupt

1: Enable ICIF interrupt.

6.1.25 Bank 1 RF: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UERRIE	URIE	UTIE	-	-	-	-	-

Bit 7 (UERRIE): URERRSF interrupt enable bit.

0: Disable UERRSF interrupt

1: Enable UERRSF interrupt.

Bit 6 (URIE): URSF interrupt enable bit.

0: Disable URSF interrupt

1: Enable URSF interrupt.

Bit 5 (UTIE): UTSF interrupt enable bit.

0: Disable UTSF interrupt

1: Enable UTSF interrupt.

Bits 4~0: Not used, set to “0” at all time

6.1.26 Bank 2 R5: URCR1 (UART Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UINVEN	-	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (UINVEN): Enable UART TXD and RXD Port Inverse Output Bit

0: Disable TXD and RXD port inverse output.

1: Enable TXD and RXD port inverse output.

Bit 6: Not used, set to "0" at all time

Bit 5 (UMODE0): UART mode select bits

UMODE0	UART Mode
0	Mode 1: 7-bit
1	Mode 1: 8-bit

Bits 4 ~ 2 (BRAT2~BRAT0): transmit Baud rate selection

BRATE2	BRATE1	BRATE0	Baud rate	500kHz	Baud Rate	1 MHz
0	0	0	Fc/1	19200	FIRC/1	38400
0	0	1	Fc/2	9600	FIRC/2	19200
0	1	0	Fc/4	4800	FIRC/4	9600
0	1	1	Fc/8	2400	FIRC/8	4800
1	0(x)	0	Fc/16	1200	FIRC/16	2400
1	0(x)	1	Fc/32	600	FIRC/32	1200
1	1	0	Reserved	Reserved	Reserved	
1	1	1	Reserved	Reserved	Reserved	

1bit UART = 26* Baud Rate

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when write into URTD register. UTBF bit will be clear by hardware when enabling transmission. And UTBF bit is read-only. Therefore, write URTD register is necessary when want to start transmitting shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.27 Bank 2 R6: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7: Not used, set to "0" at all time

Bit 6 (EVEN): select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error happened, and clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error happened, and clear to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error happen, and clear to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URRD register. URBF will be clear by hardware when enabling receiving. And URBF bit is read-only. Therefore, read URRD register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.28 Bank 2 R7: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7 ~ 0 (URTD7~URTD0): UART transmit data buffer. Write only.

6.1.29 Bank 2 R8: URRD (UART Receive Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7~0 (URRDL7~URRDL0): UART Receive Data Buffer. Read only.

6.1.30 Bank 2 RA: URCR2 (UART Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	URSS

Bit 7 ~ 1: Not used, set to "0" all the time.

Bit 0 (URSS): UART clock source selection bit

0 : The Fs is used as count source (Fc)

1 : The Fm is used as count source (Fc) (default)

6.1.31 Bank 3 R5: TM2CR1 (Timer 2 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2S	TM2RC	TM2SS1	-	-	TM2MOS	-	-

Bit 7 (TM2S): Timer 2 Start Control Bit

0: Stop and clear counter (default)

1: Start

Bit 6 (TM2RC): Timer 2 Read Control Bit

0: When this bit is set to 0, can't read data from TM2D (default).

1: When this bit is set to 1, data read from TM2D is a number of counting.

Bit 5 (TM2SS1): Timer 2 Clock Source Select Bit 1

0: Internal clock as count source (Fc)- Fs/Fm (default)

1: External TM2 pin as count source (Fc). It is used only for timer/counter mode.

Bits 4 ~ 3: Fixed to "0" all the time.(only Read)

Bit 2 (TM2MOS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One–shot mode

Bits 1~0: Fixed to "0" all the time (Read only)

6.1.32 Bank 3 R6: TM2CR2 (Timer 2 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TM2M0	TM2SS0	TM2CK3	TM2CK2	TM2CK1	TM2CK0

Bits 7~5 (TM2M2~TM2M0): Timer 2 operation mode select.

TM2M0	Operating Mode Select
0	Timer/Counter Rising Edge
1	Timer/Counter Falling Edge

Bit 4 (TM2SS0): Timer 2 clock source selection bit

0 : The Fs is used as count source (Fc) (default)

1 : The Fm is used as count source (Fc)

Bits 3~0 (TM2CK3~TM2CK0): Timer 2 clock source pre-scaler select.

TM2CK3	TM2CK2	TM2CK1	TM2CK0	Clock Source	Resolution 1 MHz	Max time 1 MHz	Resolution 16kHz	Max Time 16kHz
				Normal	F_C=1M	F_C=1M	F_C=16K	F_C=16K
0	0	0	0	F_C	1μs	65.536ms	62.5μs	4.096s
0	0	0	1	$F_C/2$	2μs	131.072ms	125μs	8.192s
0	0	1	0	$F_C/2^2$	4μs	262.144ms	250μs	16.384s
0	0	1	1	$F_C/2^3$	8μs	524.288ms	500μs	32.768s
0	1	0	0	$F_C/2^4$	16μs	1.048576s	1ms	65.536s
0	1	0	1	$F_C/2^5$	32μs	2.097152s	2ms	131.072s
0	1	1	0	$F_C/2^6$	64μs	4.194304s	4ms	262.144s
0	1	1	1	$F_C/2^7$	128μs	8.388608s	8ms	524.288s
1	0	0	0	$F_C/2^8$	256μs	16.777216s	16ms	1048.58s
1	0	0	1	$F_C/2^9$	512μs	33.554432s	32ms	2097.15s
1	0	1	0	$F_C/2^{10}$	1024μs	67.108864s	64ms	4194.3s
1	0	1	1	$F_C/2^{11}$	2048μs	134.217728s	128ms	8388.6s
1	1	0	0	$F_C/2^{12}$	4096μs	268.435456s	256ms	16777s
1	1	0	1	$F_C/2^{13}$	8.192ms	536.870912s	512ms	33554s
1	1	1	0	$F_C/2^{14}$	16.384ms	1073.741824s	1.024s	67108s
1	1	1	1	$F_C/2^{15}$	32.768ms	2147.483648s	2.048s	134217s

6.1.33 Bank 3 R7: TM2DBH (High Byte of Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DB15	TM2DB14	TM2DB13	TM2DB12	TM2DB11	TM2DB10	TM2DB9	TM2DB8

Bits 7~0 (TM2DB15~TM2DB8): Data Buffer B of 16 bit Timer 2

6.1.34 Bank 3 R8: TM2DBL (Low Byte of Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DB7	TM2DB6	TM2DB5	TM2DB4	TM2DB3	TM2DB2	TM2DB1	TM2DB0

Bits 7~0 (TM2DB7~TM2DB0): Data Buffer B of 16 bit Timer 2

6.1.35 Bank 3 R9: TM2DAH (High Byte of Timer 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DA15	TM2DA14	TM2DA13	TM2DA12	TM2DA11	TM2DA10	TM2DA9	TM2DA8

Bits 7~0 (TM2DA15~TM2DA8): Data Buffer A of 16 bit Timer 2

6.1.36 Bank 3 RA: TM2DAL (Low Byte of Timer 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2DA7	TM2DA6	TM2DA5	TM2DA4	TM2DA3	TM2DA2	TM2DA1	TM2DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TM2DA7~TM2DA0): Data Buffer A of 16 bit Timer 2

6.1.37 Bank 3 RB (Reserved)

6.1.38 Bank 3 RC: EECR1 (EEPROM Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	RD	WR

Bits 7~2: unused bit, set to 0 all the time

Bit 1 (RD): Read control bit

0: don't execute EEPROM read

1: read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware.)

Bit 0 (WR): Write control bit

0: write cycle to the EEPROM is completed.

1: initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware.)

6.1.39 Bank 3 RD: EECR2 (EEPROM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEWE	EEDF	EEPC	-	-	-	-	-

Bit 7 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: Allow EEPROM write cycles

Bit 6 (EEDF): EEPROM detect flag

0: Write cycle is completed

1: Write cycle is unfinished

Bit 5(EEPC): EEPROM power down control bit

0: switch of EEPROM

1: EEPROM is operating

Bits 4~0: unused bit, set to 0 all the time

6.1.40 Bank 3 RE: EERA (EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bits 7~0 (EERA6~EERA0): EEPROM address register

6.1.41 Bank 3 RF: EERD (EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7~0(EERD7~EERD0): EEPROM data register.

6.1.42 Bank 4 R5: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	-	PH65	-	PH63	PH62	PH61	PH60

Bit 7 (PH67): Control bit used to enable the pull high of P67 pin (Reset Pin)

0: Enable internal pull-high

1: Disable internal pull-high (default)

Bit 6: Not used, set to "0" all the time.

Bit 5 (PH65): Control bit used to enable the pull high of P65 pin

Bit 4: Not used, set to "0" all the time.

Bit 3 (PH63): Control bit used to enable the pull high of P63 pin

Bit 2 (PH62): Control bit used to enable the pull high of P62 pin

Bit 1 (PH61): Control bit used to enable the pull high of P61 pin

Bit 0 (PH60): Control bit used to enable the pull high of P60 pin

6.1.43 Bank 4 R6: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PL65	-	PL63	PL62	PL61	PL60

Bit 7 (PL67): Control bit used to enable pull low of the P67 pin

0: Enable internal pull-low

1: Disable internal pull-low (default)

Bit 6: Not used, set to "0" all the time.

Bit 5 (PL65): Control bit used to enable pull low of the P65 pin

Bit 4: Not used, set to "0" all the time.

Bit 3 (PL63): Control bit used to enable pull low of the P63 pin

Bit 2 (PL62): Control bit used to enable pull low of the P62 pin

Bit 1 (PL61): Control bit used to enable pull low of the P61 pin

Bit 0 (PL60): Control bit used to enable pull low of the P60 pin

6.1.44 Bank 4 R7: P57PHCR (Port 5, Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P7HPH	-	P5HPH	-

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P7HPH): Control bit used to enable the pull high of Port7 high nibble pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

Bit 2: Not used, set to "0" all the time.

Bit 1 (P5HPH): Control bit used to enable the pull high of Port5 high nibble pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

Bit 0: Not used, set to "0" all the time.

6.1.45 Bank 4 R8: P57PLCR (Port 5, Port 7 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P7HPL	-	P5HPL	-

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P7HPL): Control bit used to enable the pull low of Port7 high nibble pin

0: Enable internal pull-low

1: Disable internal pull-low (default)

Bit 2: Not used, set to "0" all the time.

Bit 1 (P5HPL): Control bit used to enable the pull low of Port5 high nibble pin

0: Enable internal pull-low

1: Disable internal pull-low (default)

Bit 0: Not used, set to "0" all the time.

6.1.46 Bank4 R9: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	H65	-	H63	H62	H61	H60

Bit 7~6: Not used, set to "0" all the time.

Bits 5 (H65): P65 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

Bit 4: Not used, set to "0" all the time.

Bits 3 (H63): P63 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

Bits 2 (H62): P62 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

Bit 1: Not used, set to "0" all the time.

Bit 0 (H60): P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink (default)

6.1.47 Bank 4 RA~RB (Reserved)

6.1.48 Bank 4 RC MFCR (Trim bits of Main-Frequency IRC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CA5	CA4	CA3	CA2	CA1	CA0
0	0	R/W	R/W	R/W	R/W	R/W	R/W

Bits 4~0 (CA5~CA0): Trim bits of Main frequency IRC

Trimming code						Clock Period	Frequency
CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]		
0	0	0	0	0	0	Period*(1+32%)	F*(1-24.24%)
0	0	0	0	0	1	Period*(1+31%)	F*(1-23.66%)
0	0	0	0	1	0	Period*(1+30%)	F*(1-23.08%)
0	0	0	0	1	1	Period*(1+29%)	F*(1-22.48%)
0	0	0	1	0	0	Period*(1+28%)	F*(1-21.88%)
0	0	0	1	0	1	Period*(1+27%)	F*(1-21.26%)
0	0	0	1	1	0	Period*(1+26%)	F*(1-20.63%)

Trimming code						Clock Period	Frequency
CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]		
0	0	0	1	1	1	Period*(1+25%)	F*(1-20%)
0	0	1	0	0	0	Period*(1+24%)	F*(1-19.36%)
0	0	1	0	0	1	Period*(1+23%)	F*(1-18.70%)
0	0	1	0	1	0	Period*(1+22%)	F*(1-18.03%)
0	0	1	0	1	1	Period*(1+21%)	F*(1-17.36%)
0	0	1	1	0	0	Period*(1+20%)	F*(1-16.67%)
0	0	1	1	0	1	Period*(1+19%)	F*(1-15.97%)
0	0	1	1	1	0	Period*(1+18%)	F*(1-15.26%)
0	0	1	1	1	1	Period*(1+17%)	F*(1-14.53%)
0	1	0	0	0	0	Period*(1+16%)	F*(1-13.79%)
0	1	0	0	0	1	Period*(1+15%)	F*(1-13.04%)
0	1	0	0	1	0	Period*(1+14%)	F*(1-12.28%)
0	1	0	0	1	1	Period*(1+13%)	F*(1-11.50%)
0	1	0	1	0	0	Period*(1+12%)	F*(1-10.72%)
0	1	0	1	0	1	Period*(1+11%)	F*(1-9.91%)
0	1	0	1	1	0	Period*(1+10%)	F*(1-9.09%)
0	1	0	1	1	1	Period*(1+9%)	F*(1-8.26%)
0	1	1	0	0	0	Period*(1+8%)	F*(1-7.41%)
0	1	1	0	0	1	Period*(1+7%)	F*(1-6.54%)
0	1	1	0	1	0	Period*(1+6%)	F*(1-5.66%)
0	1	1	0	1	1	Period*(1+5%)	F*(1-4.76%)
0	1	1	1	0	0	Period*(1+4%)	F*(1-3.85%)
0	1	1	1	0	1	Period*(1+3%)	F*(1-2.91%)
0	1	1	1	1	0	Period*(1+2%)	F*(1-1.96%)
0	1	1	1	1	1	Period*(1+1%)	F*(1-0.99%)
1	1	1	1	1	1	Period (default)	F (default)
1	1	1	1	1	0	Period*(1-1%)	F*(1+1.01%)
1	1	1	1	0	1	Period*(1-2%)	F*(1+2.04%)
1	1	1	1	0	0	Period*(1-3%)	F*(1+3.09%)
1	1	1	0	1	1	Period*(1-4%)	F*(1+4.17%)
1	1	1	0	1	0	Period*(1-5%)	F*(1+5.26%)
1	1	1	0	0	1	Period*(1-6%)	F*(1+6.38%)
1	1	1	0	0	0	Period*(1-7%)	F*(1+7.53%)
1	1	0	1	1	1	Period*(1-8%)	F*(1+8.7%)
1	1	0	1	1	0	Period*(1-9%)	F*(1+9.89%)

Trimming code						Clock Period	Frequency
CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]		
1	1	0	1	0	1	Period*(1-10%)	F*(1+11.11%)
1	1	0	1	0	0	Period*(1-11%)	F*(1+12.36%)
1	1	0	0	1	1	Period*(1-12%)	F*(1+13.64%)
1	1	0	0	1	0	Period*(1-13%)	F*(1+14.94%)
1	1	0	0	0	1	Period*(1-14%)	F*(1+16.28%)
1	1	0	0	0	0	Period*(1-15%)	F*(1+17.65%)
1	0	1	1	1	1	Period*(1-16%)	F*(1+19.05%)
1	0	1	1	1	0	Period*(1-17%)	F*(1+20.48%)
1	0	1	1	0	1	Period*(1-18%)	F*(1+21.95%)
1	0	1	1	0	0	Period*(1-19%)	F*(1+23.46%)
1	0	1	0	1	1	Period*(1-20%)	F*(1+25%)
1	0	1	0	1	0	Period*(1-21%)	F*(1+26.58%)
1	0	1	0	0	1	Period*(1-22%)	F*(1+28.21%)
1	0	1	0	0	0	Period*(1-23%)	F*(1+29.87%)
1	0	0	1	1	1	Period*(1-24%)	F*(1+31.58%)
1	0	0	1	1	0	Period*(1-25%)	F*(1+33.33%)
1	0	0	1	0	1	Period*(1-26%)	F*(1+35.14%)
1	0	0	1	0	0	Period*(1-27%)	F*(1+36.99%)
1	0	0	0	1	1	Period*(1-28%)	F*(1+38.89%)
1	0	0	0	1	0	Period*(1-29%)	F*(1+40.85%)
1	0	0	0	0	1	Period*(1-30%)	F*(1+42.86%)
1	0	0	0	0	0	Period*(1-31%)	F*(1+44.93%)

6.1.49 Bank 4 RD SFCR (Trim bits of Sub-Frequency IRC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	SC4	SC3	SC2	SC1	SC0
0	0	0	R/W	R/W	R/W	R/W	R/W

Bits 4~0 (SC4~SC0): Trim bits of sub frequency IRC

Trimming code					Clock Period	Frequency
SC4	SC3	SC2	SC1	SC0		
0	0	0	0	0	Period*(1+32%)	F*(1-24.24%)
0	0	0	0	1	Period*(1+30%)	F*(1-23.08%)
0	0	0	1	0	Period*(1+28%)	F*(1-21.88%)
0	0	0	1	1	Period*(1+26%)	F*(1-20.64%)
0	0	1	0	0	Period*(1+24%)	F*(1-19.37%)

Trimming code					Clock Period	Frequency
SC4	SC3	SC2	SC1	SC0		
0	0	1	0	1	Period*(1+22%)	F*(1-18.03%)
0	0	1	1	0	Period*(1+20%)	F*(1-16.67%)
0	0	1	1	1	Period*(1+18%)	F*(1-15.27%)
0	1	0	0	0	Period*(1+16%)	F*(1-13.79%)
0	1	0	0	1	Period*(1+14%)	F*(1-12.28%)
0	1	0	1	0	Period*(1+12%)	F*(1-10.72%)
0	1	0	1	1	Period*(1+10%)	F*(1-9.09%)
0	1	1	0	0	Period*(1+8%)	F*(1-7.41%)
0	1	1	0	1	Period*(1+6%)	F*(1-5.66%)
0	1	1	1	0	Period*(1+4%)	F*(1-3.85%)
0	1	1	1	1	Period*(1+2%)	F*(1-1.96%)
1	1	1	1	1	Period (default)	F (default)
1	1	1	1	0	Period*(1-2%)	F*(1+2.04%)
1	1	1	0	1	Period*(1-4%)	F*(1+4.17%)
1	1	1	0	0	Period*(1-6%)	F*(1+6.38%)
1	1	0	1	1	Period*(1-8%)	F*(1+8.7%)
1	1	0	1	0	Period*(1-10%)	F*(1+11.11%)
1	1	0	0	1	Period*(1-12%)	F*(1+13.64%)
1	1	0	0	0	Period*(1-14%)	F*(1+16.28%)
1	0	1	1	1	Period*(1-16%)	F*(1+19.05%)
1	0	1	1	0	Period*(1-18%)	F*(1+21.95%)
1	0	1	0	1	Period*(1-20%)	F*(1+25%)
1	0	1	0	0	Period*(1-22%)	F*(1+28.2%)
1	0	0	1	1	Period*(1-24%)	F*(1+31.58%)
1	0	0	1	0	Period*(1-26%)	F*(1+35.13%)
1	0	0	0	1	Period*(1-28%)	F*(1+38.89%)
1	0	0	0	0	Period*(1-30%)	F*(1+42.86%)

6.1.50 Bank 4 RE~RF (Reserved)

6.1.51 Bank 5 R5~RF (Reserved)

6.1.52 Bank 6 R5~RF (Reserved)

6.1.53 Bank 7 R5~RB (Reserved)

6.1.54 Bank 7 RC: TBWCR (Table Write Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	IAPEN
0	0	0	0	0	0	0	R/W

Bit 0 (IAPEN): IAP enable bit

0: IAP mode Disable.

1: IAP mode Enable.

6.1.55 Bank 7 RD: FLKR (Flash Key Register for Table Write Use)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FLK7	FLK6	FLK5	FLK4	FLK3	FLK2	FLK1	FLK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This FLKR register is used by table write IAP mode operation. The IAP enable signal is generated when a specific value is written into this register, e.g., **0xB4**. The register is designed to make sure that IAP operation occurs for flash update.

Note: After executing TBW instructions, H/W will clear FLKR register. To do table write again, 0xB4 must be refilled into FLKR.

6.1.56 Bank 7 RE: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TB7 ~ TB0): Table Point Address Bits 7~0.(This register for Table read and write)

6.1.57 Bank 7 RF: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	TB11	TB10	TB9	TB8
R/W	0	0	0	R/W	R/W	R/W	R/W

(This register for Table read and write)

Bit 7 (HLB): Take MLB or LSB at machine code from ROM.

HLB	Read to Register data value description
0	Read byte value is Bit7~bit0 from machine code to A reg.
1	Read byte value is Highest bit fixed “0” and bit12~bit8 from machine code.

Bits 6~4: Not used, set to "0" at all time.

Bits 3 ~0 (TB11~TB8): Table Point Address Bits 12~8.

※Note :

ROM Code Buffer (Start)	Table Write ROM Address (Destination)
BANK6 0x20	[TBPT] Low byte(bits7~0)
BANK6 0x21	[TBPT] High byte(bits14~8)
BANK6 0x22	[TBPT+1] Low byte(bits7~0)
BANK6 0x23	[TBPT+1] High byte(bits14~8)
⋮	⋮
BANK6 0x3E	[TBPT+15] Low byte(bits7~0)
BANK6 0x8F	[TBPT+15] High byte(bits14~8)
BANK7 0x20	[TBPT+16] Low byte(bits7~0)
BANK7 0x21	[TBPT+16] High byte(bits14~8)
⋮	⋮
BANK7 0X3E	[TBPT+31] Low byte(bits7~0)
BANK7 0X3F	[TBWA+31] High byte(bits14~8)

Notes:

1. When following IAP procedure, we must fill programs we desire update into BANK6 0x20~0x3F and BANK7 0x20~0x3F (64 Byte in total). Therefore, by using flash table write, MCU will be able to program code in this RAM area to set Flash ROM address in order.

2. Bank6 0x20/0x21 is IAP flash rom, starts address on every page.

3. IAP data verification must be done by user program. First, write data into RAM BANK6 0x20~0x3F and BANK7 0x20~0x3F. Then, do TBW instruction to program HW flash. Finally, do Table Read (64 Byte) from flash then equally compare data with RAM BANK 6 and 7.

4. FW verify: Read the data on flash page for serval times then compare it with SRAM.

6.2 WDT and Pre-scaler

This is one 8-bit counter available as pre-scalers for the WDT respectively. The WPSR0~WPSR2 bits of the WDTCR register are used to determine the pre-scaler of WDT. The WDT and pre-scaler will be cleared by the “WDTC” and “SLEP” instructions. Figure 6-4 depicts the circuit diagram of WDT.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of WDTCR register. With no pre-scaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

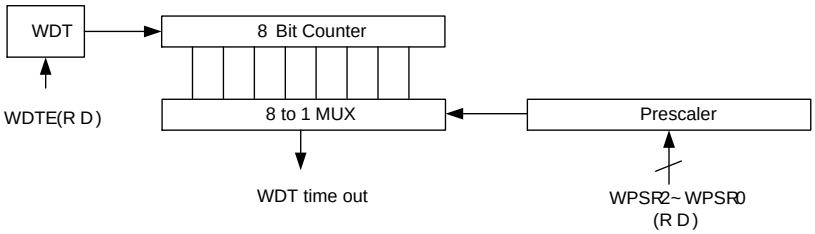


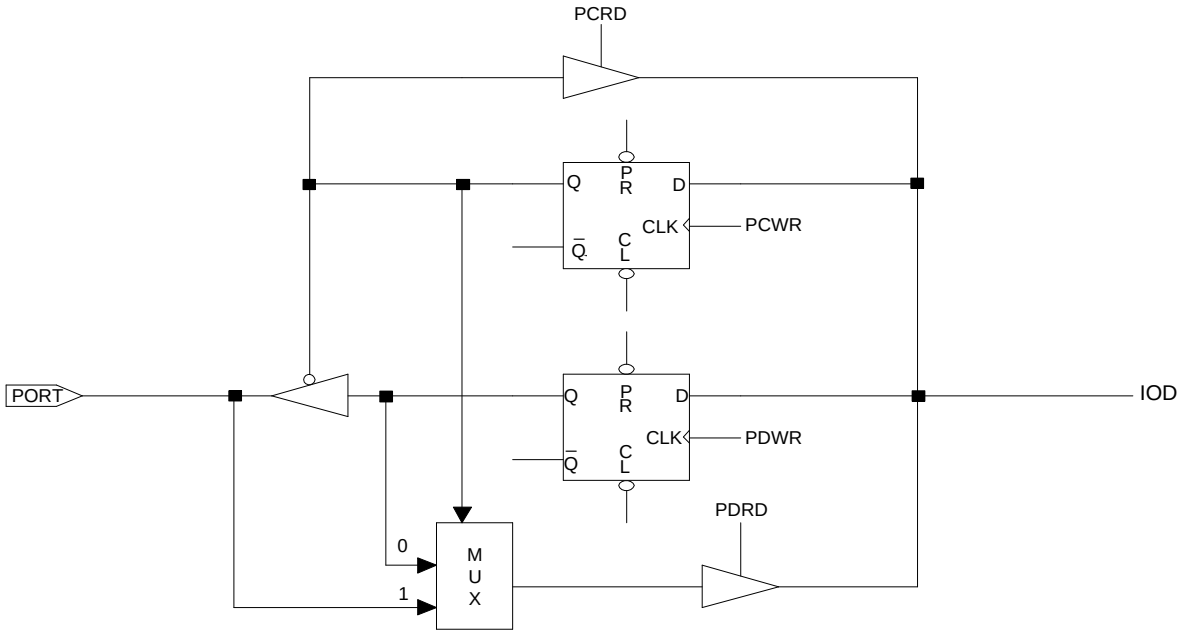
Figure 6-4 WDT Block Diagram

[1] NOTE: VDD=5V, WDT time-out period = 16.5ms ± 8%. VDD=3V, WDT time-out period = 18ms ± 8%.

6.3 I/O Ports

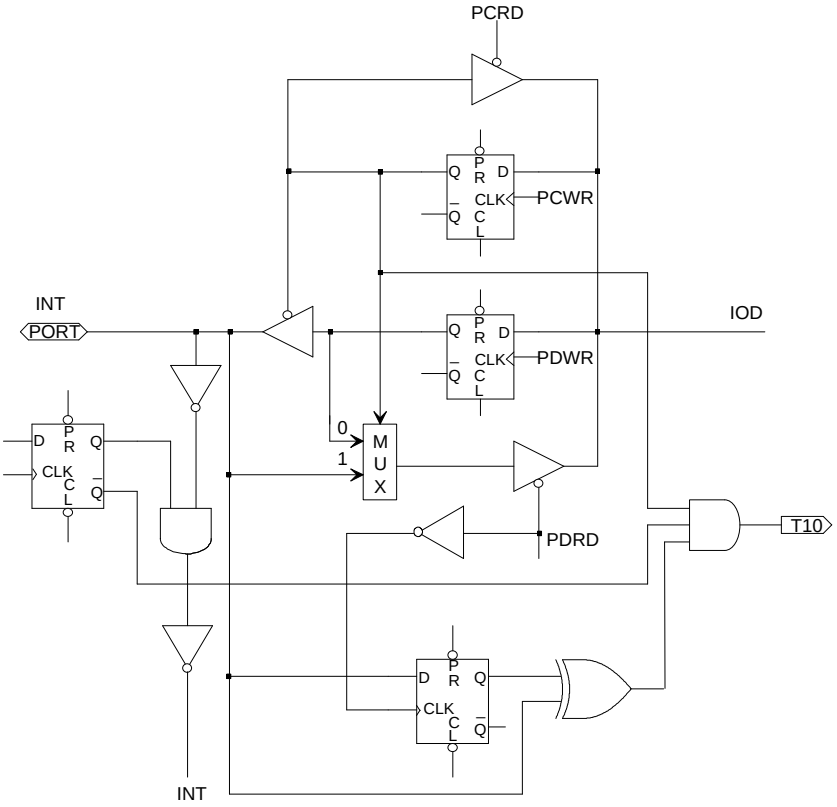
The I/O registers, Port 5~Port7 are bi-directional tri-state I/O ports. All can be pulled high and pulled low internally by software. Port 6 have wake up and interrupt function. Further, Ports 5~7 also has input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port A are shown in the following Figure 6-5, Figure 6-6, Figure 6-7, and Figure 6-8.



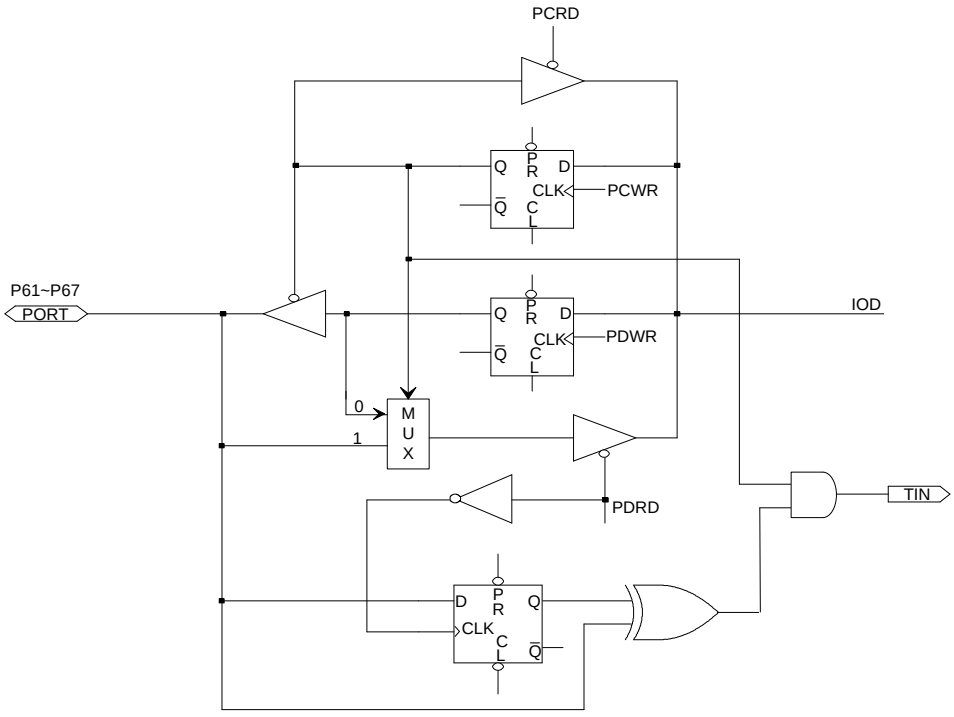
Note: Pull-down is not shown in the figure.

Figure 6-5 The Circuit of I/O Port and I/O Control Register for Ports 5~7



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-6 The Circuit of I/O Port and I/O Control Register for /INT



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-7 The Circuit of I/O Port and I/O Control Register for Port 6

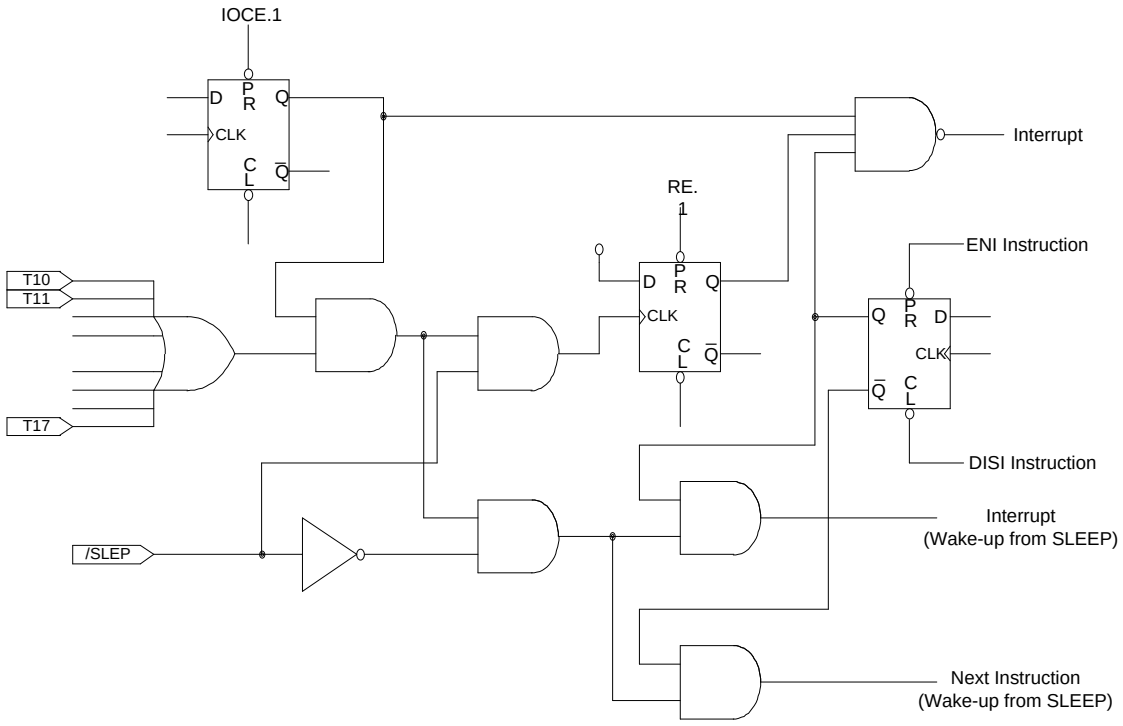


Figure 6-8 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 2 Usage of Port 6 Input Changed Wake-up/Interrupt Function

Usage of Port 5~7 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before SLEEP	(a) Before SLEEP
1. Disable WDT	1. Disable WDT
2. Read I/O Port (MOV R6,R6)	2. Read I/O Port (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set ICWE=1)	4. Enable wake-up bit (Set ICWE=1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (0004H)
	2. IF "DISI" → Next instruction

6.4 Reset and Wake-up

6.4.1 Reset

A RESET is initiated by one of the following events-

(1) Power on reset.

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approx. 18ms[2] (one oscillator start-up timer period) after the reset is detected. And if the /Reset pin goes “low” or WDT time-out is active, a reset is generated, in IRC mode the reset time is 1 clocks. Once the RESET occurs, the following functions are performed.

• The oscillator is running, or will be started.

• The Program Counter (R2) is set to all "0".

• All I/O port pins are configured as input mode (high-impedance state).

• The Watchdog timer and pre-scaler are cleared.

• The bits of the control register are set as Table 4.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up generated, in IRC mode the wake-up time is 1 clocks. The controller can be awakened by-

(1) External reset input on /RESET pin,

(2) WDT time-out (if enabled), or

(3) External (/INT) pin changes (if EXWE is enabled).

(4) Port input status changes (if ICWE is enabled).

The first two cases will cause the EM78F724N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3, 4, and5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x09~0x3C after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Only one of the Cases 3 to 4 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM78F724N can only be woken-up by Case 1 or 2. Refer to the section on Interrupt for further details.

[2] NOTE: set up time period = 16ms ± 6%

[b] If External (P60,/INT0) (P61, /INT1) pin change is used to wake-up EM78F724N and EXWE0,1 bit is enabled before SLEP, WDT must be disabled. Hence, the EM78F724N can only be woken-up by Case 3.

[c] If Port Input Status Change is used to wake-up EM78F724N and corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM78F724N can only be woken-up by Case 4.

Table 3 All kinds of wake-up mode and interrupt mode as shown below:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TM1/2 Interrupt (Used as timer/Capture)	TM1/2IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TM1/2IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TM1/2 Interrupt (Used as counter)	TM1/2IE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	TM1/2IE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
External INT	EXWEx = 0, EXIEx = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	EXWEx = 0, EXIEx = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWEx = 1, EXIEx = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	EXWEx = 1, EXIEx = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin change	ICWE = 0, PxICIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 0, PxICIE = 1	Wake-up is invalid.		Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, PxICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	ICWE = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit complete Interrupt	URWK = 0, UTIE = 0	Wake-up is invalid.		Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.	
	URWK = 0, UTIE = 1			Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
	URWK = 1, UTIE = 0,			Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	URWK = 1, UTIE = 1,			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive data Buffer full Interrupt	URWK = 0, URIE = 0	Wake-up is invalid.		Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.	
	URWK = 0, URIE = 1			Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	URWK = 1, URIE = 0,			Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	URWK = 1, URIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	URWK = 0, UERRIE = 0	Wake-up is invalid.		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	URWK = 0, UERRIE = 1			Wake-up is invalid.		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	URWK = 1, UERRIE = 0,			Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	URWK = 1, UERRIE = 1,			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT Timeout		Wake up + Reset		Wake up + Reset		Reset		Reset	

6.4.2 Summary of Register Initial Values

Legend: ***x:*** *Not used* ***P:*** *Previous value before reset*
U: *Unknown or don't care* ***t:*** *Check tables under Section 6.5.4*

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	R1 (BSR)	Bit Name	-	SBS2	SBS1	SBS0	-	GBS2	GBS1	GBS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	0	P	P	P
0x02	R2 (PCL)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	-	-	INT	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Sleep/Idle	0	0	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	IGBS1	IGBS0	RS5	RS4	RS3	RS2	RS1	RS0
		Power-On	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	-	-	-	P54	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	**P**	0	0	0	0
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	-	P65	-	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	P	0	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0, R7 (Port 7)	Bit Name	-	P76	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	0	0	0	0	0	0
0x08	BANK 0, R8 (IOCR 5)	Bit Name	-	-	-	IOCR54	-	-	-	-
		Power-On	0	0	0	1	0	0	0	0
		/RESET and WDT	0	0	0	1	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	P	0	0	0	0
0x09	BANK 0, R9 (IOCR 6)	Bit Name	IOCR67	-	IOCR65	-	IOCR63	IOCR62	IOCR61	IOCR60
		Power-On	1	0	1	0	1	1	1	1
		/RESET and WDT	1	0	1	0	1	1	1	1
		Wake-Up from Sleep/Idle	P	0	P	0	P	P	P	P
0x0A	BANK 0, RA (IOCR 7)	Bit Name	-	IOCR76	-	-	-	-	-	-
		Power-On	0	1	0	0	0	0	0	0
		/RESET and WDT	0	1	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	0	0	0	0	0	0
0X0B	BANK 0, RB (WUCR)	Bit Name	URWE	-	-	-	-	EX2WE	EX1WE	ICWE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	0	0	P
0x0C	BANK 0, RC (OMCR)	Bit Name	CPUS	IDLE	PERCS	CLK1	CLK0	SFS	RCM1	RCM0
		Power-On	1	1	0	0	0	Code Opt.	Code Opt.	Code Opt.
		/RESET and WDT	1	1	0	0	0	P	P	P
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0D	BANK 0, RD (WDTCR)	Bit Name	WDTE	EIS1	EIS0	SFSS	PSWE	PSW2	PSW1	PSW0
		Power-On	0	0	0	Code Opt.	0	0	0	0
		/RESET and WDT	0	0	0	P	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0E	BANK 0, RE (SFR1)	Bit Name	SHSF	-	-	TM2SF	TM1SF	EXSF1	EXSF0	ICSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	P	P	0	P	P
0x0F	BANK 0, RF (SFR1)	Bit Name	UERRSF	URSF	UTSF	-	-	-		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	0	0	0
0x05	BANK 1, R5 (TM1CR1)	Bit Name	TM1S	TM1RC	TM1SS1		-	TM1MOS	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	P	0	0
0x06	BANK 1, R6 (TM1CR2)	Bit Name	-	TM1M1	TM1M0	TM1SS0	TM1CK3	TM1CK2	TM1CK1	TM1CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	P	P
0x07	BANK 1, R7 (TM1DBH)	Bit Name	TM1DB15	TM1DB14	TM1DB13	TM1DB12	TM1DB11	TM1DB10	TM1DB9	TM1DB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X08	BANK 1, R8 (TM1DBL)	Bit Name	TM1DB7	TM1DB6	TM1DB5	TM1DB4	TM1DB3	TM1DB2	TM1DB1	TM1DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	BANK 1, R9 (TM1DAH)	Bit Name	TM1DA15	TM1DA14	TM1DA13	TM1DA12	TM1DA11	TM1DA10	TM1DA9	TM1DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	BANK 1, RA (TM1DAL)	-	TM1DA7	TM1DA6	TM1DA5	TM1DA4	TM1DA3	TM1DA2	TM1DA1	TM1DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	BANK 1, RB (EIESCR)	Bit Name	EIES1	EI1NRE	EI1NR1	EI1NR0	EIES0	EI0NRE	EI0NR1	EI0NR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	BANK 1, RC (STKMON)	Bit Name	STOV					STL2	STL1	STL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	0	P	P	P
0X0E	BANK 1, RE (IMR1)	Bit Name	SHIE	-	-	TM2IE	TM1IE	EXIE1	EXIE0	ICIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	P	P	P	P	P
0X0F	BANK 1, RF (IMR2)	Bit Name	UERRIE	URIE	UTIE	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	0	0	0

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X05	Bank 2, R5 (URCR1)	Bit Name	UINVEN	-	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-On	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0X06	Bank 2, R6 (URS)	Bit Name	-	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	P	P
0X07	Bank 2, R7 (URTD)	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X08	Bank 2, R8 (URRDL)	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 2, RA (URCR2)	Bit Name	-	-	-	-	-	-	-	URSS
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	0	0	P
0X05	BANK 3, R5 (TM2CR1)	Bit Name	TM2S	TM2RC	TM2SS1			TM2MOS		
		Power-On	0	0	0		0	0	0	0
		/RESET and WDT	0	0	0		0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P		0	P	0	0

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X06	BANK 3, R6 (TM2CR2)	Bit Name			TM2M0	TM2SS0	TM2CK3	TM2CK2	TM2CK1	TM2CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	P	P	P	P	P	P
0X07	BANK 3, R7 (TM2DBH)	Bit Name	TM2DB15	TM2DB14	TM2DB13	TM2DB12	TM2DB11	TM2DB10	TM2DB9	TM2DB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	P	P	P	P
0X08	BANK 3, R8 (TM2DBL)	Bit Name	TM2DB7	TM2DB6	TM2DB5	TM2DB4	TM2DB3	TM2DB2	TM2DB1	TM2DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	BANK 3, R9 (TM2DAH)	Bit Name	TM2DA15	TM2DA14	TM2DA13	TM2DA12	TM2DA11	TM2DA10	TM2DA9	TM2DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	BANK 3, RA (TM2DAL)	Bit Name	TM2DA7	TM2DA6	TM2DA5	TM2DA4	TM2DA3	TM2DA2	TM2DA1	TM2DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	BANK 3, RC (EECR1)	Bit Name							RD	WR
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	P	P
0X0D	Bank 3, RD (EECR2)	Bit Name	EEWE	EEDF	EEPC					
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	0	0	0	0	0

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	Bank 3, RE (EERA)	Bit Name	-	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	P	P	P	P	P	P	P
0X0F	Bank 3, RF (EERD)	Bit Name	EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 4, R5 (P6PHCR)	Bit Name	PH67	-	PH65	-	PH63	PH62	PH61	PH60
		Power-On	1	0	1	0	1	1	1	1
		/RESET and WDT	1	0	1	0	1	1	1	1
		Wake-Up from Sleep/Idle	P	0	P	0	P	P	P	P
0X06	Bank 4, R6 (P6PLCR)	Bit Name	PL67	-	PL65	-	PL63	PL62	PL61	PL60
		Power-On	1	0	1	0	1	1	1	1
		/RESET and WDT	1	0	1	0	1	1	1	1
		Wake-Up from Sleep/Idle	P	0	P	0	P	P	P	P
0X07	Bank 4, R7 (P57PHCR)	Bit Name	-	-	-	-	P7HPH	-	P5HPH	-
		Power-On	0	0	0	0	1	0	1	0
		/RESET and WDT	0	0	0	0	1	0	1	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	0	P	0
0X08	Bank 4, R8 (P57PLCR)	Bit Name	-	-	-	-	P7HPL	-	P5HPL	-
		Power-On	0	0	0	0	1	0	1	0
		/RESET and WDT	0	0	0	0	1	0	1	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	0	P	0
0X09	BANK 4, R9 (P6HDSCR)	Bit Name	-	-	H65	-	H63	H62	H61	H60
		Power-On	0	0	1	0	1	1	1	1
		/RESET and WDT	0	0	1	0	1	1	1	1
		Wake-Up from Sleep/Idle	0	0	P	0	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0C	BANK 4, RC (MFCR)	Bit Name			CA5	CA4	CA3	CA2	CA1	CA0
		Power-On	0	0	Code Opt.	Code Opt.	Code Opt.	Code Opt.	Code Opt.	Code Opt.
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Sleep/Idle	P	0	P	P	P	P	P	P
0X0D	BANK 4, RD (SFCR)	Bit Name				SC4	SC3	SC2	SC1	SC0
		Power-On	0	0	0	Code Opt.	Code Opt.	Code Opt.	Code Opt.	Code Opt.
		/RESET and WDT	0	0	0	P	P	P	P	P
		Wake-Up from Sleep/Idle	0	0	0	P	P	P	P	P
0X0C	BANK7, RC (TBWCR)	Bit Name	-	-	-	-	-	-	-	IAPEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X0D	BANK 7, RD (FLKR)	Bit Name	FLK7	FLK6	FLK5	FLK4	FLK3	FLK2	FLK1	FLK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	BANK 7, RE (TBTPL)	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	BANK 7, RF (TBTPH)	Bit Name	HLB	-	-	-	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P

The Status of RST, T, and P of Status Register

A RESET condition is initiated by the following events:

1. A power-on condition,
2. A high-low-high pulse on /RESET pin, and
3. Watchdog timer time-out.

The values of T and P, listed in Table 5 are used to check how the processor wakes up. Table 5 shows the events that may affect the status of T and P.

Table 5 Values of RST, T and P after RESET

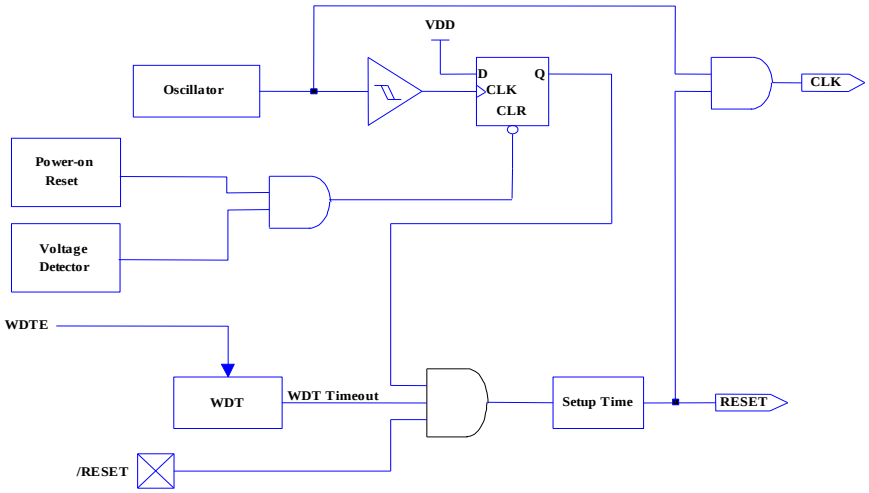
Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous status before reset

Table 6 Status of T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous value before reset



Block Diagram of Controller Reset

6.5 Interrupt

The EM78F724N has 9 interrupts (3 external, 6 internal) as listed below:

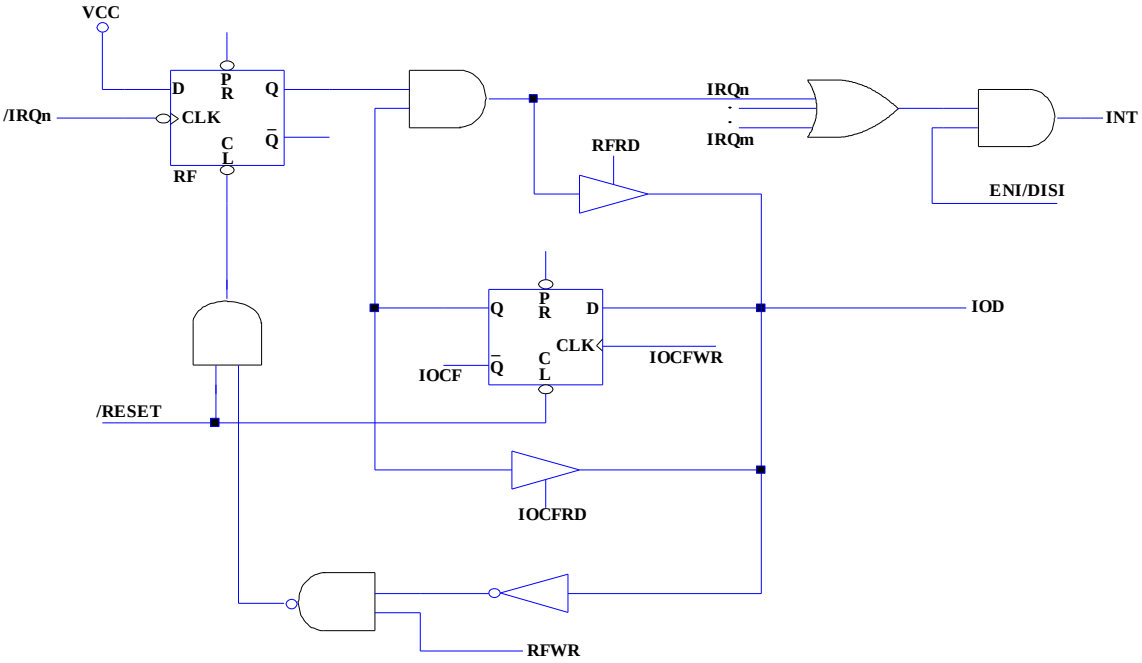
Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal/External	Reset	-	-	0	High 0
External	INT0,1	ENI + EXIE0=1	EXSF0	9	1
		ENI + EXIE1=1	EXSF1		
External	Port pin status Change	ENI + ICIE=1	ICSF	C	2
Internal	System hold	ENI+SHIE	SHSF	27	3
Internal	TM1	ENI + TM1IE=1	TM1SF	2A	4
Internal	TM2	ENI + TM2IE=1	TM2SF	33	5
Internal	UART transmit	ENI+UTIE=1	UTSF	36	6
Internal	UART error	ENI+UERRSIE=1	UERRSF	39	7
Internal	UART receive	ENI +URIE=1	URSF	3C	8

Bank0 RE~RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank1 RE~RF is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

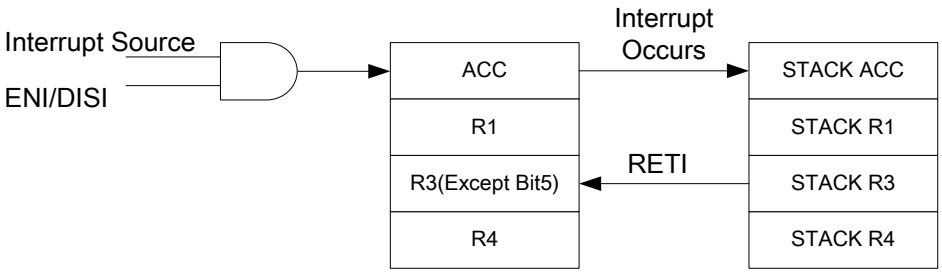
The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt equipped with digital noise rejection circuit (input pulse less than **4 system clocks time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 6) and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 (Bit 0~Bit 6) and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 (Bit 0~Bit 6) and R4 will be pushed back.

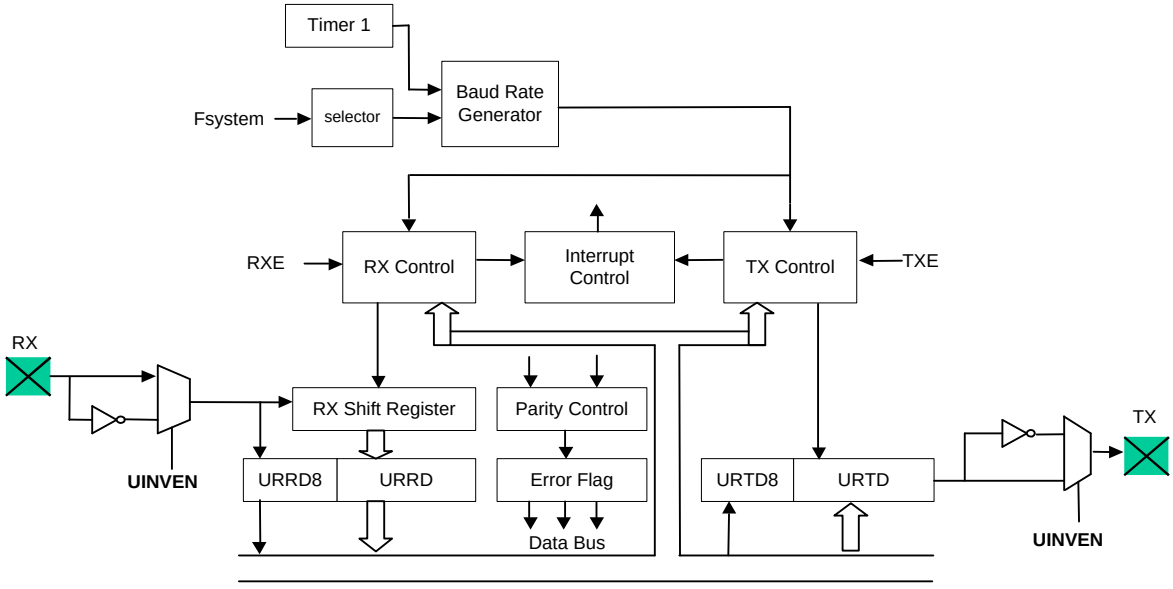


Interrupt Input Circuit



Interrupt Backup Diagram

6.6 UART (Universal Asynchronous Receiver/Transmitter)



Function Block Diagram

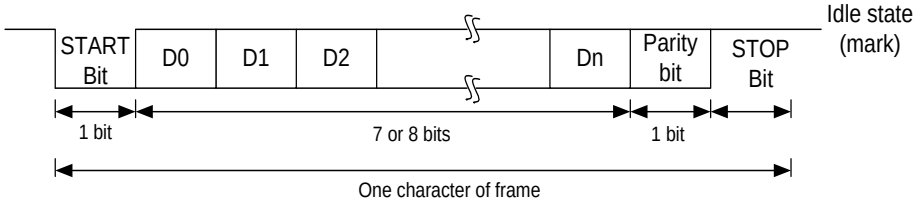
In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

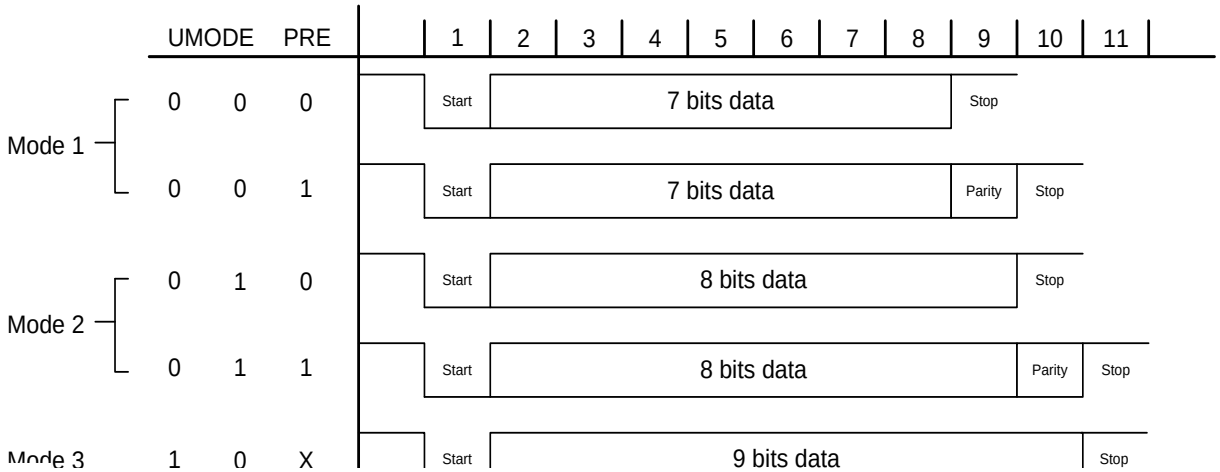
In receiving, the UART synchronizes on the falling edge of the start bit. When two or three “0” are detected during three samples, it is recognized as normal start bit and the receiving operation is started.



Data Format in UART

UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. Figure below shows the data format in each mode.



UART Model

Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBF bit of the URCR register will be cleared by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one “0” bit is output.
6. Transmit data: 7 or8 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one “1” bit (stop bit) is output.

Mark state: output “1” continues until the start bit of the next transmitted data.
After transmitting the stop bit, the UART generates a UTSF interrupt (if enabled).

Receiving

In receiving, the UART operates as follows:

1. Set RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to 1. This means UART interrupt will occur.
4. The UART makes the following checks:
   (a) Parity check: The number of 1 of the received data must match the even or odd parity setting of the EVEN bit in the URS register.

(b) Frame check: The start bit must be 0 and the stop bit must be 1.

(c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

If any checks failed, the UERRSF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software otherwise, UERRSF interrupt will occur when the next byte is received.

5. Read received data from URRD register. And URBF bit will be set by hardware.

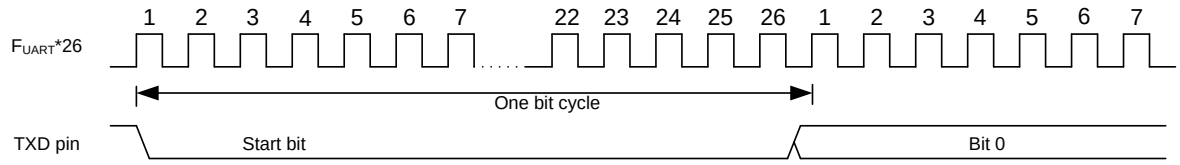
Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

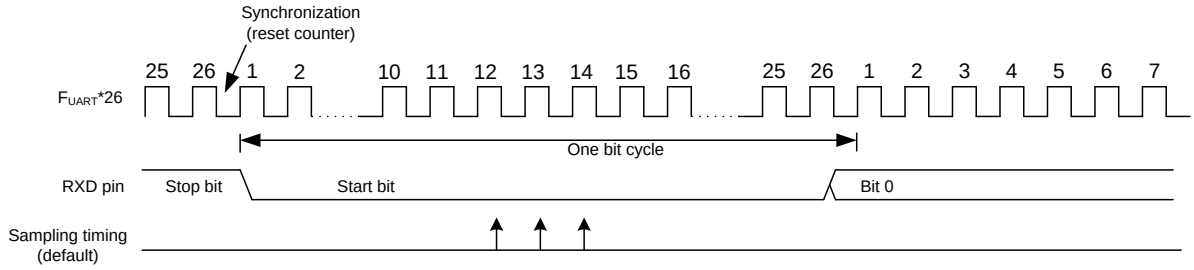
The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

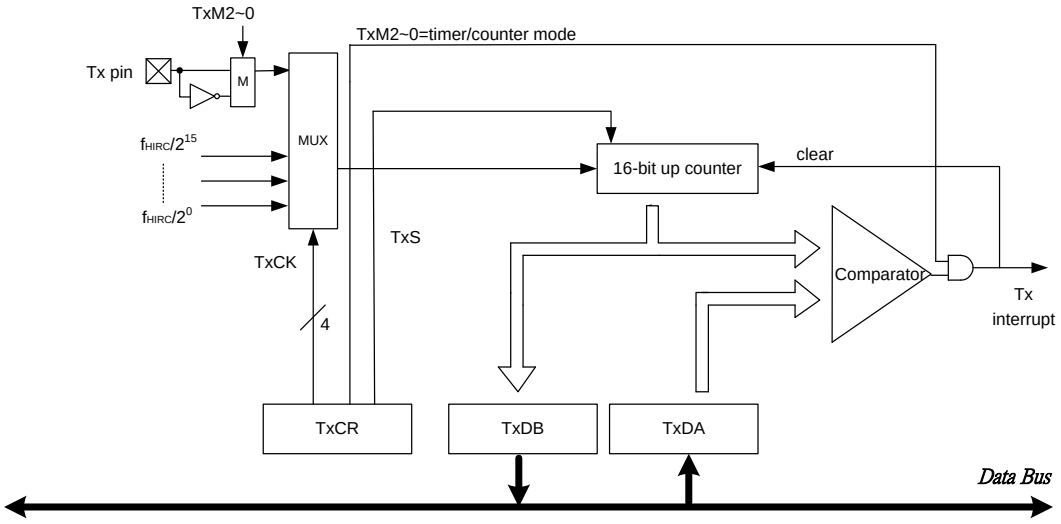


UART Timing

6.7 Timer/Counter 1/2

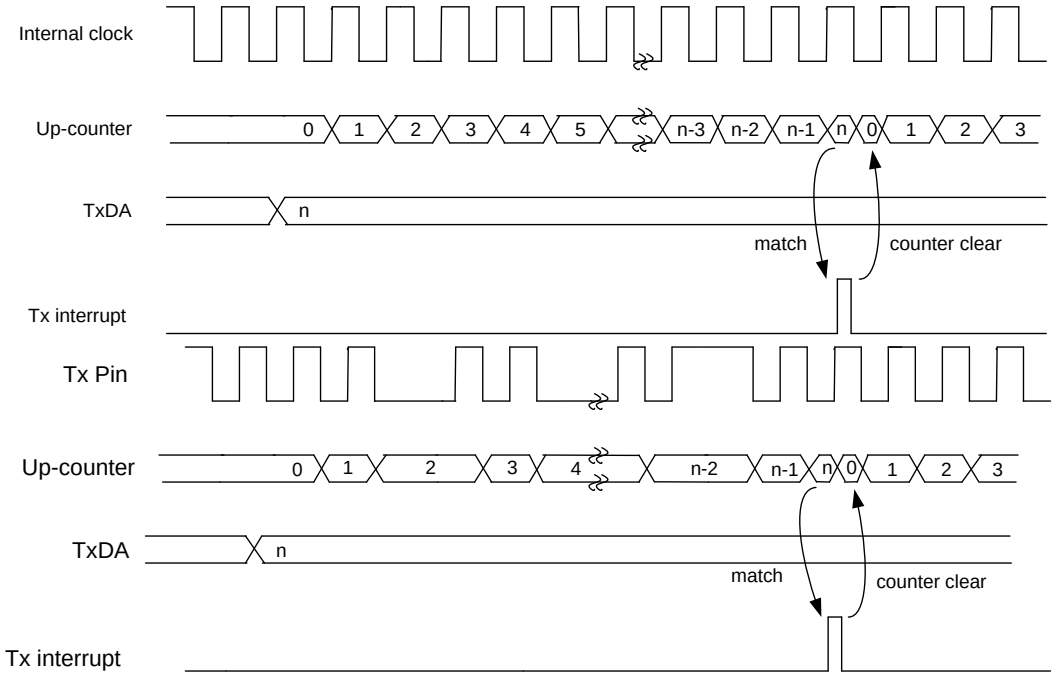
There are two timers in the EM78F724N. Timer 1 and Timer 2 are 16 bits up-counter.

Timer/Counter Mode



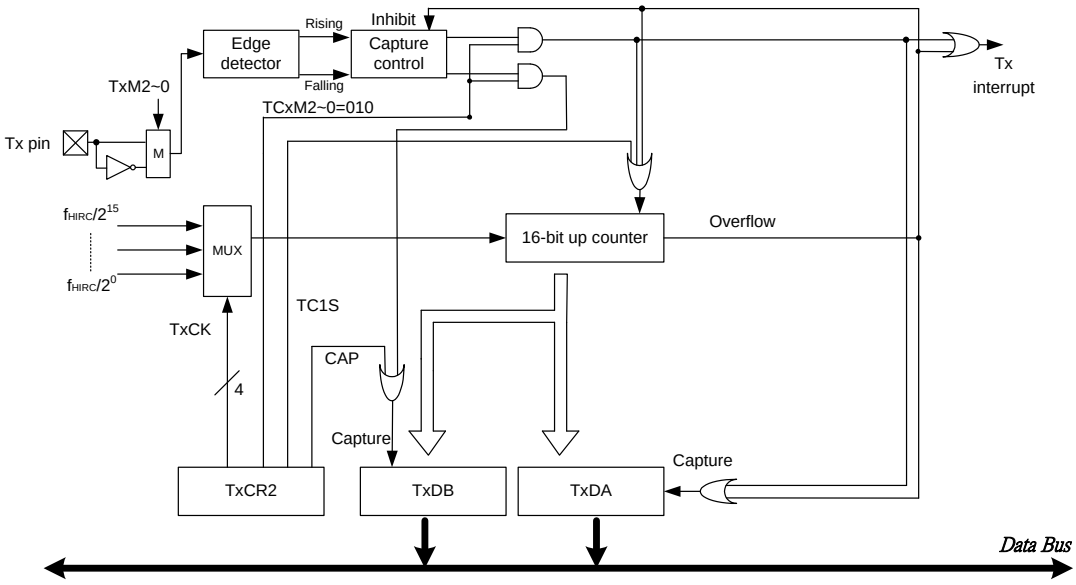
Timer/Counter mode

In Timer/Counter mode, counting up is performed using internal clock(F_{HIRC}) or Tx pin. When the contents of up-counter are matched the TxDA, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TxDB by setting TxRC to “1”.



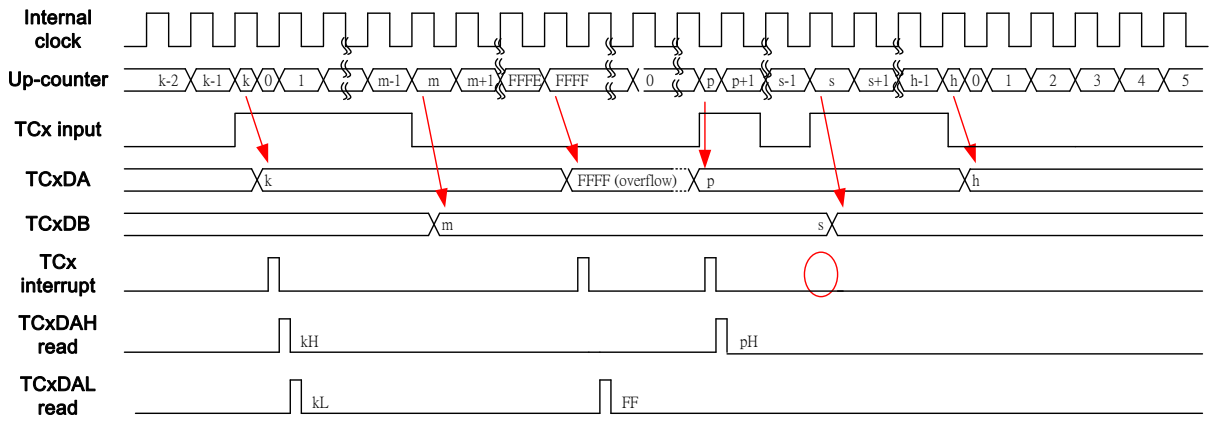
Timer/Counter mode waveform

Capture Mode

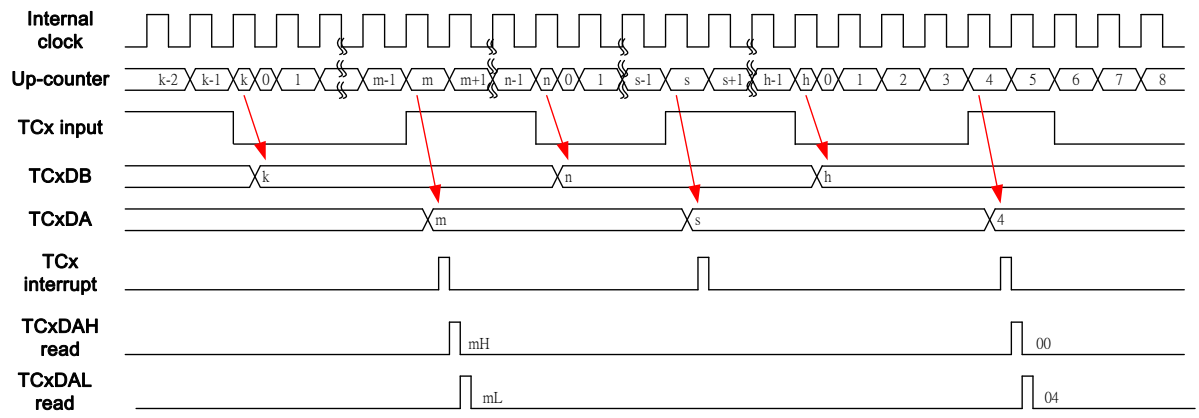


Capture Mode

In Capture mode, the pulse width, period and duty of the Tx input pin are measured in this mode, which can be used to decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of Tx pin , the contents of counter is loaded into TxDA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TA pint, the contents of counter are loaded into TxDB. At this time, the counter is still countering. Once the next rising edge of Tx pin triggers, the contents of counter are loaded into TxDA, the counter is cleared and interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TxDA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TxDA value is FFH.



Capture Mode Waveform 1



Capture mode waveform 2

Notes

In capture interrupt service routine or after waking up from idle, we must do the following processes in order.

1. Clear Timer SFR flag.
2. Process user program.
3. Read TM1DAH.
4. Read TM1DAL in the end.

6.8 Code Option Register

The EM78F724N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.8.1 Code Option Register (Word 0)

Word 0													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**HLP**	**-**	**-**	**RESETENB**	**-**	**TBWEN**	**ENWDTB**	**-**	**-**	**-**	**EEPR2**	**EEPR1**	**EEPR0**
1	Low	-	-	Enable	-	Enable	Enable	-	-	-	High	High	High
0	High	-	-	Disable	-	Disalbe	Disable	-	-	-	Low	Low	Low
default	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 12 (HLP): Power consumption selection.

0: High power consumption, applies to working frequency above 400kHz

1: Low power consumption, applies to working frequency at 400kHz or below 400kHz

Bit 11 ~ Bit 10: Not used, always set to "0"

Bit 9 (RESETENB): Reset pin enable bit

0: Disable, P65//RESET=>P65 (default)

1: Enable, P65//RESET=>RESET pin.

Bit 8 ~ Bit 7: Not used, always set to "0"

Bit 6 (ENWDTB): Watchdog timer enable bit

0: Disable

1: Enable

Bits 2~0 (EEPR2~EEPR0): EEPROM Protect Bit. Each protect status is as follows:

EEPR2	EEPR1	EEPR0	Protect
1	1	1	Enable
0	0	0	Disable

6.8.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**COBS1**	**COBS2**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**IRCWUT1**	**IRCWUT0**
1	-	High	High	High	High	High	High	High	High	High	High	High	High
0	-	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
default	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit 12 : Not used, set to "0" at all time

Bits 11 (COBS1): Code Option bit selection 1 for SFCR reg.

0: Sub IRC **trim bits** get from code option R2 (bit12~8) (default)

1: Sub IRC **trim bits** get from Bank4 RD

Bits 10 (COBS2): Code Option bit selection 1 for MFCR reg.

0: Main IRC **trim bits** get from code option R1 (bit9~4) (default)

1: Main IRC **trim bits** get from Bank4 RC

Bit 9 ~ Bit 4 (C5 ~ C0): Internal RC mode calibration bits. (IRC frequency auto calibration)

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode selection bits

RCM1	RCM0	Frequency
0	**0**	Reserved
0	**1**	500kHz
1	**0**	1 MHz
1	**1**	8MHz

Bits 1~0 (IRCWUT1~IRCWUT0): IRC Warm Up Time.

IRCWUT1	IRCWUT0	Clock
0	**0**	1 clock
0	**1**	2 clocks
1	**0**	4 clocks
1	**1**	8 clocks

CPU Mode Switch	IRC Frequency	Waiting Time before CPU Starting to Work
Sleep → Normal Idle→ Normal Green → Normal	500kHz, 1 MHz,8MHz	WSTO + SST+1/2/4/8 clocks (main frequency)
Sleep → Green Idle → Green	128kHz	WSTO +SST+1 clock (sub frequency)

6.8.3 Code Option Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**SC4**	**SC3**	**SC2**	**SC1**	**SC0**	**EFTIMEN**	**SHCLK1**	**SHCLK0**	**SFS**	**IRCPSS**	**-**	**SFSS**	**-**
1	High	High	High	High	High	Disable	High	High	High	VDD	-	High	-
0	Low	Low	Low	Low	Low	Enable	Low	Low	Low	Regulator	-	Low -	-
Default	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 12 ~ 8 (SC4 ~ SC0): sub-frequency calibrator (WDT frequency auto calibration)

Bit 7 (EFTIMEN): EFT improvement Enable bit.

0: Enable low pass filter, the filter is <10MHz (Default)

1: Disable low pass filter

Bits 6~5 (SHCLK1~ SHCLK0): System hold clock select bits

Shcksel1:0	System Hold Clock
00	8 clock (default)
01	4 clock
10	16 clock
11	32 clock

Bits 4 (SFS): Sub-frequency select.

Bits 1 (SFSS): Sub-frequency Sub select.

SFS	SFSS	Frequency
0	**0**	16kHz
0	**1**	No Use
1	**0**	128kHz
1	**1**	Reserved

Bit 3 (IRCPSS) : IRC Power Source Select

0: Enable regulator for improving IRC accurately but more power consumed.

1: Disable regulator for saving power but more error of IRC.

Bit 2 and Bit 0: Not used, always set to "0"

6.9 Power on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes into steady state. The EM78F724N is equipped with a built-in Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd rises fast enough (50 ms or less). However, under critical applications; extra devices may still be required to assist in solving power-up problems.

6.10 External Power-on Reset Circuit

The circuit shown in Figure 6-9 uses an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to achieve minimum operation voltage. This circuit is used when the power supply has slow rising time. As the current leakage from the /RESET pin is ±5μA, it is recommended that R should not

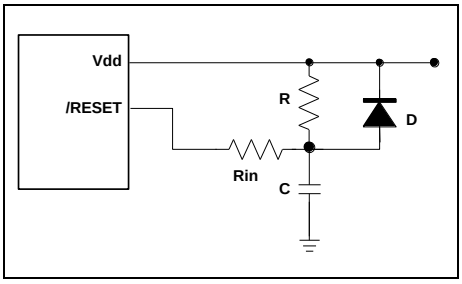


Figure 6-9 External Power-up Reset Circuit

be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the moment of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin), will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.11 Residue-Voltage Protection

When battery is replaced, the device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figures below show how to accomplish a proper residue-voltage protection circuit.

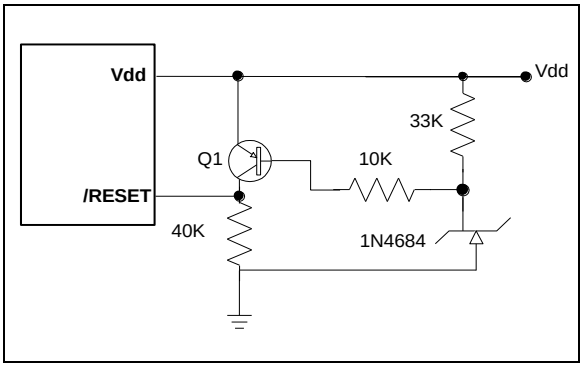


Figure 6-10 Circuit 1 for the Residue Voltage Protection

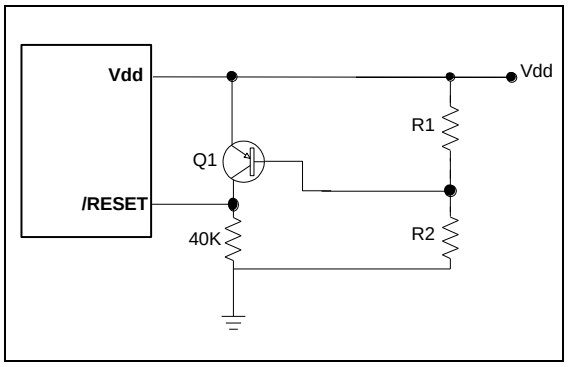


Figure 6-11 Circuit 2 for the Residue Voltage Protection

6.12 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

A) "JMP", "CALL", "RET", "RETL", "RETI" commands are executed with one instruction cycle. The conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the Instruction Set also has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table:

The following symbols are used in the following table:

"**R**" *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

"**b**" *Bit field designator that selects the value for the bit located in the Register "**R**" and which affects the operation.*

"**K**" *8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
MOV R,A	A → R	None
CLRA	0 → A	Z
TBWR	Table write start instruction	None
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z

(Continuation)

Mnemonic	Operation	Status Affected
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None[1]
BS R,b	1 → R(b)	None[2]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
ADD A,k	k+A → A	Z, C, DC
LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC4	None
LJMP k	Next instruction : k kkkk kkkk kkkk k→PC4	None
TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None
SBANK k	k → R1(6:4)	None
GBANK k	k → R1(2:0), k(1:0) → R4(7:6)	None

[1] *This instruction is not recommended for interrupt status register operation.*

[2] *This instruction cannot operate under interrupt status register.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.5V	to	3.6V
Working Frequency	DC	to	8 MHz

8 DC Electrical Characteristics

(Ta=25°C, VDD=3.3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 3.3V	8MHz,1 MHz, 500kHz,	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	µA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7	0.56Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7	-0.3V	-	0.44Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.56Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.44Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	INT	0.56Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	INT	-0.3V	-	0.44Vdd	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = 0.9VDD	-2.5			mA
IOL1	Output Low Voltage (Ports 5, 6, 7)	VOL = 0.1VDD	6.5			mA
IOH2	Output High Voltage(High drive) (P60~P63,P65)	VOH = 0.7VDD	-12			mA
IOL2	Output Low Voltage(High sink) (P60~P63,P65)	VOL = 0.3VDD	31			mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IPH	Pull-high current (15KΩ) (Ports 5, 6, 7)	Pull-high active, input pin at VSS		-220		μA
IPL	Pull-low current (220Kohm)(Port6)	Pull-low active, input pin at Vdd		15		μA
IPL2	Pull-low current (10Kohm) (Port5,7)	Pull-low active, input pin at Vdd		330		μA
ICC1	Operating supply current (Normal mode)	/RESET= 'High', Fm=1MHz (IRC type), Fs on, output pin floating, WDT enabled	-	160	-	μA
ICC2	Operating supply current (Normal mode)	/RESET= 'High', Fm=8MHz (IRC type), Fs on, output pin floating, WDT enabled	-	562.5	-	μA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm=500kHz (IRC type), Fs on, output pin floating, WDT enabled		120		μA
ICC4	Operating supply current (Green mode)	/RESET= 'High', Low Power, Fm=1MHz (IRC type), Fs =128kHz PERCS=0, Output pin floating, WDT enabled			20	μA
ICC5	Operating supply current (idle mode)	/RESET= 'High', Low Power, Fm=1MHz (IRC type), Fs=128kHz, PERCS=0, Output pin floating, WDT enabled			3	μA
ISB1		/RESET= 'High', Fm & Fs off, All input and I/O pins at VDD, output pin floating, WDT disabled			0.8	μA
ISB2		/RESET= 'High', Fm & Fs off, All input and I/O pins at VDD, output pin floating, WDT Enabled			2.5	μA

Note: *These parameters are theoretical values and have not been tested nor verified.*

Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C. These data are for design reference only and have not been tested.

8.1 Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Twrite	Page/byte Write	Vdd = 2.5V~ 3.6V Temperature =-40°C~85°C	-	2	3	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

8.2 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Page program time	Vdd = 2.5V~ 3.6V Temperature = -40°C ~ 85°C	-	1	1.5	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9 AC Electrical Characteristics

■ **-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	RC type	2000	–	DC	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

******N*: *Selected pre-scaler ratio*

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F724NAMS10	MSOP	10	118 mil

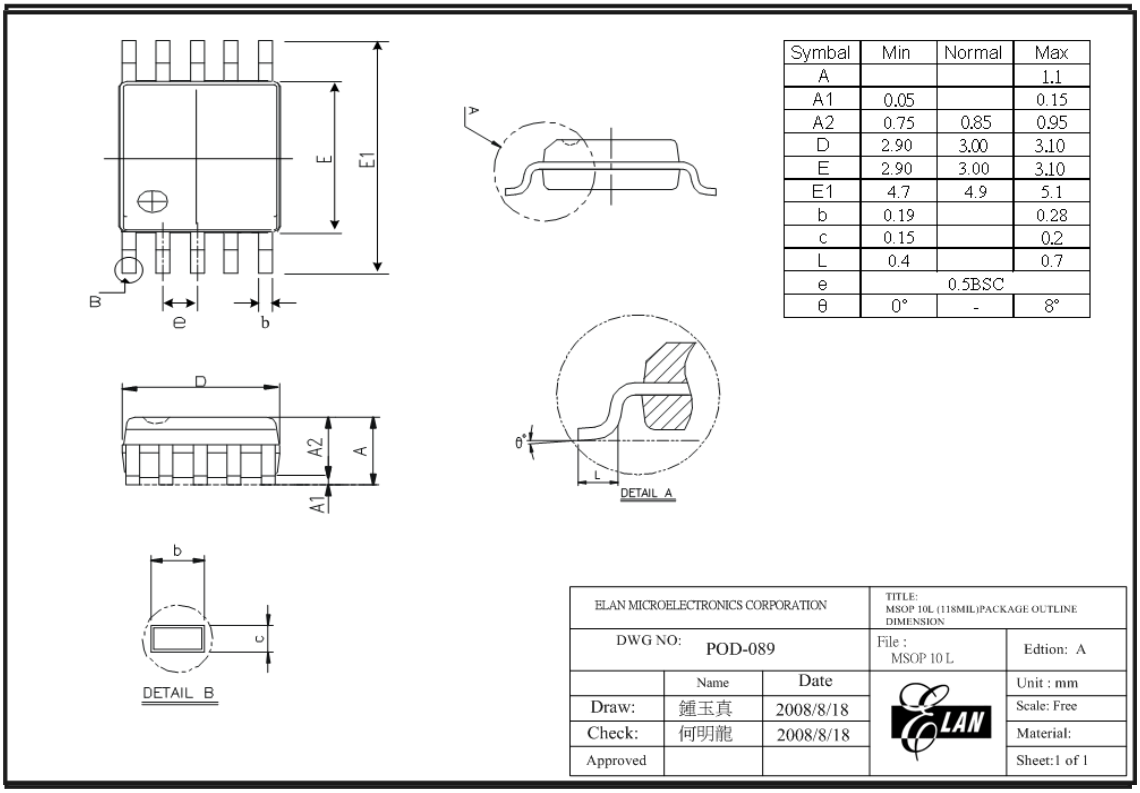
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents should be less than 100ppm and complies with Sony specifications.

Part No.	EM78F724N
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 EM78F724NAMS10 118mil



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e		0.5BSC	
θ	0°	-	8°

ELAN MICROELECTRONICS CORPORATION			TITLE: MSOP 10L (118MIL)PACKAGE OUTLINE DIMENSION	
DWG NO: POD-089			File : MSOP 10 L	Edtion: A
	Name	Date		Unit : mm
Draw:	鍾玉真	2008/8/18		Scale: Free
Check:	何明龍	2008/8/18		Material:
Approved				Sheet:1 of 1

Figure B-1 EM78F724N 10-Pin MSOP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.