# EM88F752N

## 8-BIT
## Microcontroller

# Product
# Specification

**DOC. VERSION 1.1**

**ELAN MICROELECTRONICS CORP.**

December 2015

## ELAN  MICROELECTRONICS  CORPORATION

# Contents

# APPENDIX

## Specification Revision History

| Version | Revision Description | Date |
|---------|---------------------|------|
| 1.0 | Released version | 2015/10/30 |
| 1.1 | 1. Added a Note on the application<br><br>2. Added Figure 6-40<br><br>3. Modified the Bit Name of TPEPCR1, TPEPCR2 registers<br><br>4. Modified the description of the switch bits<br><br>5. Modified the description of TPAEP<br><br>6. Modified the Absolute Maximum Ratings<br><br>7. Modified the DC and AC Electrical Characteristics<br><br>8. Modified the Package Name<br><br>9. Modified the Name of the Registers<br><br>10. Modified the Oscillation Characteristics<br><br>11. Modified Table E-1<br><br>12. Modified Table Figure 6-3<br><br>13. Modified the description of IRC Oscillator Modes<br><br>14. Modified the description of Instruction Set<br><br>15. Deleted Figure 6-12 | 2015/12/11 |

# 1   General Description

EM88F752N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It has an on-chip 2K*16-bits electrical flash memory.

Debug function is built in EM88F752N chip. User can read the program code from JTAG port and monitor the on chip register status, memory and program trace log on computer.

EM88F752N includes a capacitive touch-sensitive function. The capacitive touch key, a self-contained, is covered with a plastic or glass case. The system controller converts finger data to button presses, depending on finger location and human interface context.

Using OCDS, user can develop their program for several flash types IC of ELAN

# 2 Features

- CPU configuration
  - **2K×16** bits Flash memory
  - (48+256) bytes general purpose register
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 1 mA at 5V/4MHz
  - Typically 15 μA, at 3V/16kHz
  - Typically 22 μA, at 3V/32kHz
  - Typically 1 μA, during sleep mode
  - 3 programmable Level Volt Reset
    LVR: 4.0V, 3.5V, 2.7V, 1.8V (POR)
  - 1 set of 4 programmable Level Voltage Detector
    LVD: 4.5V, 4.0V, 3.3V, 2.2V
  - Six CPU operation modes (Normal, Green, Idle, Sleep, TK-Idle TK-Sleep)
- I/O port configuration
  - 6 bidirectional I/O ports: P5, P6, P8
  - 4 programmable pin change wake-up ports : P5, P6, P8
  - 6 programmable pull-down I/O ports: P5, P6, P8
  - 6 programmable pull-high I/O ports: P5, P6, P8
  - 6 programmable open-drain I/O ports: P5, P6, P8
  - 6 programmable high-sink/drive I/O ports: P5, P6, P8
- Operating voltage range:
  - 2.4V~5.5V at -40°C~85°C (industrial)
  - 2.1V~5.5V at 0°C~70°C (commercial)
- Operating frequency range (base on two clocks):
  **Main oscillator:**
  - Crystal mode:
    DC ~ 20 MHz at 4.5V~5.5V
    DC ~ 16 MHz at 3.5V~5.5V
    DC ~ 8 MHz at 2.1V~5.5V
  - IRC mode:
    DC ~ 20 MHz at 4.5V~5.5V
    DC ~ 16 MHz at 3.5V~5.5V
    DC ~ 8 MHz at 2.1V~5.5V

| InternalRC Frequency | TouchKey Frequency | Drift Rate | | | |
|---|---|---|---|---|---|
| | | Temp. (-40~+85℃) | Voltage (2.1~5.5V) | Process | Total |
| 1 MHz | 24 MHz | ±2% | ±1% | ±1% | ±4% |
| 4 MHz | 24 MHz | ±2% | ±1% | ±1% | ±4% |
| 6 MHz | 24 MHz | ±2% | ±1% | ±1% | ±4% |
| 8 MHz | 24 MHz | ±2% | ±1% | ±1% | ±4% |
| 12 MHz | 24 MHz | ±2% | ±1% | ±1% | ±4% |
| 16 MHz | 16 MHz | ±2% | ±1% | ±1% | ±4% |
| 20 MHz | 20 MHz | ±2% | ±1% | ±1% | ±4% |

\* Kernel and TK used the same IRC clock source

**Sub oscillator:**
- IRC mode: 16k/128kHz
- Crystal Mode : 32.768kHz

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Two Pulse Width Modulation (PWMA, PWMB) with 10-bit resolution shared with Timers A and B
  - Three 8-bit timers (TC1/TC2/TC3) with seven modes: Timer/Counter/Capture/Window/Buzzer/PWM/ PDO (Programmable Divider Output) modes. Timers 1 and 2 can be cascaded to one 16-bit counter/timer TC1+TC2 can be cascaded to one 16-bit counter/timer
  - 8+1 channels Analog-to-Digital Converter with 12-bit resolution
    One of the channels is 1/2 VDD power detection
  - Touch key function 10 traces(Sensor) for 1 groups, operating voltage range from 2.4V to 5.5V
  - I$^2$C function with 7/10 bits address and 8 bits data transmit/receive mode
  - Power down (Sleep) mode
- 21 available interrupts: (3 external, 17 internal)
  - Watch timer interrupt
  - External interrupt: EINT0,EINT1
  - TCC overflow interrupt
  - TC1, TC2, TC3 overflow interrupt
  - Input-port status changed interrupt
  - ADC completion interrupt
  - PWMA, PWMB period/duty match completion
  - I$^2$C transfer/receive/stop interrupt
  - LVD interrupt
  - System hold interrupt
  - Touch key conversion finish, limit check, error interrupt
- Single instruction cycle commands
- Five kinds of oscillation range in Crystal Mode

| Crystal Range | Oscillator Mode |
|---|---|
| 20 MHz ~ 12 MHz | HXT1 |
| 12 MHz ~ 6 MHz | HXT2 |
| 6 MHz ~ 1 MHz | XT |
| 1 MHz ~ 100 kHz | LXT1 |
| 32.768kHz | LXT2 |

- Programmable free running watchdog timer
  - Watchdog Timer: 16.5ms ± 5% with VDD =5V at 25°C, Temperature range ± 5% (-40°C ~+85°C)
  - Watchdog Timer: 16.5ms ± 5% with VDD = 3V at 25°C, Temperature range ± 5% (-40°C~+85°C)
  - Two clocks per instruction cycle
- Package Type:
  - 20-pin SOP     :     300mil     EM88F752NSO20UJ
  - 20-pin DIP     :     300mil     EM88F752ND20UJ
  - 20-pin SSOP     :     209mil     EM88F752NSS20UJ
  - 16-pin DIP     :     300mil     EM88F752ND16UJ
  - 16-pin SSOP     :     150mil     EM88F752NSS16UJ
  - 16-pin SOP     :     150mil     EM88F752NSO16UJ
  - 16-pin DIP     :     300mil     EM88F752NAD16UJ
  - 16-pin SSOP     :     150mil     EM88F752NASS16UJ
  - 16-pin SOP     :     150mil     EM88F752NASO16UJ

**Note:** *These are all Green products which do not contain hazardous substances.*

## 2.1 Selection Table

| Features | | EM88F752N | EM88F752N | EM88F752NA |
|---|---|---|---|---|
| Package Type | | SSOP-20<br>SOP-20<br>DIP-20 | SSOP-16<br>SOP-16<br>DIP-16 | SSOP-16<br>SOP-16<br>DIP-16 |
| Operation Voltage (V) | | 2.1~5.5[2] | 2.1~5.5[2] | 2.1~5.5[2] |
| Operating Speed | Oscillator Speed (MHz) | 20 | 20 | 20 |
| | Instruction cycle (ns) | 100 | 100 | 100 |
| On-chip Flash (16-bit Word) | | 2K | 2K | 2K |
| On-chip SRAM (8-bit Byte) | | 304 | 304 | 304 |
| Watchdog Timer | | Yes | Yes | Yes |
| RTC (Watch Time) | | Yes | Yes | Yes |
| PWM Output | Resolution | 10 | 10 | 10 |
| | PWM Timer | 2 | 1 | 2 |
| | PWM Output | 4 | 1 | 2 |
| | Complement | Yes | No | No |
| | Dead-time | Yes | No | No |
| 12-bit ADC | kSPS | 100 | 100 | 100 |
| | Power Detection | ½ VDD | ½ VDD | ½ VDD |
| | Channels | 8 | 7 | 8 |
| | Sample-and-Hold | 1 | 1 | 1 |
| TCC | | 8 bits[*1] | 8 bits[*1] | 8 bits[*1] |
| TC1 | Timer/Counter/Capture Window /PWM/PDO | 8 bits[*1] | 8 bits[*1] | 8 bits[*1] |
| TC2 | | 8 bits[*1] | 8 bits[*1] | 8 bits[*1] |
| TC3 | | 8 bits[*1] | 8 bits[*1] | 8 bits[*1] |
| TP | | 10 Traces | 7 Traces | 9 Traces |
| External Interrupts | | 2 | 2 | 2 |
| Inter-integrated circuit (I2C) | | 1 | 1 | 1 |
| I/O Pins (Shared) | GPIO | 18 | 14 | 14 |
| | Direct LED Driver Pin | 18 | 14 | 14 |
| | Direct LED Driver Current (Typ.) | 90mA[1] | 90mA[1] | 90mA[1] |
| Temp. | -40°C ~ 85°C | Yes[2] | Yes[2] | Yes[2] |

[1] Hi-sink current enable and output is GND +1.5V

[2] Operating voltage: 2.4V~5.5V at -40°C ~85°C (Industrial)
2.1V~5.5V at 0°C~70°C (commercial)

*Table 2-1   EM88F752N Selection Table*

# 3   Pin Configuration



| | | | | |
|---|---|---|---|---|
| VSS | 1 | | 20 | VDD |
| OSCI/RCOUT/P80 | 2 | | 19 | P50/ADC0/INT0/TPS10 |
| OSCO/P81 | 3 | | 18 | P51/ADC1/INT1/TPS9 |
| SCL0/RESET/P82 | 4 | | 17 | P52/ADC2/TCC/TPS8 |
| XIN/SCL1/TC2/P83 | 5 | **EM88F752N** | 16 | P53/ADC3/TPS7 |
| XOUT/SDA1/TC1/P84 | 6 | **SOP/SSOP/DIP-20** | 15 | P54/ADC4/TPS6 |
| 2W_SCL/P64 | 7 | | 14 | P55/ADC5/TPS5 |
| 2W_SDA/P63 | 8 | | 13 | P56/PWMA/ADC6/TPS4 |
| SDA0//PWMB/P62 | 9 | | 12 | P57/PWMB/ADC7/TPS3 |
| TPS1//PWMA/P61 | 10 | | 11 | P60/TC3/VREF/TPS2 |
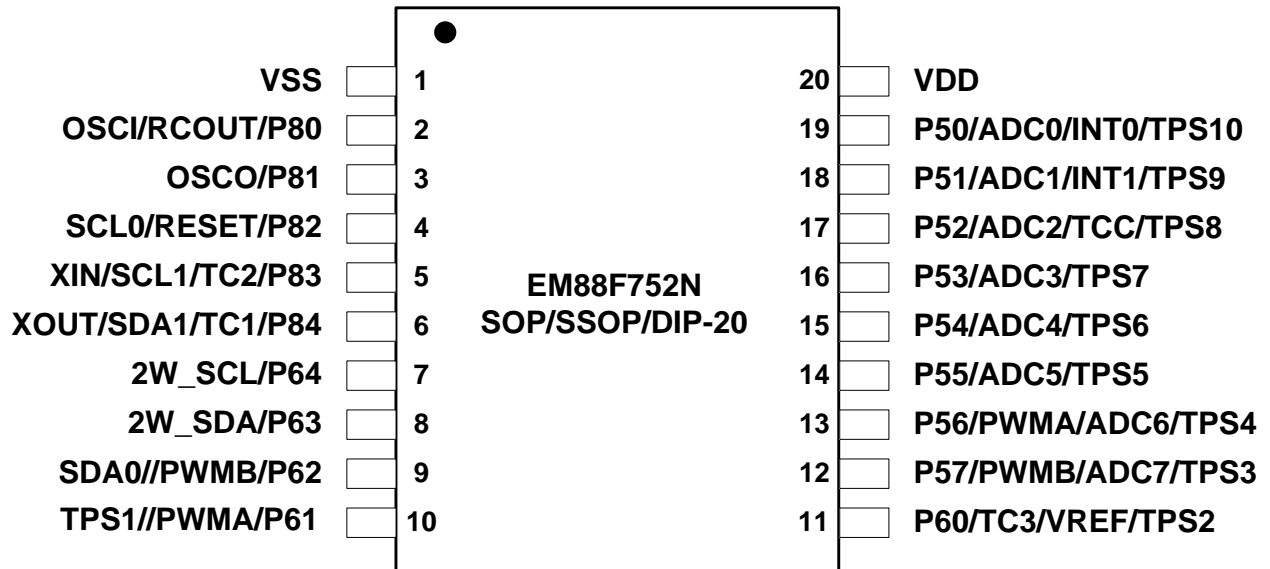
*Figure 3-1   EM88F752N SOP/SSOP/DIP-20 Pin Assignment*
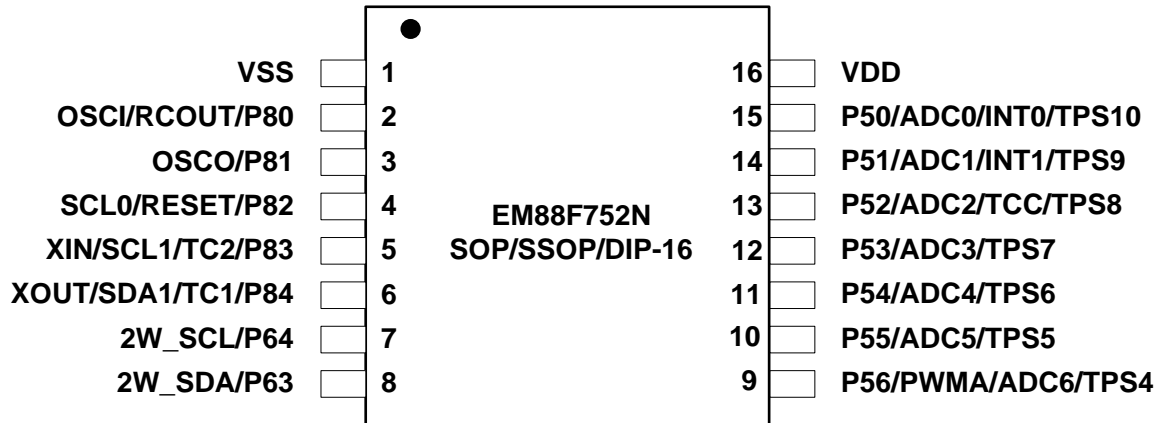
*Figure 3-2   EM88F752N SOP/SSOP/DIP-16 Pin Assignment*
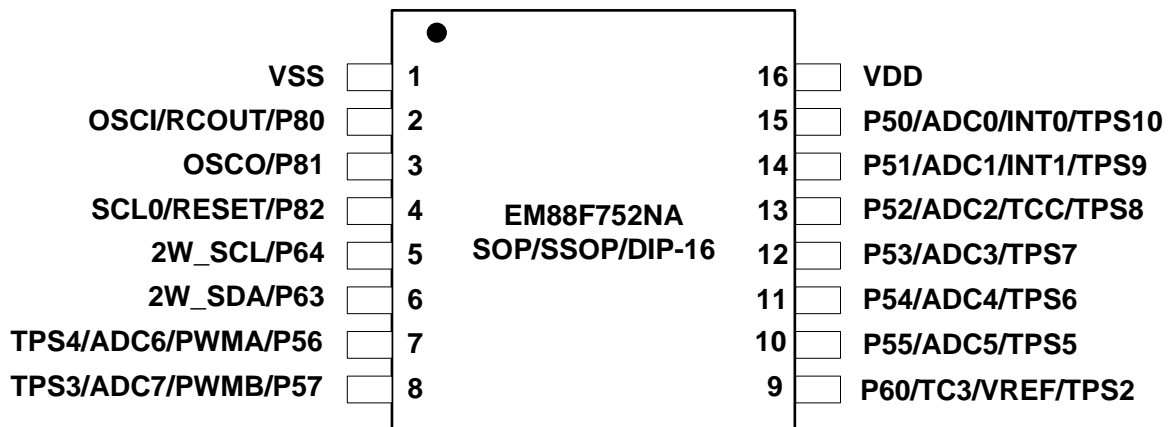


*Figure 3-3   EM88F752NA SOP/SSOP/DIP-16 Pin Assignment*

# 4 Pin Description

| Name | Function | Input Type | Output Type | Description |
|------|----------|------------|-------------|-------------|
| VDD | VDD | Power | − | Power |
| VSS | VSS | Power | − | Ground |
| P50/ADC0/INT0/TPS10 | P50 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | ADC0 | AN | − | ADC Input 0 |
| | INT0 | ST | − | External Interrupt 0 |
| | TPS10 | AN | − | TPS10 is a Touch Pad sense pin |
| P51/ADC1/INT1/TPS9 | P51 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | ADC1 | AN | − | ADC Input 1 |
| | INT1 | ST | − | External Interrupt 1 |
| | TPS9 | AN | − | TPS9 is a Touch Pad sense pin |
| P52/ADC2/TCC/TPS8 | P52 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | ADC2 | AN | − | ADC Input 2 |
| | TCC | ST | − | Real Time Clock/Counter clock input |
| | TPS8 | AN | − | TPS8 is Touch Pad sense pin |
| P53/ADC3/TPS7 | P53 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | ADC3 | AN | − | ADC Input 3 |
| | TPS7 | AN | − | TPS7 is a Touch Key sense pin |
| P54/ADC4/TPS6 | P54 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wakeup |
| | ADC4 | AN | − | ADC Input 4 |
| | TPS6 | AN | − | TPS6 is Touch Pad sense pin |
| P55/ADC5/TPS5 | P55 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | ADC5 | AN | − | ADC Input 5 |
| | TPS5 | AN | − | TPS5 is a Touch Pad sense pin |
| P56/PWMA/ADC6/TPS4 | P56 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | PWMA | − | CMOS | PWMA output |
| | ADC6 | AN | − | ADC Input 6 |
| | TPS4 | AN | − | TPS4 is a Touch Pad sense pin |

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| P57/PWMB/ADC7/ TPS3 | P57 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | PWMB | – | CMOS | PWMB output |
| | ADC7 | AN | – | ADC Input 7 |
| | TPS3 | AN | – | TPS3 is a Touch Pad sense pin |
| P60/TC3/VREF/ TPS2 | P60 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | TC3 | ST | CMOS | 8-bit Timer/Counter 3 |
| | VREF | AN | – | Voltage reference for ADC |
| | TPS2 | AN | – | TPS2 is a Touch Pad sense pin |
| P61/ /PWMA/TPS1 | P61 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | /PWMA | – | CMOS | /PWMA output |
| | TPS1 | AN | – | TPS1 is a Touch Pad sense pin |
| P62/SDA0/ /PWMB | P62 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | SDA0 | ST | CMOS | $I^2C$ serial data line. It is open-drain |
| | /PWMB | – | CMOS | /PWMB output |
| P63/2W_SDA | P63 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | 2W_SDA | ST | CMOS | On-chip Debug System data pin |
| P64/2W_SCL | P64 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up |
| | 2W_SCL | ST | CMOS | On-chip Debug System clock pin |
| P80/RCOUT/OSCI | P80 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain |
| | RCOUT | – | CMOS | Clock output of external RC oscillator (Open-drain) |
| | OSCI | XTAL | – | Clock input of crystal/resonator oscillator |
| P81/OSCO | P81 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain |
| | OSCO | – | XTAL | Clock output of crystal/resonator oscillator |

| Name | Function | Input Type | Output Type | Description |
|------|----------|------------|-------------|-------------|
| P82/RESET/SCL0 | P82 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain |
| | RESET | ST | − | |
| | SCL0 | ST | CMOS | $I^2C$ serial clock line. It is open-drain |
| P83/TC2/SCL1/XIN | P83 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain |
| | TC2 | ST | CMOS | 8-bit Timer/Counter 2 |
| | SCL1 | ST | CMOS | $I^2C$ serial clock line. It is open-drain |
| | XIN | XTAL | − | Clock input of crystal/resonator oscillator |
| P84/TC1/SDA1/XOUT | P84 | ST | CMOS | Bidirectional I/O pin with programmable pull-down, pull-high, open-drain |
| | TC1 | ST | CMOS | 8-bit Timer/Counter 1 |
| | SDA1 | ST | CMOS | $I^2C$ serial data line. It is open-drain |
| | XOUT | − | XTAL | Clock output of crystal/resonator oscillator |

# 5   Functional Block Diagram
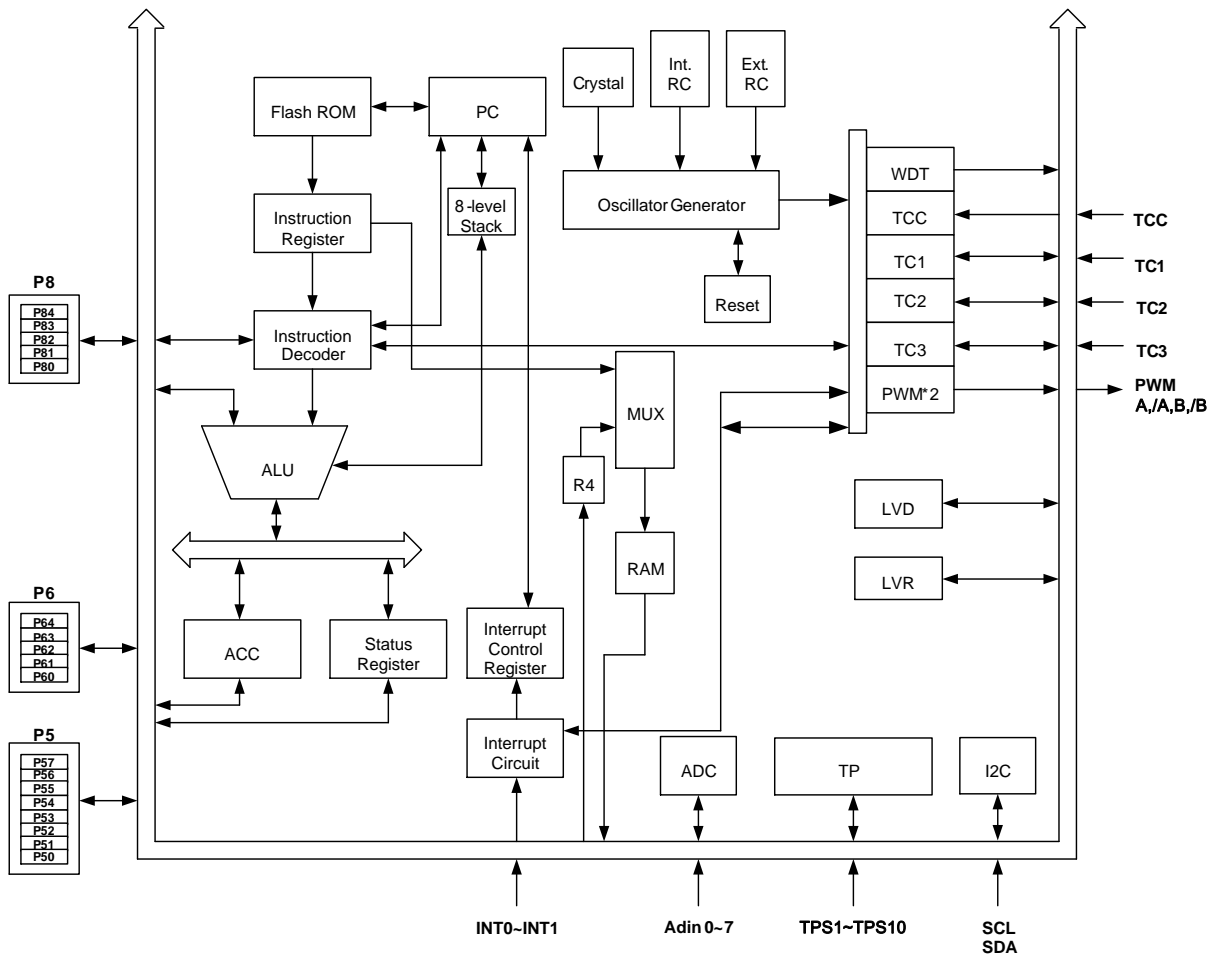


*Figure 5-1   Function Block Diagram*

# 6 Function Description

## 6.1 Operational Registers

### 6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

### 6.1.2 R1: BSR (Bank Selection Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | SBS1 | SBS0 | - | - | GBS1 | GBS0 |
| 0 | 0 | R/W | R/W | 0 | 0 | R/W | R/W |

**Bits 7~6:** Not used, set to "0" all the time.

**Bits 5~4 (SBS1~SBS0):** special register bank select bit. It is used to select Bank 0/1/2 of special register **R5~R4F**.

| SBS1 | SBS0 | Special Register Bank |
|------|------|----------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | x |

**Bits 3~2:** Not used, set to "0" all the time.

**Bits 2~0 (GBS1~GBS0):** general register bank select bit. It is used to select Bank 0~3 of general register R80~RFF.

| GBS0 | RAM Bank |
|------|----------|
| 0 | 0 |
| 1 | 1 |

### 6.1.3 R2: PCL (Program Counter Low)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (PC7~PC0):** The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 15-bit wide. The structure is depicted in Figure 6-1.

- Generating 2K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.

- R2 is set as all "0"s when under RESET condition.

- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 8K ($2^{13}$).

- "LCALL" instruction loads the lower 13 bits of the PC, and then PC+1 is pushed into the stack.  Thus, the subroutine entry address can be located anywhere within 8K ($2^{13}$).

- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.

- Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6","INC R2",·····) will cause the ninth bit and the above bits (PC8~PC12) of the PC not change.

- All instructions are single instruction cycle (Fsys/2) except "LCALL", "CALL", "LJMP" and "JMP" instructions. The "LCALL" and "LJMP" instructions need two instructions cycles.
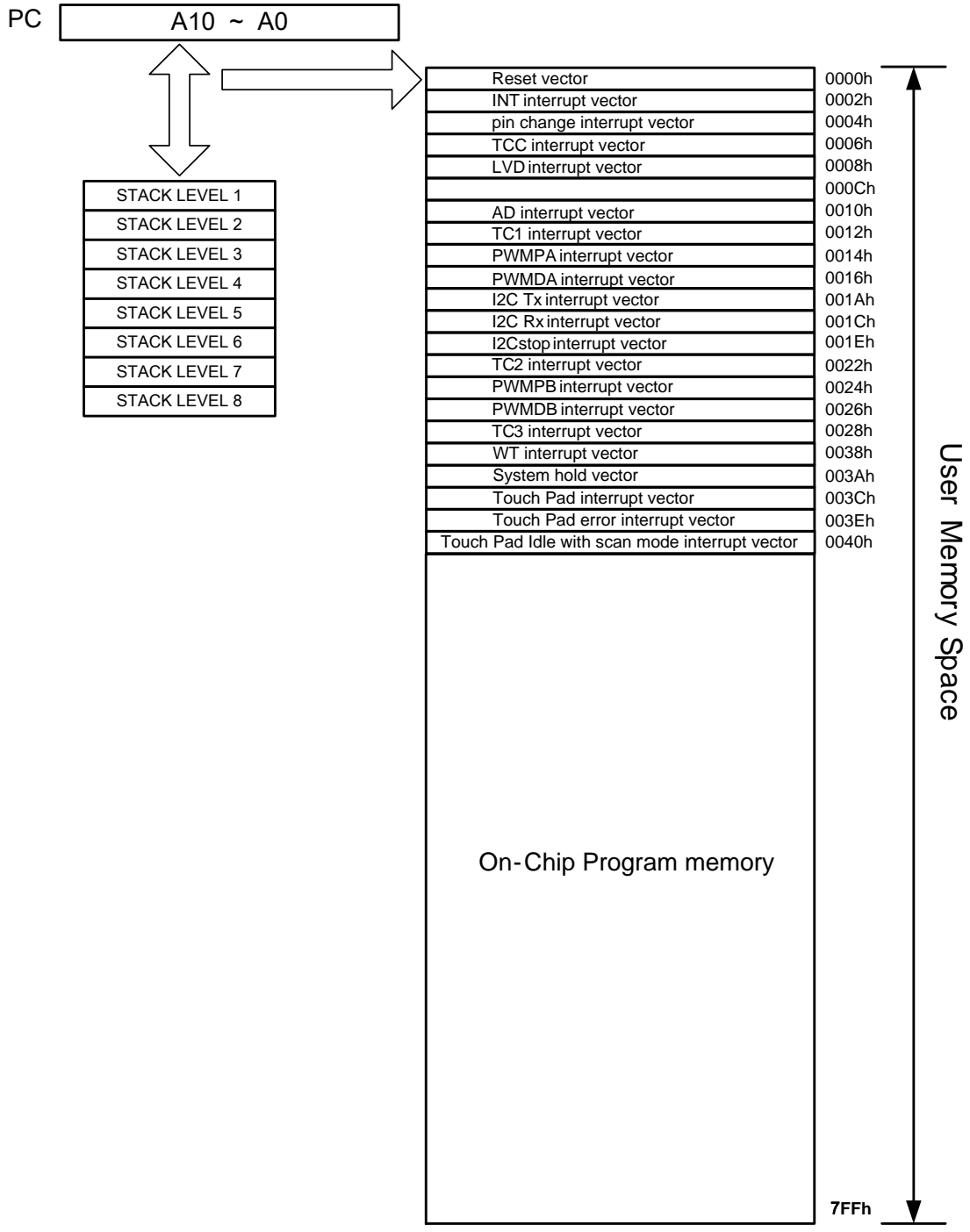
*Figure 6-1   Program Counter Organization*

| Address | Bank 0 | Bank 1 | Bank 2 |
|---------|--------|--------|--------|
| 0X00 | IAR (Indirect Addressing Register) | | |
| 0X01 | BSR (Bank Selection Control Register) | | |
| 0X02 | PCL (Program Counter Low) | | |
| 0X03 | SR (Status Register) | | |
| 0X04 | RSR (RAM Selection Reg.) | | |
| 0X05 | Port 5 | IOCR8 | TPEPCR1 |
| 0X06 | Port 6 | Reserved | TPEPCR2 |
| 0X07 | Reserved | Reserved | Reserved |
| 0X08 | Port 8 | P5PHCR | Reserved |
| 0X09 | Reserved | P6PHCR | TPCCR |
| 0X0A | Reserved | P8PHCR | TPCR1 |
| 0x0B | IOCR5 | P5PLCR | TPCR2 |
| 0X0C | IOCR6 | P6PLCR | TPCR3 |
| 0X0D | Reserved | P8PLCR | TPAHTH |
| 0X0E | OMCR (Operating Mode Control Reg.) | P5HDSCR | TPAHTL |
| 0X0F | EIESCR (External Interrupt Edge Select Control Reg.) | P6HDSCR | TPALTH |
| 0X10 | WUCR1 | P8HDSCR | TPALTL |
| 0X11 | WUCR2 | P5ODCR | Reserved |
| 0X12 | WUCR3 | P6ODCR | Reserved |
| 0X13 | Reserved | P8ODCR | Reserved |
| 0X14 | SFR1 (Status Flag Register 1) | DeadTCR | Reserved |
| 0X15 | SFR2 (Status Flag Register 2) | DeadTR | TPAH |
| 0X16 | SFR3 (Status Flag Register 3) | PWMSCR | TPAL |
| 0X17 | SFR4 (Status Flag Register 4) | PWMACR | Reserved |
| 0X18 | Reserved | PRDAL | Reserved |
| 0X19 | SFR6 (Status Flag Register 6) | PRDAH | TPSTH |
| 0X1A | Reserved | DTAL | TPSTL |
| 0X1B | IMR1 (Interrupt Mask Register 1) | DTAH | Reserved |
| 0X1C | IMR2 (Interrupt Mask Register 2) | TMRAL | Reserved |
| 0X1D | IMR3 (Interrupt Mask Register 3) | TMRAH | Reserved |
| 0X1E | IMR4 (Interrupt Mask Register 4) | PWMBCR | Reserved |
| 0X1F | Reserved | PRDBL | Reserved |
| 0X20 | IMR6 (Interrupt Mask Register 6) | PRDBH | Reserved |
| 0X21 | WDTCR | DTBL | Reserved |
| 0X22 | TCCCR | DTBH | Reserved |

| Address | Bank 0 | Bank 1 | Bank 2 |
|---------|--------|--------|--------|
| 0X23 | TCCD | TMRBL | Reserved |
| 0X24 | TC1CR1 | TMRBH | Reserved |
| 0X25 | TC1CR2 | Reserved | Reserved |
| 0X26 | TC1DA | Reserved | Reserved |
| 0X27 | TC1DB | Reserved | Reserved |
| 0X28 | TC2CR1 | Reserved | Reserved |
| 0X29 | TC2CR2 | Reserved | Reserved |
| 0X2A | TC2DA | Reserved | Reserved |
| 0x2B | TC2DB | Reserved | Reserved |
| 0X2C | TC3CR1 | Reserved | Reserved |
| 0X2D | TC3CR2 | Reserved | Reserved |
| 0X2E | TC3DA | Reserved | Reserved |
| 0X2F | TC3DB | Reserved | Reserved |
| 0X30 | I2CCR1 | Reserved | Reserved |
| 0X31 | I2CCR2 | Reserved | Reserved |
| 0X32 | I2CSA | Reserved | Reserved |
| 0X33 | I2CDB | Reserved | Reserved |
| 0X34 | I2CDAL | Reserved | Reserved |
| 0X35 | I2CDAH | Reserved | Reserved |
| 0X36 | Reserved | Reserved | Reserved |
| 0X37 | Reserved | Reserved | Reserved |
| 0X38 | Reserved | Reserved | Reserved |
| 0X39 | Reserved | Reserved | Reserved |
| 0X3A | Reserved | Reserved | Reserved |
| 0x3B | Reserved | Reserved | Reserved |
| 0X3C | Reserved | Reserved | Reserved |
| 0X3D | Reserved | Reserved | Reserved |
| 0X3E | ADCR1 | Reserved | Reserved |
| 0X3F | Reserved | Reserved | Reserved |
| 0X40 | ADISR | EECR1 | Reserved |
| 0X41 | ADER1 | Reserved | Reserved |
| 0X42 | Reserved | Reserved | Reserved |
| 0X43 | ADDL | Reserved | Reserved |
| 0X44 | ADDH | FLKR | Reserved |
| 0X45 | ADCVL | TBPTL | Reserved |

| Address | Bank 0 | Bank 1 | Bank 2 |
|---------|--------|--------|--------|
| 0X46 | ADCVH | TBPTH | Reserved |
| 0X47 | Reserved | STKMON | LOCKPR |
| 0X48 | Reserved | PCH | LOCKCR |
| 0X49 | Reserved | LVDCR | Reserved |
| 0X4A | Reserved | Reserved | Reserved |
| 0x4B | Reserved | Reserved | Reserved |
| 0X4C | Reserved | Reserved | Reserved |
| 0X4D | Reserved | TBWCR | Reserved |
| 0X4E | Reserved | TBWAL | Reserved |
| 0X4F | Reserved | TBWAH | Reserved |
| 0X50 | | | |
| 0X51 | | | |
| . | | | |
| . | General Purpose Register | | |
| 0x7E | | | |
| 0X7F | | | |
| 0X80 | | | |
| 0X81 | | | |
| . | | | |
| . | Bank 0 | Bank 1 | |
| . | | | |
| 0XFE | | | |
| 0XFF | | | |

*Figure 6-2   Data Memory Configuration*

### 6.1.4  R3: SR (Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| INT | N | OV | T | P | Z | DC | C |
| F | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (INT):** Interrupt Enable flag

> 0: Interrupt masked by DISI or hardware interrupt

> 1: Interrupt enabled by ENI/RETI instructions

**Bit 6 (N):** Negative flag

The negative flag stores the state of the most significant bit of the output result

> 0: The result of the operation is not negative

> 1: The result of the operation is negative

**Bit 5 (OV):** Overflow flag.

OV is set when a two's complement overflow occurs as a result of an operation

> 0: No overflow occurred

> 1: Overflow occurred

**Bit 4 (T):** Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

**Bit 3 (P):** Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

**Bit 2 (Z):** Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

**Bit 1 (DC)**: Auxiliary carry flag

**Bit 0 (C):** Carry flag

C is set when a carry occurs and cleared when borrow occurs during an arithmetic operation. The Carry Flag bit is set or cleared, depending on the operation that is performed

For ADD, ADC, INC, INCA instruction

> 0: No carry occurs

> 1: Carry occurs

For SUB, SUBB, DEC, DECA, NEG instruction

> 0: Borrow occurs

> 1: No borrow occurs

For RLC, RRC, RLCA, RRCA instruction

The Carry flag is used as a link between the least significant bit (LSB) and most significant bit (MSB).

### 6.1.5 R4: RSR (RAM Select Register)

**Bits 7~0 (RSR7~RSR0):** used to select registers (Address: 00~FF) in the indirect address mode. Users can see the configuration of the data memory in more detail in Figure 6-2.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RSR7 | RSR6 | RSR5 | RSR4 | RSR3 | RSR2 | RSR1 | RSR0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

### 6.1.6 Bank 0 R5 ~ RA (Port 5 ~ Port A)

R5, R6, R7, R8, R9 and RA are I/O data registers.

### 6.1.7 Bank 0 RB IOCR5 (I/O Port 5 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

### 6.1.8 Bank 0 RC IOCR6 (I/O Port 6 Control Register)

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

### 6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CPUS | IDLE | - | - | - | RCM2 | RCM1 | RCM0 |
| R/W | R/W | 0 | 0 | 0 | R/W | R/W | R/W |

**Bit 7 (CPUS):** CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator (default)

When CPUS=0, the CPU oscillator select a sub-oscillator and the main oscillator is stopped.

**Bit 6 (IDLE):** Idle Mode Enable Bit. This bit will decide SLEP instruction which mode to
go.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode (default)
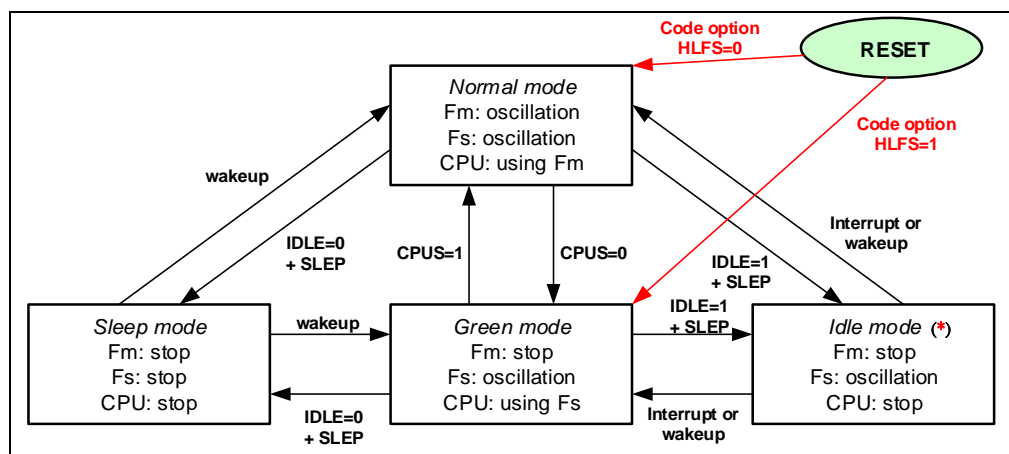


*Figure 6-3   CPU Operation Mode*

*Note*

(*) *Switching Operation Mode from Idle → Normal, Idle → Green*

*If the clock source of the timer is Fs, the timer/counter will continue to count in Idle mode.  When the matching
condition of the timer/counter occurs during Idle mode, the interrupt flag of the Timer/Counter will be active.  The
MCU will jump to the interrupt vector when the corresponding interrupt is enabled.*

## Oscillation Characteristics

### HLFS=0 (Normal)

| Fmain | Fsub | Power-on LVR | Pin-Reset / WDT | |
|---|---|---|---|---|
| | | | N / G / I | S |
| RC 1M, 4M 6M, 8M | RC | 16ms + WSTO + (8 or 32)*1/Fmain | WSTO + (8 or 32)*1/Fmain | WSTO + (8 or 32)*1/Fmain |
| | XT | 16ms + WSTO +510*1/Fsub | WSTO + (8 or 32)*1/Fmain | WSTO + 510*1/Fsub |
| RC 12M,16M, 20M | RC | 16ms + WSTO +32*1/Fmain | WSTO + 32*1/Fmain | WSTO + 32*1/Fmain |
| | XT | 16ms + WSTO + 510*1/Fsub | WSTO + 32*1/Fmain | WSTO + 510*1/Fsub |
| XT | RC | 16ms + WSTO +510*1/Fmain | WSTO + 510*1/Fmain | WSTO + 510*1/Fmain |
| | XT | 16ms + WSTO +510*1/Fsub | WSTO + 510*1/Fmain | WSTO + 510*1/Fsub |

### HLFS=1 (Green)

| Fmain | Fsub | Power-on LVR | Pin-Reset / WDT | |
|---|---|---|---|---|
| | | | N / G / I | S |
| RC 1M,4M, 6M, 8M | RC | 16ms + WSTO + 8 *1/Fsub | WSTO + 8*1/Fsub | WSTO + 8*1/Fsub |
| | XT | 16ms + WSTO + 510*1/Fsub | WSTO + 8*1/Fsub | WSTO + 510*1/Fsub |
| RC 12M,16M, 20M | RC | 16ms + WSTO + 8*1/Fsub | WSTO + 8*1/Fsub | WSTO + 8*1/Fsub |
| | XT | 16ms + WSTO + 510*1/Fsub | WSTO + 8*1/Fsub | WSTO + 510*1/Fsub |
| XT | RC | 16ms + WSTO + 8*1/Fsub | WSTO + 8*1/Fsub | WSTO + 8*1/Fsub |
| | XT | 16ms + WSTO + 510*1/Fsub | WSTO + 8*1/Fsub | WSTO + 510*1/Fsub |

| Fmain | Fsub | G → N | I → N | S → N |
|---|---|---|---|---|
| RC 1M, 4M 6M, 8M | RC | WSTO + (8 or 32)*1/Fmain | WSTO + (8 or 32)*1/Fmain | WSTO + (8 or 32)*1/Fmain |
| | XT | WSTO + (8 or 32)*1/Fmain | WSTO + (8 or 32)*1/Fmain | WSTO + 510*1/Fsub |
| RC 12M,16M, 20M | RC | WSTO + 32*1/Fmain | WSTO + 32*1/Fmain | WSTO + 32*1/Fmain |
| | XT | WSTO + 32*1/Fmain | WSTO + 32*1/Fmain | WSTO + 510*1/Fsub |
| XT | RC | WSTO + 510*1/Fmain | WSTO + 510*1/Fmain | WSTO + 510*1/Fmain |
| | XT | WSTO + 510*1/Fmain | WSTO + 510*1/Fmain | WSTO + 510*1/Fsub |

| Fmain | Fsub | I → G | S → G |
|---|---|---|---|
| RC XT | RC | WSTO + 8*1/Fsub | WSTO + 8*1/Fsub |
| | XT | WSTO + 8*1/Fsub | WSTO + 510*1/Fsub |

*N: Normal mode*          *WSTO: Waiting Time from Start-to-Oscillation*

*G: Green mode*           *I: Idle mode*          *S: Sleep mode*

**Bits 5~3:** Not used, set to "0" all the time

**Bits 2~0 (RCM2~RCM0):** Internal RC mode selection bits

| RCM2 | RCM1 | RCM0 | Frequency (MHz) |
|------|------|------|-----------------|
| 0 | 0 | 0 | 4 (Default) |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 12 |
| 1 | 0 | 1 | 16 |
| 1 | 1 | 0 | 20 |
| 1 | 1 | 1 | NA |

### 6.1.10   Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | EIES1 | EIES0 | - | - |
| 0 | 0 | 0 | 0 | R/W | R/W | 0 | 0 |

**Bits 7~4:** Not used, set to "0" all the time

**Bit 3 (EIES1):** external interrupt edge select bit

> 0: Falling edge interrupt

> 1: Rising edge interrupt

**Bit 2 (EIES0):** external interrupt edge select bit

> 0: Falling edge interrupt

> 1: Rising edge interrupt

**Bits 1~0:** Not used, set to "0" all the time

### 6.1.11   Bank 0 R10: WUCR1 (Wake-up Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | LVDWK | ADWK | INT1WK | INT0WK | - | - |
| 0 | 0 | R/W | R/W | R/W | R/W | 0 | 0 |

**Bits 7~6:** Not used, set to "0" all the time

**Bit 5 (LVDWK):** Low Voltage Detect Wake-up Enable Bit

> 0: Disable Low Voltage Detect wake-up

> 1: Enable Low Voltage Detect wake-up

**Bit 4 (ADWK):** A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter interrupt vector or to wake-up IC from sleep/idle with AD conversion running, the ADWK bit must be set to "enable".

**Bit 3 (INT1WK):** External Interrupt (INT1 pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

**Bit 2 (INT0WK):** External Interrupt (INT0 pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter interrupt vector or to wake-up IC from sleep/idle, the INTWK bits must be set to "enable".

**Bits 1~0:** Not used, set to "0" all the time

### 6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | I2CWK | - | - |
| 0 | 0 | 0 | 0 | 0 | R/W | 0 | 0 |

**Bits 7~3:** Not used, set to "0" all the time.

**Bit 2 (I2CWK):** I2C wake-up enable bit. It's available when I2C works at slave mode.

0: Disable

1: Enable

*I2C slave mode cannot transmit at IC Green mode, or else SCL held and kept at low level. SCL is released when IC switches to Normal mode.

**Bits 1~0:** Not used, set to "0" all the time

### 6.1.13   Bank 0 R12: WUCR3 (Wake-up Control Register 3)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ICWKP8 | - | ICWKP6 | ICWKP5 | - | - | - | - |
| R/W | 0 | R/W | R/W | 0 | 0 | 0 | 0 |

**Bits 7~4 (ICWKP8~ICWKP5):** pin change wake up enable for Ports 8/6/5.

0: Disable wake up function

1: Enable wake up function

**Bits 3~0:** Not used, set to "0" all the time

| Wake-up Signal | Condition Signal | Sleep Mode | | Idle Mode | | Green Mode | | Normal Mode | |
|---|---|---|---|---|---|---|---|---|---|
| | | DISI | ENI | DISI | ENI | DISI | ENI | DISI | ENI |
| Pin Change INT | ICWKPx = 0, PxICIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | ICWKPx = 0, PxICIE = 1 | Wake-up is invalid | | | | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| | ICWKPx = 1, PxICIE = 0 | Wake up + Next Instruction | | | | Interrupt is invalid | | | |
| | ICWKPx = 1, PxICIE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |

**\***: When the MCU wakes up from sleep or idle mode, the PxICSF must be equal to 1. If ICSF is equal to 0, it means the pin status doesn't change or the pin change ICIE is disabled, hence the MCU cannot be awakened.

**\*\***: Px = Ports 8/6/5

### 6.1.14   Bank 0 R13: (Reserved)

### 6.1.15   Bank 0 R14: SFR1 (Status Flag Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | LVDSF | ADSF | EXSF1 | EXSF0 | WTSF | TCSF |
| 0 | 0 | F | F | F | F | F | F |

Each corresponding status flag is set to "1" when interrupt condition is triggered.

**Bits 7~6:** Not used, set to "0" all the time

**Bit 5 (LVDSF):** Low Voltage Detector status flag.

| LVDEN | LVDS1, LVDS0 | LVD Voltage Interrupt Level | LVDSF |
|-------|--------------|-----------------------------|-------|
| 1 | 11 | 2.2V | 1* |
| 1 | 10 | 3.3V | 1* |
| 1 | 01 | 4.0V | 1* |
| 1 | 00 | 4.5V | 1* |
| 0 | xx | NA | 0 |

**\*** If VDD has crossover at the LVD voltage interrupt level as VDD varies, LVDSF =1.

**Bit 4 (ADSF):** Status flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

**Bit 3 (EXSF1):** External Interrupt 1 Status flag.

**Bit 2 (EXSF0):** External Interrupt 0 Status flag.

**Bit 1 (WTSF):** Watch timer status flag.

**Bit 0 (TCSF):** TCC overflow status flag. Set when TCC overflows, reset by software.

---

**NOTE**
*If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.*

---

### 6.1.16 Bank 0 R15: SFR2 (Status Flag Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | TC3SF | TC2SF | TC1SF |
| 0 | 0 | 0 | 0 | 0 | F | F | F |

Each corresponding status flag is set to "1" when interrupt condition is triggered.

**Bits 7~3:** Not used, set to "0" all the time

**Bit 2 (TC3SF):** 8-bit Timer/Counter 3 status flag, cleared by software

**Bit 1 (TC2SF)**: 8-bit Timer/Counter 2 status flag, cleared by software.

**Bit 0 (TC1SF):** 8/16-bit Timer/Counter 1 status flag, cleared by software.

### 6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | PWMBPSF | PWMBDSF | PWMAPSF | PWMADSF |
| 0 | 0 | 0 | 0 | F | F | F | F |

**Bits 7~4:** Not used, set to "0" all the time

**Bit 3 (PWMBPSF):** Status flag of period-matching for PWMB (Pulse Width Modulation). Set when a selected period is reached, reset by software.

**Bit 2 (PWMBDSF):** Status flag of duty-matching for PWMB (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

**Bit 1 (PWMAPSF):** Status flag of period-matching for PWMA (Pulse Width Modulation). Set when a selected period is reached, reset by software.

**Bit 0 (PWMADSF):** Status flag of duty-matching for PWMA (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

### 6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P8ICSF | - | P6ICSF | P5ICSF | - | I2CSTPSF | I2CRSF | I2CTSF |
| F | 0 | F | F | 0 | F | F | F |

**Bit 7 (P8ICSF):** Port 8 input status change status flag. Set when Port 8 input changes, reset by software.

**Bit 6:** Not used, set to "0" all the time.

**Bit 5 (P6ICSF):** Port 6 input status change status flag. Set when Port 6 input changes, reset by software.

**Bit 4 (P5ICSF):** Port 5 input status change status flag. Set when Port 5 input changes, reset by software.

**Bit 3:** Not used, set to "0" all the time.

**Bit 2 (I2CSTPSF):** I2C stop status flag. Set when I2C receive stop signal.

**Bit 1 (I2CRSF):** I2C receive status flag. Set when I2C receives 1 byte data and responds to ACK signal. Reset by firmware or I2C disable.

**Bit 0 (I2CTSF):** I2C transmit status flag. Set when I2C transmits 1 byte data and receives handshake signal (ACK or NACK). Reset by firmware or I2C disable

### 6.1.19 Bank 0 R18: (Reserved)

### 6.1.20   Bank 0 R19: SFR6 (Status Flag Register 6)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------|-------|-------|
| SHSF  | -     | -     | -     | TPCSF | TPSESF | -     | TPSF  |
| F     | 0     | 0     | 0     | F     | F      | 0     | F     |

**Bit 7 (SHSF):** System hold status flag, Set when system hold occur, reset by software.

**Bits 6~4:** Not used, set to "0" all the time

**Bit 3 (TPCSF):** Touch Key Compare status flag. Set when Touch Key idle with scan mode threshold compare conditions are fulfilled, reset by software.

**Bit 2 (TPSESF):** Touch Key Sense Error status flag. Set when Touch Key can't finish the conversion before timer get to the TPSTH/TPSTL register value, reset by software.

**Bit 1:** Not used, set to "0" all the time

**Bit 0 (TPSF):** Status flag for Touch Key Conversion. Set when Touch Key conversion is completed. Reset by software (except idle with scan mode condition)

### 6.1.21   Bank 0 R1A: (Reserved)

### 6.1.22   Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| -     | -     | LVDIE | ADIE  | EXIE1 | EXIE0 | WTIE  | TCIE  |
| 0     | 0     | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |

**Bits 7~6:** Not used, set to "0" all the time.

**Bit 5 (LVDIE):** LVDSF interrupt enable bit.

>        0: Disable LVDSF interrupt

>        1: Enable LVDSF interrupt

**Bit 4 (ADIE):** ADSF interrupt enable bit.

>        0: Disable ADSF interrupt

>        1: Enable ADSF interrupt.

**Bit 3 (EXIE1):** EXSF1 interrupt enable and **INT1 function enable bit.**

>        0: P51/ADC1/INT1/TPS9 is P51/ADC1/TPS9 pin,
>           EXSF1 always equal to 0.

>        1: Enable EXSF1 Interrupt and P51/ADC1/INT1/TPS9 is INT pin

**Bit 2 (EXIE0):** EXSF0 interrupt enable and **INT0 function enable bit.**

> 0: P50/ADC0/INT0/TPS10 is P50/ADC0/TPS10 pin,
>    EXSF0 always equals 0.

> 1: Enable EXSF0 Interrupt and P50/ADC0/INT0/TPS10 is INT pin

**Bit 1 (WTIE):** Watch timer interrupt enable bit

> 0: Disable WTSF interrupt

> 1: Enable WTSF interrupt

**Bit 0 (TCIE):** TCSF interrupt enable bit.

> 0: Disable TCSF interrupt

> 1: Enable TCSF interrupt

---

**NOTE**

*If the interrupt mask and instruction "ENI" is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.*

---

### 6.1.23   Bank 0 R1C: IMR2 (Interrupt Mask Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | TC3IE | TC2IE | TC1IE |
| 0 | 0 | 0 | 0 | 0 | R/W | R/W | R/W |

**Bits 7~3:** Not used, set to "0" all the time.

**Bit 2 (TC3IE)**: Interrupt enable bit.

> 0: Disable TC3SF interrupt

> 1: Enable TC3SF interrupt

**Bit 1 (TC2IE)**: Interrupt enable bit.

> 0: Disable TC2SF interrupt

> 1: Enable TC2SF interrupt

**Bit 0 (TC1IE)**: Interrupt enable bit.

> 0: Disable TC1SF interrupt

> 1: Enable TC1SF interrupt

**NOTE**

*If the interrupt mask and instruction "ENI" is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.*

### 6.1.24 Bank 0 R1D: IMR3 (Interrupt Mask Register 3)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | PWMBPIE | PWMBDIE | PWMAPIE | PWMADIE |
| 0 | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bits 7~4:** Not used, set to "0" all the time.

**Bit 3 (PWMBPIE):** PWMBPSF interrupt enable bit.

      0: Disable period-matching of PWMB interrupt

      1: Enable period-matching of PWMB interrupt

**Bit 2 (PWMBDIE):** PWMBDSF interrupt enable bit.

      0: Disable duty-matching of PWMB interrupt

      1: Enable duty-matching of PWMB interrupt

**Bit 1 (PWMAPIE):** PWMAPSF interrupt enable bit.

      0: Disable period-matching of PWMA interrupt

      1: Enable period-matching of PWMA interrupt

**Bit 0 (PWMADIE):** PWMADSF interrupt enable bit.

      0: Disable duty-matching of PWMA interrupt

      1: Enable duty-matching of PWMA interrupt

**NOTE**

*If the interrupt mask and instruction "ENI" is enabled, the program counter would jump into corresponding interrupt vector when the corresponding status flag is set.*

### 6.1.25 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| P8ICIE | - | P6ICIE | P5ICIE | - | I2CSTPIE | I2CRIE | I2CTIE |
| R/W | 0 | R/W | R/W | 0 | R/W | R/W | R/W |

**Bit 7 (P8ICIE):** P8ICSF interrupt enable bit.

      0: Disable P8ICSF interrupt

      1: Enable P8ICSF interrupt

**Bit 6:** Not used, set to "0" all the time.

**Bit 5 (P6ICIE):** P6ICSF interrupt enable bit.

> 0: Disable P6ICSF interrupt

> 1: Enable P6ICSF interrupt

**Bit 4 (P5ICIE):** P5ICSF interrupt enable bit.

> 0: Disable P5ICSF interrupt

> 1: Enable P5ICSF interrupt

**Bit 3:** Not used, set to "0" all the time.

**Bit 2 (I2CSTPIE):** I2C stop interrupt enable bit.

> 0: Disable interrupt

> 1: Enable interrupt

**Bit 1 (I2CRIE):** I2C Interface RX interrupt enable bit

> 0: Disable interrupt

> 1: Enable interrupt

**Bit 0 (I2CTIE):** I2C Interface TX interrupt enable bit

> 0: Disable interrupt

> 1: Enable interrupt

---

**NOTE**
*If the interrupt mask and instruction "ENI" is enabled, the program counter would jump into corresponding interrupt vector when the corresponding status flag is set.*

---

### 6.1.26 Bank 0 R1F: (Reserved)

### 6.1.27 Bank 0 R20: IMR6 (Interrupt Mask Register 6)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|---------|------|
| SHIE | - | - | - | TPCIE | - | TPERRIE | TPIE |
| R/W | 0 | 0 | 0 | R/W | 0 | R/W | R/W |

**Bit 7 (SHIE):** SHSF Interrupt Enable Bit.

> 0: Disable SHSF interrupt

> 1: Enable SHSF interrupt

**Bits 6~4:** Not used, set to "0" all the time.

**Bit 3 (TPCIE):** TPCSF Interrupt Enable Bit.

> 0: Disable TPCSF interrupt

> 1: Enable TPCSF interrupt

**Bit 2:** Not used, set to "0" all the time.

**Bit 1 (TPERRIE):** TPSESF Interrupt Enable Bit.

> 0: Disable TPSESF interrupt

> 1: Enable TPSESF interrupt

**Bit 0 (TPIE):** TPIE Interrupt Enable Bit.

> 0: Disable TPSF interrupt

> 1: Enable TPSF interrupt

### 6.1.28 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WDTE | - | - | - | PSWE | WPSR2 | WPSR1 | WPSR0 |
| R/W | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bit 7 (WDTE):** Watchdog Timer Enable Bit. WDTE is both readable and writable.

> 0: Disable WDT

> 1: Enable WDT

**Bits 6~4:** Not used, set to "0" all the time.

**Bit 3 (PSWE):** Prescaler enable bit for WDT

> 0: Prescaler disable bit. WDT rate is 1:1

> 1: Prescaler enable bit. WDT rate is set at Bits 2~0.

**Bits 2~0 (WPSR2~WPSR0):** WDT Prescaler Bits

| WPSR2 | WPSR1 | WPSR0 | WDT Rate |
|-------|-------|-------|----------|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

### *6.1.29   Bank 0 R22: TCCCR (TCC Control Register)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | TCCS | TS | TE | PSTE | TPSR2 | TPSR1 | TPSR0 |
| 0 | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7:** Not used, set to "0" all the time.

**Bit 6 (TCCS):** TCC Clock Source Select Bit

   0: Fs (sub clock)

   1: Fm (main clock)

**Bit 5 (TS):** TCC signal source

   0: Internal instruction cycle clock

   1: Transition on the TCC pin, TCC period must be larger than the
      internal instruction clock period.

**Bit 4 (TE):** TCC Signal Edge

   0: Increment if the transition from low to high takes place on the TCC
      pin;

   1: Increment if the transition from high to low takes place on the TCC pin

**Bit 3 (PSTE):** Prescaler enable bit for TCC

   0: Prescaler disable bit. TCC rate is 1:1.

   1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

**Bits 2~0 (TPSR2~TPSR0):** TCC Prescaler Bits

| TPSR2 | TPSR1 | TPSR0 | TCC Rate |
|:---:|:---:|:---:|:---:|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

## 6.1.30 Bank 0 R23: TCCD (TCC Data Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| TCC7 | TCC6 | TCC5 | TCC4 | TCC3 | TCC2 | TCC1 | TCC0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TCC7~TCC0):** TCC data

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. Writable and readable as any other registers.

## 6.1.31 Bank 0 R24: TC1CR1 (Timer/Counter 1 Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| TC1S | TC1RC | TC1SS1 | TC1MOD | TC1FF | TC1MOS | TC1IS1 | TC1IS0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (TC1S):** Timer/Counter 1 Start Control Bit

> 0: Stop and clear counter (default)

> 1: Start

**Bit 6 (TC1RC)**: Timer 1 Read Control Bit. To load current number of counter into TC1DB register. It's useful only in counter mode.

> 0: Disable function. When using capture mode, this bit must be set to "0" (default).

> 1: Enable function. The number of counting are loaded into TC1DB.

**Bit 5 (TC1SS1):** Timer/Counter 1 Clock Source Select Bit 1

>> 0: Internal clock as count source (Fc)- Fs/Fm (default)

>> 1: External TC1 pin as count source (Fc). It is used only for timer/counter mode.

**Bit 4 (TC1MOD):** Timer Operation Mode Selection Bit

>> 0: Two 8-bit timers

>> 1: Timers 1 and 2 are cascaded as one 16-bit timer. The corresponding control register of 16-bit timer is from timer 1. TC2DB and TC2DA are high byte. TC1DB and TC1DA are low byte.

**Bit 3 (TC1FF):** Inversion for Timer/Counter 1 as PWM or PDO mode

>> 0: Duty is Logic 1 (default)

>> 1: Duty is Logic 0

**Bit 2 (TC1MOS):** Timer Output Mode Select Bit

>> 0: Repeating mode (default)

>> 1: One–shot mode

---

**NOTE**
*One-shot mode means the timer only counts one cycle.*

---

**Bits 1~0 (TC1IS1~ TC1IS0):** Timer 1 Interrupt Type Select Bits.  These two bits are used when the Timer operates in PWM mode.

| TC1IS1 | TC1IS0 | Timer 1 Interrupt Type Select |
|--------|--------|-------------------------------|
| 0 | 0 | TC1DA (period) matching |
| 0 | 1 | TC1DB (duty) matching |
| 1 | x | TC1DA and TC1DB matching |

### 6.1.32   Bank 0 R25: TC1CR2 (Timer/Counter 1 Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC1M2 | TC1M1 | TC1M0 | TC1SS0 | TC1CK3 | TC1CK2 | TC1CK1 | TC1CK0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5 (TC1M2~TC1M0):** Timer/Counter 1 operation mode select.

| TC1M2 | TC1M1 | TC1M0 | Operating Mode Select |
|:---:|:---:|:---:|---|
| 0 | 0 | 0 | Timer/Counter Rising Edge |
| 0 | 0 | 1 | Timer/Counter Falling Edge |
| 0 | 1 | 0 | Capture Mode Rising Edge |
| 0 | 1 | 1 | Capture Mode Falling Edge |
| 1 | 0 | 0 | Window mode |
| 1 | 0 | 1 | Programmable Divider output |
| 1 | 1 | 0 | Pulse Width Modulation output |
| 1 | 1 | 1 | Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50) |

**Bit 4 (TC1SS0):** Timer/Counter 1 clock source selection bit

**0** : The Fs is used as count source (Fc) (default)

**1** : The Fm is used as count source (Fc)

**Bits 3~0 (TC1CK3~TC1CK0):** Timer/Counter 1 clock source prescaler select.

| TC1CK3 | TC1CK2 | TC1CK1 | TC1CK0 | Clock Source Normal | Resolution 8 MHz $F_C=8M$ | Max time 8 MHz $F_C=8M$ | Resolution 16kHz $F_C=16K$ | Max. time 16kHz $F_C=16K$ |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| 0 | 0 | 0 | 0 | $F_C$ | 125ns | 32 µs | 62.5 µs | 16ms |
| 0 | 0 | 0 | 1 | $F_C/2$ | 250ns | 64 µs | 125 µs | 32ms |
| 0 | 0 | 1 | 0 | $F_C/2^2$ | 500ns | 128 µs | 250 µs | 64ms |
| 0 | 0 | 1 | 1 | $F_C/2^3$ | 1µs | 256 µs | 500 µs | 128ms |
| 0 | 1 | 0 | 0 | $F_C/2^4$ | 2µs | 512 µs | 1ms | 256ms |
| 0 | 1 | 0 | 1 | $F_C/2^5$ | 4µs | 1024 µs | 2ms | 512ms |
| 0 | 1 | 1 | 0 | $F_C/2^6$ | 8µs | 2048 µs | 4ms | 1024ms |
| 0 | 1 | 1 | 1 | $F_C/2^7$ | 16µs | 4096 µs | 8ms | 2048ms |
| 1 | 0 | 0 | 0 | $F_C/2^8$ | 32µs | 8192 µs | 16ms | 4096ms |
| 1 | 0 | 0 | 1 | $F_C/2^9$ | 64µs | 16384 µs | 32ms | 8192ms |
| 1 | 0 | 1 | 0 | $F_C/2^{10}$ | 128µs | 32768 µs | 64ms | 16384ms |
| 1 | 0 | 1 | 1 | $F_C/2^{11}$ | 256µs | 65536 µs | 128ms | 32768ms |
| 1 | 1 | 0 | 0 | $F_C/2^{12}$ | 512µs | 131072 µs | 256ms | 65536ms |
| 1 | 1 | 0 | 1 | $F_C/2^{13}$ | 1.024ms | 262144 µs | 512ms | 131072ms |
| 1 | 1 | 1 | 0 | $F_C/2^{14}$ | 2.048ms | 524.288ms | 1.024s | 262144ms |
| 1 | 1 | 1 | 1 | $F_C/2^{15}$ | 4.096ms | 1.048s | 2.048s | 524288ms |

### 6.1.33   Bank 0 R26: TC1DA (Timer/Counter 1 Data Buffer A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC1DA7 | TC1DA6 | TC1DA5 | TC1DA4 | TC1DA3 | TC1DA2 | TC1DA1 | TC1DA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC1DA7~TC1DA0):** Data Buffer A of 8-bit Timer/Counter 1

### 6.1.34   Bank 0 R27: TC1DB (Timer/Counter 1 Data Buffer B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC1DB7 | TC1DB6 | TC1DB5 | TC1DB4 | TC1DB3 | TC1DB2 | TC1DB1 | TC1DB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC1DB7~TC1DB0):** Data Buffer B of 8 bit Timer/Counter 1

---

**NOTE**

1.  *When Timer / Counter x is used as PWM mode, the duty value stored at register TCxDB must be smaller than or equal to the period value stored at register TCxDA.,i.e. duty $\leq$ period. And then the PWM waveform is generated. If duty is larger than the period, the PWM output waveform is kept at* **high** *voltage level.*

2.  *The period value set by users is extra plus 1 in inner circuit.*
    *For example:*
    *The period value is set as 0x4F, the circuit actually processes 0x50 period length.*
    *The period value is set as 0xFF, the circuit actually processes 0x100 period length.*

---

### 6.1.35   Bank 0 R28: TC2CR1 (Timer/Counter 2 Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC2S | TC2RC | TC2SS1 | – | TC2FF | TC2MOS | TC2IS1 | TC2IS0 |
| R/W | R/W | R/W | – | R/W | R/W | R/W | R/W |

**Bit 7 (TC2S):** Timer/Counter 2 Start Control Bit

> 0: Stop and clear counter (default)

> 1: Start

**Bit 6 (TC2RC):** Timer 2 Read Control Bit

> 0: When this bit is set to 0, cannot read data from TC2DB (default).

> 1: When this bit is set to 1, data read from TC2DB is a number of
>    counting.

**Bit 5 (TC2SS1):** Timer/Counter 2 clock source select Bit 1

　　　　　 0: Internal clock as count source (Fc)- Fs/Fm (default)

　　　　　 1: External TC2 pin as count source (Fc). It is used only for timer/counter mode.

**Bit 4:** Not used, set to "0" all the time.

**Bit 3 (TC2FF):** Inversion for Timer/Counter 2 as PWM or PDO mode

　　　　　 0: Duty is Logic 1 (default)

　　　　　 1: Duty is Logic 0

**Bit 2 (TC2MOS):** Timer Output Mode Select Bit

　　　　　 0: Repeating mode (default)

　　　　　 1: One–shot mode

---

**NOTE**

*One-shot mode means the timer only counts one cycle.*

---

**Bits 1~0 (TC2IS1~ TC2IS0):** Timer 2 Interrupt Type Select Bits.  These two bits are used when the Timer operates in PWM mode.

| TC2IS1 | TC2IS0 | Timer 2 Interrupt Type Select |
|--------|--------|-------------------------------|
| 0 | 0 | TC2DA (period) matching |
| 0 | 1 | TC2DB (duty) matching |
| 1 | x | TC2DA and TC2DB matching |

## 6.1.36 Bank 0 R29: TC2CR2 (Timer/Counter 2 Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC2M2 | TC2M1 | TC2M0 | TC2SS0 | TC2CK3 | TC2CK2 | TC2CK1 | TC2CK0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5 (TC2M2~TC2M0):** Timer/Counter 2 operation mode select.

| TC2M2 | TC2M1 | TC2M0 | Operating Mode Select |
|-------|-------|-------|-----------------------|
| 0 | 0 | 0 | Timer/Counter Rising Edge |
| 0 | 0 | 1 | Timer/Counter Falling Edge |
| 0 | 1 | 0 | Capture Mode Rising Edge |
| 0 | 1 | 1 | Capture Mode Falling Edge |
| 1 | 0 | 0 | Window mode |
| 1 | 0 | 1 | Programmable Divider output |
| 1 | 1 | 0 | Pulse Width Modulation output |
| 1 | 1 | 1 | Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50) |

**Bit 4 (TC2SS0):** Timer/Counter 2 clock source select Bit 0

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

**Bits 3~0 (TC2CK3~TC2CK0):** Timer/Counter 2 clock source prescaler select.

| TC2CK3 | TC2CK2 | TC2CK1 | TC2CK0 | Clock Source | Resolution 8 MHz | Max. time 8 MHz | Resolution 16kHz | Max time 16kHz |
|---|---|---|---|---|---|---|---|---|
| | | | | Normal | $F_C$=8M | $F_C$=8M | $F_C$=16K | $F_C$=16K |
| 0 | 0 | 0 | 0 | $F_C$ | 125ns | 32 µs | 62.5 µs | 16ms |
| 0 | 0 | 0 | 1 | $F_C/2$ | 250ns | 64 µs | 125 µs | 32ms |
| 0 | 0 | 1 | 0 | $F_C/2^2$ | 500ns | 128 µs | 250 µs | 64ms |
| 0 | 0 | 1 | 1 | $F_C/2^3$ | 1 µs | 256 µs | 500 µs | 128ms |
| 0 | 1 | 0 | 0 | $F_C/2^4$ | 2 µs | 512 µs | 1ms | 256ms |
| 0 | 1 | 0 | 1 | $F_C/2^5$ | 4 µs | 1024 µs | 2ms | 512ms |
| 0 | 1 | 1 | 0 | $F_C/2^6$ | 8 µs | 2048 µs | 4ms | 1024ms |
| 0 | 1 | 1 | 1 | $F_C/2^7$ | 16 µs | 4096 µs | 8ms | 2048ms |
| 1 | 0 | 0 | 0 | $F_C/2^8$ | 32 µs | 8192 µs | 16ms | 4096ms |
| 1 | 0 | 0 | 1 | $F_C/2^9$ | 64 µs | 16384 µs | 32ms | 8192ms |
| 1 | 0 | 1 | 0 | $F_C/2^{10}$ | 128 µs | 32768 µs | 64ms | 16384ms |
| 1 | 0 | 1 | 1 | $F_C/2^{11}$ | 256 µs | 65536 µs | 128ms | 32768ms |
| 1 | 1 | 0 | 0 | $F_C/2^{12}$ | 512 µs | 131072 µs | 256ms | 65536ms |
| 1 | 1 | 0 | 1 | $F_C/2^{13}$ | 1.024ms | 262144 µs | 512ms | 131072ms |
| 1 | 1 | 1 | 0 | $F_C/2^{14}$ | 2.048ms | 524.288ms | 1.024s | 262144ms |
| 1 | 1 | 1 | 1 | $F_C/2^{15}$ | 4.096ms | 1.048s | 2.048s | 524288ms |

### 6.1.37  Bank 0 R2A: TC2DA (Timer/Counter 2 Data Buffer A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| TC2DA7 | TC2DA6 | TC2DA5 | TC2DA4 | TC2DA3 | TC2DA2 | TC2DA1 | TC2DA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC2DA7~TC2DA0):** Data Buffer A of the 8 bit Timer/Counter 2.

### 6.1.38  Bank 0 R2B: TC2DB (Timer/Counter 2 Data Buffer B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| TC2DB7 | TC2DB6 | TC2DB5 | TC2DB4 | TC2DB3 | TC2DB2 | TC2DB1 | TC2DB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC2DB7~TC2DB0):** Data Buffer B of the 8 bit Timer/Counter 2

### 6.1.39    Bank 0 R2C: TC3CR1 (Timer/Counter 3 Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------|--------|--------|
| TC3S | TC3RC | TC3SS1 | - | TC3FF | TC3MOS | TC3IS1 | TC3IS0 |
| R/W | R/W | R/W | 0 | R/W | R/W | R/W | R/W |

**Bit 7 (TC3S):** Timer/Counter 3 start control

> 0: Stop and clear counter (default)

> 1: Start

**Bit 6 (TC3RC):** Timer 3 Read Control Bit

> 0: When this bit is set to 0, cannot read data from TC3DB (default).

> 1: When this bit is set to 1, data read from TC3DB is a number of counting.

**Bit 5 (TC3SS1):** Timer/Counter 3 clock source select Bit 1
> 0: Internal clock as count source (Fc)- Fs/Fm (default)

> 1: External TC3 pin as count source (Fc). It is used only for timer/counter mode.

**Bit 4:** Not used, set to "0" all the time.

**Bit 3 (TC3FF):** Inversion for Timer/Counter 3 as PWM or PDO mode.

> 0: Duty is Logic 1 (default)

> 1: Duty is Logic 0.

**Bit 2 (TC3MOS):** Timer Output Mode Select Bit

> 0: Repeating mode (default)

> 1: One–shot mode

---

**NOTE**
*One-shot mode means the timer only counts a circle.*

---

**Bits 1~0 (TC3IS1~ TC3IS0):** Timer 3 Interrupt Type Select Bits.  These two bits are used when the Timer operates in PWM mode.

| TC3IS1 | TC3IS0 | Timer 3 Interrupt Type Select |
|--------|--------|-------------------------------|
| 0 | 0 | TC3DA(period) matching |
| 0 | 1 | TC3DB(duty) matching |
| 1 | x | TC3DA and TC3DB matching |

### 6.1.40 Bank 0 R2D: TC3CR2 (Timer/Counter 3 Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| TC3M2 | TC3M1 | TC3M0 | TC3SS0 | TC3CK3 | TC3CK2 | TC3CK1 | TC3CK0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5 (TC3M2~TC3M0):** Timer/Counter 3 operation mode select.

| TC3M2 | TC3M1 | TC3M0 | Operating Mode Select |
|-------|-------|-------|------------------------|
| 0 | 0 | 0 | Timer/Counter Rising Edge |
| 0 | 0 | 1 | Timer/Counter Falling Edge |
| 0 | 1 | 0 | Capture Mode Rising Edge |
| 0 | 1 | 1 | Capture Mode Falling Edge |
| 1 | 0 | 0 | Window mode |
| 1 | 0 | 1 | Programmable Divider output |
| 1 | 1 | 0 | Pulse Width Modulation output |
| 1 | 1 | 1 | Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50) |

**Bit 4 (TC3SS0):** Timer/Counter 3 clock source select Bit 0

0: The Fs is used as count source (Fc) (default)

1: The Fm is used as count source (Fc)

**Bits 3~0 (TC3CK3~TC3CK0):** Timer/Counter 3 clock source prescaler select.

| TC3CK3 | TC3CK2 | TC3CK1 | TC3CK0 | Clock Source | Resolution 8 MHz | Max. time 8 MHz | Resolution 16kHz | Max. time 16kHz |
|--------|--------|--------|--------|--------------|------------------|-----------------|------------------|-----------------|
| | | | | Normal | $F_C$=8M | $F_C$=8M | $F_C$=16K | $F_C$=16K |
| 0 | 0 | 0 | 0 | $F_C$ | 125ns | 32 µs | 62.5 µs | 16ms |
| 0 | 0 | 0 | 1 | $F_C/2$ | 250ns | 64 µs | 125 µs | 32ms |
| 0 | 0 | 1 | 0 | $F_C/2^2$ | 500ns | 128 µs | 250 µs | 64ms |
| 0 | 0 | 1 | 1 | $F_C/2^3$ | 1 µs | 256 µs | 500 µs | 128ms |
| 0 | 1 | 0 | 0 | $F_C/2^4$ | 2 µs | 512 µs | 1ms | 256ms |
| 0 | 1 | 0 | 1 | $F_C/2^5$ | 4 µs | 1024 µs | 2ms | 512ms |
| 0 | 1 | 1 | 0 | $F_C/2^6$ | 8 µs | 2048 µs | 4ms | 1024ms |
| 0 | 1 | 1 | 1 | $F_C/2^7$ | 16 µs | 4096 µs | 8ms | 2048ms |
| 1 | 0 | 0 | 0 | $F_C/2^8$ | 32 µs | 8192 µs | 16ms | 4096ms |
| 1 | 0 | 0 | 1 | $F_C/2^9$ | 64 µs | 16384 µs | 32ms | 8192ms |
| 1 | 0 | 1 | 0 | $F_C/2^{10}$ | 128 µs | 32768 µs | 64ms | 16384ms |
| 1 | 0 | 1 | 1 | $F_C/2^{11}$ | 256 µs | 65536 µs | 128ms | 32768ms |
| 1 | 1 | 0 | 0 | $F_C/2^{12}$ | 512 µs | 131072 µs | 256ms | 65536ms |
| 1 | 1 | 0 | 1 | $F_C/2^{13}$ | 1.024ms | 262144 µs | 512ms | 131072ms |
| 1 | 1 | 1 | 0 | $F_C/2^{14}$ | 2.048ms | 524.288ms | 1.024s | 262144ms |
| 1 | 1 | 1 | 1 | $F_C/2^{15}$ | 4.096ms | 1.048s | 2.048s | 524288ms |

### 6.1.41 Bank 0 R2E: TC3DA (Timer/Counter 3 Data Buffer A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC3DA7 | TC3DA6 | TC3DA5 | TC3DA4 | TC3DA3 | TC3DA2 | TC3DA1 | TC3DA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC3DA7~TC3DA0):** Data Buffer A of 8 bit Timer/Counter 3

### 6.1.42 Bank 0 R2F: TC3DB (Timer/Counter 3 Data Buffer B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TC3DB7 | TC3DB6 | TC3DB5 | TC3DB4 | TC3DB3 | TC3DB2 | TC3DB1 | TC3DB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TC3DB7~TC3DB0):** Data Buffer B of 8 bit Timer/Counter 3

### 6.1.43 Bank 0 R30: I2CCR1 (I2C Status and Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Strobe/Pend | IMS | ISS | STOP | SAR_EMPTY | ACK | FULL | EMPTY |
| R/W | R/W | R/W | R/W | R | R | R | R |

**Bit 7 (Strobe/Pend):** In master mode, it is used as strobe signal to control I2C circuit to send SCL clock. Reset automatically after receiving or transmitting handshake signal (ACK or NACK). In slave mode, it is used as pending signal, user should clear it after filling data into Tx buffer or obtaining data from Rx buffer to inform slave I2C circuit to release SCL signal.

**Bit 6 (IMS):** I2C Master/Slave mode select bit.

    0: Slave (Default)

    1: Master

**Bit 5 (ISS):** I2C Fast/Standard mode select bit. (If Fm is 4 MHz and I2CTS2~0<0,0,1>)

    0: Standard mode (100K bit/s)

    1: Fast mode (400K bit/s)

**Bit 4 (STOP):** In Master mode, if STOP=1 and R/nW=1 then MCU must return nACK signal to slave device before send STOP signal. If STOP=1 and R/nW=0 then MCU send STOP signal after receive an ACK signal. Reset when MCU send STOP signal to Slave device. In slave mode, if STOP=1 and R/nW=0 then MCU must return nACK signal to master device.

**Bit 3 (SAR_EMPTY):** Set when MCU transmit 1 byte data from I2C Slave Address Register and receive ACK (or nACK) signal. Reset when MCU write 1 byte data to I2C Slave Address Register.

**Bit 2 (ACK):** The ACK condition bit is set to 1 by hardware when the device responds acknowledge (ACK). Reset when the device responds not-acknowledge (nACK) signal

**Bit 1 (FULL):** Set by hardware when I2C receive buffer register is full. Reset by hardware when MCU read data from I2C receive buffer register.

**Bit 0 (EMPTY):** Set by hardware when I2C transmit buffer register is empty and receive ACK (or nACK) signal. Reset by hardware when MCU write new data to I2C transmit buffer register.

### 6.1.44   Bank 0 R31: I2CCR2 (I2C Status and Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| I2CBF | GCEN | I2COPT | BBF | I2CTS2 | I2CTS1 | I2CTS0 | I2CEN |
| R | R/W | R/W | R | R/W | R/W | R/W | R/W |

**Bit 7 (I2CBF):** I2C Busy Flag Bit

0: clear to "0", in Slave mode, if receive STOP signal or I2C slave address not match.

1: set when I2C communicate with master in slave mode.

*Set when STAR signal, clear when I2C disable or STOP signal for Slave mode.

**Bit 6 (GCEN):** I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

**Bit 5 (I2COPT):** I2C pin optional bit. It is used to switch the pin position of I2C function.

0: Placed I2C pins in P62 (SDA0) and P82 (SCL0) (default)

1: Placed I2C pins in P84 (SDA1) and P83 (SCL1).

*Default value corresponding code option Word2 I2COPT

**Bit 4 (BBF):** Busy Flag Bit. I2C detection is busy in the master mode. Read only.

*Set when STAR signal, clear when STOP signal for Master mode.

**Bits 3~1 (I2CTS2~I2CTS0):** I2C Transmit Clock Select Bits. When using different operating frequency (Fm), these bits must be set correctly to let SCL clock fill-in with standard/fast mode.

I2CCR1 Bit 5=1, Fast Mode

| I2CTS2 | I2CTS1 | I2CTS0 | SCL CLK | Operating Fm (MHz) |
|--------|--------|--------|---------|---------------------|
| 0 | 0 | 0 | NA | NA |
| 0 | 0 | 1 | Fm/10 | 4 |
| 0 | 1 | 0 | Fm/15 | 6 |
| 0 | 1 | 1 | Fm/20 | 8 |
| 1 | 0 | 0 | Fm/30 | 12 |
| 1 | 0 | 1 | Fm/40 | 16 |
| 1 | 1 | 0 | Fm/50 | 20 |
| 1 | 1 | 1 | NA | NA |

I2CCR1 Bit 5=0, Standard Mode

| I2CTS2 | I2CTS1 | I2CTS0 | SCL CLK | Operating Fm (MHz) |
|--------|--------|--------|---------|---------------------|
| 0 | 0 | 0 | Fm/10 | 1 |
| 0 | 0 | 1 | Fm/40 | 4 |
| 0 | 1 | 0 | Fm/60 | 6 |
| 0 | 1 | 1 | Fm/80 | 8 |
| 1 | 0 | 0 | Fm/120 | 12 |
| 1 | 0 | 1 | Fm/160 | 16 |
| 1 | 1 | 0 | Fm/200 | 20 |
| 1 | 1 | 1 | NA | NA |

**Bit 0 (I2CEN):** I2C Enable Bit

0: Disable I2C mode (Default)

1: Enable I2C mode

### 6.1.45   Bank 0 R32: I2CSA (I2C Slave Address Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | IRW |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~1 (SA6~SA0):** When MCU used as master device for I2C application. This is the slave device address register.

**Bit 0 (IRW):** When MCU used as master device for I2C application. This bit is Read/Write transaction control bit.

0: Write

1: Read

### 6.1.46    Bank 0 R33: I2CDB (I2C Data Buffer Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (DB7~DB0):** I2C Receive/Transmit Data Buffer.

### 6.1.47    Bank 0 R34: I2CDAL (I2C Device Address Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (DA7~DA0):** When MCU used as slave device for I2C application, this
register store the address of MCU. It is used to identify the data on the I2C
bus to extract the message delivered to the MCU.

### 6.1.48    Bank 0 R35: I2CDAH (I2C Device Address Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | DA9 | DA8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~2:** Not used bits, set to "0" all the time.

**Bits 1~0 (DA9~DA8):** Device address bits.

### 6.1.49    Bank 0 R36 ~R3D: (Reserved)

### 6.1.50    Bank 0 R3E: ADCR1 (ADC Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CKR2 | CKR1 | CKR0 | ADRUN | ADP | ADOM | SHS1 | SHS0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5 (CKR2~0):** Clock Rate Selection of ADC

| System Mode | CKR2~0 | Clock Rate | Max. System Operation Frequency in 2.1~2.2V | Max. System Operation Frequency in 2.2~2.7V | Max. System Operation Frequency in 2.7~5V |
|---|---|---|---|---|---|
| Normal Mode | 000 | FMain/16 | 8 MHz | 16 MHz | 20 MHz |
| | 001 | FMain/8 | 4 MHz | 8 MHz | 16 MHz |
| | 010 | FMain/4 | 2 MHz | 4 MHz | 8 MHz |
| | 011 | FMain/2 | 1 MHz | 2 MHz | 4 MHz |
| | 100 | FMain/64 | 20 MHz | 20 MHz | 20 MHz |
| | 101 | FMain/32 | 16 MHz | 20 MHz | 20 MHz |
| | 110 | FMain/1 | 500 kHz | 1 MHz | 2 MHz |
| | 111 | FSub | Fs | Fs | Fs |
| Green Mode | xxx | FSub | Fs | Fs | Fs |

**Bit 4 (ADRUN):** ADC Starts to Run

**In single mode:**

0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software

**In continuous mode:**

0: ADC is stopped.

1: ADC is running unless this bit is reset by software

**Bit 3 (ADP):** ADC Power

0: ADC is in power down mode.

1: ADC is operating normally.

**Bit 2 (ADOM):** ADC Operation Mode Selection

0: ADC operates in single mode.

1: ADC operates in continuous mode.

**Bits 1~0 (SHS1~0):** Sample and Hold Timing Selection

| SHS[1:0] | Sample and Hold Timing |
|---|---|
| 00 | $2 \times T_{AD}$ |
| 01 | $4 \times T_{AD}$ |
| 10 | $8 \times T_{AD}$ |
| 11 | $12 \times T_{AD}$ |

### 6.1.51 Bank 0 R3F: ADCR2 (ADC Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | VPIS2 | ADIM | ADCMS | VPIS1 | VPIS0 | VREFP | - |
| 0 | R/W | R/W | R/W | R/W | R/W | R/W | 0 |

**Bit 7:** Not used, set to "0" all the time.

**Bit 5 (ADIM):** ADC Interrupt Mode

> 0: Normal mode. Interrupt occurred after AD conversion completed.

> 1: Compare mode. Interrupt occurred when comparison result conforms the setting of ADCMS bits.

**Bit 4 (ADCMS):** ADC Comparison Mode Selection.

**In compare mode:**

> 0: Interrupt occurred when AD conversion data is greater than data in ADCD register.

> It means when ADD > ADCD, interrupt occurred.

> 1: Interrupt occurred when AD conversion data is less than data in ADCD register.

> It means when ADD < ADCD, interrupt occurred.

**In normal mode:**

> No effect

**Bits 6, 3 ~ 2 (VPIS2~0):** Internal Positive Reference Voltage Selection.

| VPIS[2] | VPIS[1:0] | Reference Voltage |
|---------|-----------|-------------------|
| 0 | 00 | AVDD |
| 0 | 01 | 4 V |
| 0 | 10 | 3 V |
| 0 | 11 | 2 V |
| 1 | 11 | 2.5 V |

**Bit 1 (VREFP):** Positive Reference Voltage Selection

> 0: Internal positive reference voltage. The actual voltage is set by VPIS[1:0] bits

> 1: From VREF pin.

**Bit 0:** Not used, set to "0" all the time.

---

**NOTE**

*When using internal voltage reference and the code option word2<7> is set to "0", users need to wait 50 μs at least the first time to enable and stabilize the internal voltage reference circuit. After that, users only need to wait 6us at least whenever switching voltage references.*

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### 6.1.52    Bank 0 R40: ADISR (Analog to Digital Converter Input Channel Selection Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | ADIS3 | ADIS2 | ADIS1 | ADIS0 |
| 0 | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bits 7~4:** Not used, set to "0" all the time.

**Bits 3~0 (ADIS4~0):** ADC input channel selection bits

| ADIS[3:0] | Selected Channel |
|-----------|------------------|
| 0000 | ADC0 |
| 0001 | ADC1 |
| 0010 | ADC2 |
| 0011 | ADC3 |
| 0100 | ADC4 |
| 0101 | ADC5 |
| 0110 | ADC6 |
| 0111 | ADC7 |
| 1xxx* | 1/2 VDD PowerDet. |

***Note:***

*: For internal signal source use. Users only need to set ADIS3=1, these AD input
channels are instantly active, internal Vref Stable Time is 4 μs.

### 6.1.53 Bank 0 R41: ADER 1 (Analog to Digital Converter Input Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (ADE7):** AD converter enable bit of P67 pin.

> 0: Disable ADC7, P57/PWMB/ADC7/TPS3 act as I/O or PWMB or TPS3 pin

> 1: Enable ADC7 act as analog input pin.

**Bit 6 (ADE6):** AD converter enable bit of P56 pin.

> 0: Disable ADC6, P56/PWMA/ADC6/TPS4 act as I/O or PWMA or TPS4 pin

> 1: Enable ADC6 act as analog input pin

**Bit 5 (ADE5):** AD converter enable bit of P55 pin.

> 0: Disable ADC5, P55/ADC5/TPS5 act as I/O or TPS5 pin

> 1: Enable ADC5 act as analog input pin

**Bit 4 (ADE4):** AD converter enable bit of P54 pin.

> 0: Disable ADC4, P54/ADC4/TPS6 act as I/O or TPS6 pin

> 1: Enable ADC4 act as analog input pin

**Bit 3 (ADE3):** AD converter enable bit of P53 pin.

> 0: Disable ADC3, P53/ADC3/TPS7 act as I/O or TPS7 pin

> 1: Enable ADC3 act as analog input pin

**Bit 2 (ADE2):** AD converter enable bit of P52 pin.

> 0: Disable ADC2, P52/ADC2/TCC/TPS8 act as I/O or TCC or TPS8 pin

> 1: Enable ADC2 act as analog input pin

**Bit 1 (ADE1):** AD converter enable bit of P51 pin.

> 0: Disable ADC1, P51/ADC1/INT1/TPS9 act as I/O or /INT1 or TPS9 pin

> 1: Enable ADC1 act as analog input pin

**Bit 0 (ADE0):** AD converter enable bit of P50 pin.

> 0: Disable ADC0, P50/ADC0/INT0/TPS10 act as I/O or /INT0 or TPS10 pin

> 1: Enable ADC0 act as analog input pin

### 6.1.54 Bank 0 R42: (Reserved)

### 6.1.55 Bank 0 R43: ADDL (Low Byte of Analog to Digital Converter Data)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (ADD7~0):** Low Byte of AD Data Buffer

### 6.1.56 Bank 0 R44: ADDH (High Byte of Analog to Digital Converter Data)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADD15 | ADD14 | ADD13 | ADD12 | ADD11 | ADD10 | ADD9 | ADD8 |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (ADD15~8):** High Byte of AD Data Buffer.

The format of AD data is dependent on code option ADFM. The following table shows how the data justified in different ADFM setting.

| ADFM | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|---|------|-------|-------|-------|-------|-------|-------|-------|-------|
| 12 bits | 0 | ADDH | | | | | ADD11 | ADD10 | ADD9 | ADD8 |
| | | ADDL | ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| | 1 | ADDH | ADD11 | ADD10 | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 |
| | | ADDL | | | | | ADD3 | ADD2 | ADD1 | ADD0 |

### 6.1.57 Bank 0 R45 ADCVL (Low Byte of Analog to Digital Converter Comparison)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADCD7 | ADCD6 | ADCD5 | ADCD4 | ADCD3 | ADCD2 | ADCD1 | ADCD0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (ADCD7~0):** Low Byte Data for AD Comparison.

User should use the data format as the same as ADDH and ADDL register. Otherwise, the fault result will be got after AD comparison.

### *6.1.58   Bank 0 R46 ADCVH (High Byte of Analog to Digital Converter Comparison)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADCD15 | ADCD14 | ADCD13 | ADCD12 | ADCD11 | ADCD10 | ADCD9 | ADCD8 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (ADCD15~8):** High Byte Data for AD Comparison

User should use the data format the same as ADDH and ADDL register. Otherwise, the fault result will be got after AD comparison.

### *6.1.59   Bank 0 R47 ~ R4F (Reserved)*

### *6.1.60   Bank 1 R5 IOCR8 (I/O Port 8 Control Register)*

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance (default)

### *6.1.61   Bank 1 R6 ~ R7 (Reserved)*

### *6.1.62   Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH57 | PH56 | PH55 | PH54 | PH53 | PH52 | PH51 | PH50 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (PH57):** Control bit used to enable pull-high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high (default)

**Bit 6 (PH56):** Control bit used to enable pull-high of the P56 pin

**Bit 5 (PH55):** Control bit used to enable pull-high of the P55 pin

**Bit 4 (PH54):** Control bit used to enable pull-high of the P54 pin

**Bit 3 (PH53):** Control bit used to enable pull-high of the P53 pin

**Bit 2 (PH52):** Control bit used to enable pull-high of the P52 pin

**Bit 1 (PH51):** Control bit used to enable pull-high of the P51 pin

**Bit 0 (PH50):** Control bit used to enable pull-high of the P50 pin

### 6.1.63 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | PH64 | PH63 | PH62 | PH61 | PH60 |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time

**Bit 4 (PH64):** Control bit used to enable pull-high of the P64 pin

      0: Enable internal pull-high

      1: Disable internal pull-high (default)

**Bit 3 (PH63):** Control bit used to enable pull-high of the P63 pin

**Bit 2 (PH62):** Control bit used to enable pull-high of the P62 pin

**Bit 1 (PH61):** Control bit used to enable pull-high of the P61 pin

**Bit 0 (PH60):** Control bit used to enable pull-high of the P60 pin

### 6.1.64 Bank 1 RA: P8PHCR (Port 8 Pull-high Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | P8HPH | P8LPH | - | - |
| 0 | 0 | 0 | 0 | R/W | R/W | 0 | 0 |

**Bits 7~4:** Not used, set to "0" all the time.

**Bit 3 (P8HPH):** Control bit used to enable pull-high of the Port 8 high nibble pin

      0: Enable internal pull-high

      1: Disable internal pull-high (default)

**Bit 2 (P8LPH):** Control bit used to enable the pull high of Port 8 low nibble pin

**Bits 1~0:** Not used, set to "0" all the time.

### 6.1.65   Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PL57 | PL56 | PL55 | PL54 | PL53 | PL52 | PL51 | PL50 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (PL57):** Control bit used to enable pull low of the P57 pin

        0: Enable internal pull-low

        1: Disable internal pull-low (default)

**Bit 6 (PL56):** Control bit used to enable pull low of the P56 pin

**Bit 5 (PL55):** Control bit used to enable pull low of the P55 pin

**Bit 4 (PL54):** Control bit used to enable pull low of the P54 pin

**Bit 3 (PL53):** Control bit used to enable pull low of the P53 pin

**Bit 2 (PL52):** Control bit used to enable pull low of the P52 pin

**Bit 1 (PL51):** Control bit used to enable pull low of the P51 pin

**Bit 0 (PL50):** Control bit used to enable pull low of the P50 pin

### 6.1.66   Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | PL64 | PL63 | PL62 | PL61 | PL60 |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time.

**Bit 4 (PL64):** Control bit used to enable pull low of the P64 pin

        0: Enable internal pull-low

        1: Disable internal pull-low (default)

**Bit 3 (PL63):** Control bit used to enable pull low of the P63 pin

**Bit 2 (PL62):** Control bit used to enable pull low of the P62 pin

**Bit 1 (PL61):** Control bit used to enable pull low of the P61 pin

**Bit 0 (PL60):** Control bit used to enable pull low of the P60 pin

### 6.1.67 Bank 1 RD: P8PLCR (Ports 8 Pull-low Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | P8HPL | P8LPL | - | - |
| 0 | 0 | 0 | 0 | R/W | R/W | 0 | 0 |

**Bits 7~4:** Not used, set to "0" all the time.

**Bit 3 (P8HPL):** Control bit used to enable pull low of the Port 8 low nibble pin

        0: Enable internal pull-low

        1: Disable internal pull-low (default)

**Bit 2 (P8LPL):** Control bit used to enable pull low of the Port 8 low nibble pin

**Bits 1~0:** Not used, set to "0" all the time.

### 6.1.68 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| H57 | H56 | H55 | H54 | H53 | H52 | H51 | H50 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (H57~H50):** P57~P50 high drive/sink current control bits

        0: Enable high drive/sink

        1: Disable high drive/sink (default)

### 6.1.69 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | H64 | H63 | H62 | H61 | H60 |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time.

**Bits 4~0 (H64~H60):** P64~P60 high drive/sink current control bits

        0: Enable high drive/sink

        1: Disable high drive/sink (default)

### 6.1.70   Bank 1 R10: P8HDSCR (Port 8 High Drive/Sink Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|-------|-------|
| - | - | - | - | P8HHDS | P8LHDS | - | - |
| 0 | 0 | 0 | 0 | R/W | R/W | 0 | 0 |

**Bits 7~4:** Not used, set to "0" all the time.

**Bit 3 (P8HHDS):** Control bit used to enable high drive/sink of Port 8 high nibble pin

0: Enable high drive/sink

1: Disable high drive/sink (default)

**Bit 2 (P8LHDS):** Control bit used to enable high drive/sink of Port8 low nibble pin

**Bits 1~0:** Not used, set to "0" all the time.

### 6.1.71   Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OD57 | OD56 | OD55 | OD54 | OD53 | OD52 | OD51 | OD50 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (OD57~OD50):** Open-Drain control bits

0: Disable open-drain function (default)

1: Enable open-drain function

### 6.1.72   Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | OD64 | OD63 | OD62 | OD61 | OD60 |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time.

**Bits 4~0 (OD64~OD60):** Open-Drain control bits

0: Disable open-drain function (default)

1: Enable open-drain function

### 6.1.73   Bank 1 R13: P8AODCR (Port 8 Open-Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | P8HOD | P8LOD | - | - |
| 0 | 0 | 0 | 0 | R/W | R/W | 0 | 0 |

**Bits 7~4:** Not used, set to "0" all the time.

**Bit 3 (P8HOD):** Control bit used to enable open-drain of Port 8 high nibble pin

       0: Disable open-drain function (default)

       1: Enable open-drain function

**Bit 2 (P8LOD):** Control bit used to enable open-drain of Port 8 low nibble pin

**Bits 1~0:** Not used, set to "0" all the time.

### 6.1.74   Bank 1 R14: DeadTCR (Dead Time Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | DEADTBE | DEADTAE | DEADTP1 | DEADTP0 |
| 0 | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bits 7~4:** Not used, set to "0" all the time

**Bit 3 (DEADTBE):** Enable dead-time function for PWMB and /PWMB (for dual PWM)

       0: Disable (default)

       1: Enable

**Bit 2 (DEADTAE):** Enable dead-time function for PWMA and /PWMA (for dual PWM)

       0: Disable (default)

       1: Enable

**Bits 1~0 (DEADTP1~DEADTP0):** Dead-time prescaler

| DEADTP1 | DEADTP0 | Prescaler |
|---------|---------|-----------|
| 0 | 0 | 1:1 (default) |
| 0 | 1 | 1:2 |
| 1 | 0 | 1:4 |
| 1 | 1 | 1:8 |

**NOTE**

*The deadtime function is only for dual PWM. If using a single PWM function (not dual PWM), the deadtime function is always disabled.*

### 6.1.75   Bank 1 R15: DeadTR (Dead Time Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DEADTR7 | DEADTR6 | DEADTR5 | DEADTR4 | DEADTR3 | DEADTR2 | DEADTR1 | DEADTR0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (DEADTR7~0):** The contents of the register are dead-time

### 6.1.76   Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | DEADS | - | - | PWMBS | PWMAS |
| 0 | 0 | 0 | R/W | 0 | 0 | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time.

**Bit 4 (DEADS):** Clock selection for dead time timer

> 0: Fs (default)

> 1: Fm

**Bits 3~2:** Not used, set to "0" all the time.

**Bit 1 (PWMBS):** Clock selection for PWMB timer

> 0: Fs (default)

> 1: Fm

**Bit 0 (PWMAS):** Clock selection for PWMA timer

> 0: Fs (default)

> 1: Fm

### 6.1.77   Bank 1 R17: PWMACR (PWMA Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PWMAE | IPWMAE | PWMAA | IPWMAA | TAEN | TAP2 | TAP1 | TAP0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (PWMAE):** PWMA enable bit

    0: Disable (default)

    1: Enable. The compound pin is used as PWMA pin

**Bit 6 (IPWMAE):** Inverse PWMA enable bit

    0: Disable (default)

    1: Enable. The compound pin is used as /PWMA pin

**Bit 5 (PWMAA):** Active level of PWMA

    0: duty -deadtime is Logic 1 (default)

    1: duty is-deadtime is Logic 0

**Bit 4 (IPWMAA):** active level of inverse PWMA

    0: period-duty-deadtime is Logic 1 (default)

    1: period-duty-deadtime is Logic 0

**Bit 3 (TAEN):** TMRA enable bit. All PWM functions are valid only as this bit is set

    0 = TMRA is off (default)

    1 = TMRA is on

| PWMxE | TxEN | Function Description |
|-------|------|----------------------|
| *0* | *0* | *Not used as PWM function; I/O pin or other function pin.* |
| *0* | *1* | *Timer function; I/O pin or other function pin.* |
| *1* | *0* | *PWM function, the waveform keeps at inactive level.* |
| *1* | *1* | *PWM function, the normal PWM output waveform.* |

*\*x = A, B

**Bits 2~0 (TAP2~TAP0):** TMRA clock prescaler option bits

| TAP2 | TAP1 | TAP0 | Prescaler |
|------|------|------|-----------|
| 0 | 0 | 0 | 1:1 (default) |
| 0 | 0 | 1 | 1:2 |
| 0 | 1 | 0 | 1:4 |
| 0 | 1 | 1 | 1:8 |
| 1 | 0 | 0 | 1:16 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

### 6.1.78   Bank 1 R18: PRDAL (Low Byte of PWMA Period)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PRDA7 | PRDA6 | PRDA5 | PRDA4 | PRDA3 | PRDA2 | PRDA1 | PRDA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (PRDA7~ PRDA 0):** The contents of the register are low byte of the PWMA period.

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**NOTE**

*The PWMA duty/period is reloaded when PRDAL register is updated.*

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### 6.1.79   Bank 1 R19: PRDAH (High Byte of PWMA Period)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | PRDA9 | PRDA8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~0 (PRDA9~ PRDA 8):** The contents of the register are high byte of PWMA period

### 6.1.80   Bank 1 R1A: DTAL (Low Byte of PMWA Duty)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DTA7 | DTA6 | DTA5 | DTA4 | DTA3 | DTA2 | DTA1 | DTA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (DTA7~ DTA0):** The contents of the register are low byte of the PWMA duty

### 6.1.81    Bank 1 R1B: DTAH (High Byte of PMWA Duty)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | DTA9 | DTA8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~0 (DTA9~ DTA 8):** The contents of the register are high byte of the PWMA duty

### 6.1.82    Bank 1 R1C: TMRAL (Low Byte of Timer A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TMRA7 | TMRA6 | TMRA5 | TMRA4 | TMRA3 | TMRA2 | TMRA1 | TMRA0 |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (TMRA7~ TMRA 0):** The contents of the register are low byte of the PWMA timer which is counting. This is read-only.

### 6.1.83    Bank 1 R1D: TMRAH (High byte of Timer A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | TMRA9 | TMRA8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R | R |

**Bits 7~0 (TMRA9~ TMRA 8):** The contents of the register are high byte of the PWMA timer which is counting. This is read-only.

### 6.1.84    Bank 1 R1E: PWMBCR (PWMB Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PWMBE | IPWMBE | PWMBA | IPWMBA | TBEN | TBP2 | TBP1 | TBP0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (PWMBE):** PWMB enable bit

>   0: Disable (default)

>   1: Enable. The compound pin is used as PWMB pin

**Bit 6 (IPWMBE):** Inverse PWMB enable bit

>   0: Disable (default)

>   1: Enable. The compound pin is used as /PWMB pin

**Bit 5 (PWMBA):** Active level of PWMB

>   0: duty is Logic 1 (default)

>   1: duty is Logic 0

**Bit 4 (IPWMBA):** Active level of inverse PWMB

> 0: period-duty is Logic 1 (default)

> 1: period-duty is Logic 0

**Bit 3 (TBEN):** TMRB enable bit. All PWM functions are valid only as this bit is set

> 0: TMRB is off (default)

> 1: TMRB is on

**Bits 2~0 (TBP2~TBP0):** TMRB clock prescaler option bits

| TBP2 | TBP1 | TBP0 | Prescaler |
|------|------|------|-------------|
| 0 | 0 | 0 | 1:1 (default) |
| 0 | 0 | 1 | 1:2 |
| 0 | 1 | 0 | 1:4 |
| 0 | 1 | 1 | 1:8 |
| 1 | 0 | 0 | 1:16 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

## 6.1.85   Bank 1 R1F: PRDBL (Low Byte of PWMB Period)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PRDB7 | PRDB6 | PRDB5 | PRDB4 | PRDB3 | PRDB2 | PRDB1 | PRDB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (PRDB7~ PRDB 0):** The contents of the register are low bytes of the PWMB period.

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**NOTE**
*The PWMB duty/period be reloaded when PRDBL register update.*

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## 6.1.86   Bank 1 R20: PRDBH (High Byte of PWMB period)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | PRDB9 | PRDB8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~0 (PRDB9~ PRDB 8):** The contents of the register are high bytes of PWMB period.

### 6.1.87    Bank 1 R21: DTBL (Low Byte of PMWB Duty)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DTB7 | DTB6 | DTB5 | DTB4 | DTB3 | DTB2 | DTB1 | DTB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (DTB7~ DTB 0):** The contents of the register are low byte of the PWMB duty

### 6.1.88    Bank 1 R22: DTBH (High Byte of PMWB Duty)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | DTB9 | DTB8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~0 (DTB9~ DTB 8):** The contents of the register are high byte of the PWMB duty

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**NOTE**

*The value in the dead-time register must be less than the value in the duty cycle register in order to prevent unexpected behavior on both of the PWM outputs.*

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### 6.1.89    Bank 1 R23: TMRBL (Low Byte of Timer B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TMRB7 | TMRB6 | TMRB5 | TMRB4 | TMRB3 | TMRB2 | TMRB1 | TMRB0 |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (TMRB7~ TMRB 0):** The contents of the register are low byte of the PWMB timer which is counting. This is read-only.

### 6.1.90    Bank 1 R24: TMRBH (High Byte of Timer B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | TMRB9 | TMRB8 |
| 0 | 0 | 0 | 0 | 0 | 0 | R | R |

**Bits 7~0 (TMRB9~ TMRB 8):** The contents of the register are high byte of the PWMB timer which is counting. This is read-only

### 6.1.91    Bank 1 R25 ~ R39: (Reserved)

### 6.1.92   Bank 1 R40: WCR and EECR1 (Watch Timer and EEPROM Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|--------|-------|-------|-------|-------|-------|
| WTE | WTSSB1 | WTSSB0 | - | - | - | - | - |
| R/W | R/W | R/W | 0 | 0 | 0 | 0 | 0 |

**Bit 7 (WTE):** Watch Timer Enable Bit

    0: Disable

    1: Enable

**Bits 6~5 (WTSSB1~WTSSB0):** Watch Timer Interval Select Bits

| WTSSB1 | WTSSB0 | Timer Interval Select | Timer Interval Select (LXT3 = 32.768kHz) |
|--------|--------|-----------------------|-------------------------------------------|
| 0 | 0 | 32768 / Fs | 1.0s |
| 0 | 1 | 16384 / Fs | 0.5s |
| 1 | 0 | 8192 / Fs | 0.25s |
| 1 | 1 | 128 / Fs | 3.91ms |

**Note:** *The clock source of the watch timer comes from the sub-IRC or crystal 32.768kHz.*

**Bits 4~0:** unused bit, set to 0 all the time

### 6.1.93   Bank 1 R41~R43: (Reserved)

### 6.1.94   Bank 1 R44: FLKR (Flash Key Register for Table Write Use)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|--------|-------|-------|-------|-------|-------|
| FLK[7] | FLK[6] | FLK[5] | FLK[4] | FLK[3] | FLK[2] | FLK[1] | FLK[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This FLKR register is used by table write IAP mode operation. The IAP enable signal is generated when a specific value is written into this register, e.g., **0xB4**. The register is designed to make sure that IAP operation occurs for flash update.

### 6.1.95   Bank 1 R45: TBPTL (Table Point Low Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|--------|-------|-------|-------|-------|-------|
| TB7 | TB6 | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TB7~TB0):** Table Point Address Bits 7~0.

### 6.1.96 Bank 1 R46: TBPTH (Table Point High Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| HLB | RDS | - | TB12 | TB11 | TB10 | TB9 | TB8 |
| R/W | R/W | 0 | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (HLB):** Take high byte or low byte at machine code from ROM.

| RDS | HLB | Read to Register Data Value Description |
|-----|-----|----------------------------------------|
| 0 | 0 | Read byte value is Bit 7~Bit 0 from machine code. |
| 0 | 1 | Read byte value is Highest bit fixed "0" and Bit 14~Bit 8 from machine code. |

**Bit 6 (RDS):** ROM data select bit, read machine code information select.

       0: ROM data (Must be 0 all the time)

**Bit 5:** unused bit, set to 0 all the time

**Bits 4 ~0 (TB12~TB8):** Table Point Address Bits 12~8.

### 6.1.97 Bank 1 R47: STKMON (Stack Point)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| STOV | - | - | - | STL3 | STL2 | STL1 | STL0 |
| R | 0 | 0 | 0 | R | R | R | R |

**Bit 7 (STOV):** Stack pointer overflow indication bit. Only read.

**Bits 3~0 (STL3~ STL 0):** Stack pointer number. Only read.

### 6.1.98 Bank 1 R48: PCH (Program Counter High)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | PC12 | PC11 | PC10 | PC9 | PC8 |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Not used, set to "0" all the time.

**Bits 4~0 (PC12~PC8):** The high byte of program counter.

### 6.1.99    Bank 1 R49: LVDCR (Low Voltage Detector Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LVDEN | - | LVDS1 | LVDS0 | LVDB | - | - | - |
| R/W | 0 | R/W | R/W | R | 0 | 0 | 0 |

**Bit 7 (LVDEN):** Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

**Bits 5~4 (LVDS1~LVDS0):** Low Voltage Detector Level Bits.

| LVDEN | LVDS1, LVDS0 | LVD Voltage Interrupt Level | LVDB |
|-------|--------------|-----------------------------|------|
| 1 | 11 | VDD < 2.2V | 0 |
| | | VDD > 2.4V | 1 |
| 1 | 10 | VDD < 3.3V | 0 |
| | | VDD > 3.5V | 1 |
| 1 | 01 | VDD < 4.0V | 0 |
| | | VDD > 4.2V | 1 |
| 1 | 00 | VDD < 4.5V | 0 |
| | | VDD > 4.7V | 1 |
| 0 | XX | NA | 1 |

**Bit 3 (LVDB):** Low Voltage Detector State Bit. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVDS1 ~ LVDS0), this bit will be cleared.

0: The low voltage is detected.

1: The low voltage is not detected or LVD function is disabled.

**Bits 6, 2~0:** Not used, set to "0" all the time.

### 6.1.100   Bank 1 R4D TBWCR (Table Write Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | - | IAPEN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | R/W |

**Bits 7~1:** not used bits, fixed to "0" all the time.

**Bit 0 (IAPEN):** IAP enable bit

0: IAP mode Disable

1: IAP mode Enable

### 6.1.101   Bank 1 R4E: TBWAL (Table Write Start Address Low Byte)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TBWA[7] | TBWA[6] | TBWA[5] | TBWA[4] | TBWA[3] | TBWA[2] | TBWA[1] | TBWA[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TBWA[7]~TBWA[0]):** Table Write Star Address Bits 7~0, TBWA[4]~TBWA[0] always fixed to "0".

### 6.1.102   Bank 1 R4F: TBWAH (Table Write Start Address High Byte)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | TBWA[12] | TBWA[11] | TBWA[10] | TBWA[9] | TBWA[8] |
| 0 | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bits 7~5:** Fixed to "0" all the time ( Read only)

**Bits 4~0 (TBWA[12]~TBWA[8]):** Table Write Address Bits 12~8.

※**Note** :

| ROM Code Buffer (Start) | Table Write ROM Address (Destination) |
|-------------------------|---------------------------------------|
| BANK1 0x80 | [TBWA] Low byte (Bits 7~0) |
| BANK1 0x81 | [TBWA] High byte (Bits 14~8) |
| BANK1 0x82 | [TBWA+1] Low byte (Bits 7~0) |
| BANK1 0x83 | [TBWA+1] High byte (Bits 14~8) |
| ⋮ | ⋮ |
| BANK1 0XBE | [TBWA+31] Low byte (Bits 7~0) |
| BANK1 0XBF | [TBWA+31] High byte (Bits 14~8) |

### 6.1.103   Bank 2 R5 TPEPCR1 (Touch Key Group A Enable Pin Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPAEP8 | TPAEP7 | TPAEP6 | TPAEP5 | TPAEP4 | TPAEP3 | TPAEP2 | TPAEP1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (TPAEP8):** Touch Key Enable Pin Control Bit

0: TPS8 function pin disable

1: TPS8 function pin enable

**Bit 6 (TPAEP7):** Touch Key Enable Pin Control Bit

> 0: TPS7 function pin disable

> 1: TPS7 function pin enable

**Bit 5 (TPAEP6):** Touch Key Enable Pin Control Bit

> 0: TPS6 function pin disable

> 1: TPS6 function pin enable

**Bit 4 (TPAEP5):** Touch Key Enable Pin Control Bit

> 0: TPS5 function pin disable

> 1: TPS5 function pin enable

**Bit 3 (TPAEP4):** Touch Key Enable Pin Control Bit

> 0: TPS4 function pin disable

> 1: TPS4 function pin enable

**Bit 2 (TPAEP3):** Touch Key Enable Pin Control Bit

> 0: TPS3 function pin disable

> 1: TPS3 function pin enable

**Bit 1 (TPAEP2):** Touch Key Enable Pin Control Bit

> 0: TPS2 function pin disable

> 1: TPS2 Pad function pin enable

**Bit 0 (TPAEP1):** Touch Key Enable Pin Control Bit

> 0: TPS1 function pin disable

> 1: TPS1 function pin enable

### 6.1.104   Bank 2 R6 TPEPCR2 (Touch Key Group A Enable Pin Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | - | - | - | - | - | TPAEP10 | TPAEP9 |
| 0 | 0 | 0 | 0 | 0 | 0 | R/W | R/W |

**Bits 7~2:** Not used bits, fixed to "0" all the time.

**Bit 1 (TPAEP10):** Touch Key Enable Pin Control Bit

> 0: TPS10 function pin disable

> 1: TPS10 function pin enable

**Bit 0 (TPAEP9):** Touch Key Enable Pin Control Bit

> 0: TPS9 function pin disable

> 1: TPS9 function pin enable

### 6.1.105 Bank 2 R7 ~ R8 (Reserved)

### 6.1.106 Bank 2 R9 TPCCR (Touch Key Charge Discharge Current Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
| - | - | - | - | TPACS3 | TPACS2 | TPACS1 | TPACS0 |
| 0 | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bits 3~0 (TPACS3~TPCACS0):** Touch Key Group A Charge Discharge Current
Source Select

| TPACS3 | TPACS2 | TPACS1 | TPACS0 | Current (µA) |
|--------|--------|--------|--------|--------------|
| 0 | 0 | 0 | 0 | 4 |
| 0 | 0 | 0 | 1 | 6 |
| 0 | 0 | 1 | 0 | 8 |
| 0 | 0 | 1 | 1 | 10 |
| 0 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 1 | 14 |
| 0 | 1 | 1 | 0 | 16 |
| 0 | 1 | 1 | 1 | 18 |
| 1 | 0 | 0 | 0 | 20 |
| 1 | 0 | 0 | 1 | 22 |

| TPACS3 | TPACS2 | TPACS1 | TPACS0 | Current (µA) |
|--------|--------|--------|--------|--------------|
| 1 | 0 | 1 | 0 | 24 |
| 1 | 0 | 1 | 1 | 26 |
| 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 0 | 1 | 30 |
| 1 | 1 | 1 | 0 | 32 |
| 1 | 1 | 1 | 1 | 34 |

*x = A, B

### 6.1.107 Bank 2 RA TPCR1 (Touch Key Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
| - | - | - | - | TPASW3 | TPASW2 | TPASW1 | TPASW0 |
| 0 | 0 | 0 | 0 | R/W | R/W | R/W | R/W |

**Bits 7~4:** Not used bits, fixed to "0" all the time.

**Bits 3~0 (TPASW3~ TPASW0):** Touch Key Group A Switch bits

| TPASW3 | TPASW2 | TPASW1 | TPASW0 | Function |
|--------|--------|--------|--------|----------|
| 0 | 0 | 0 | 0 | TPS1 On, Other TPSx un-select |
| 0 | 0 | 0 | 1 | TPS2 On, Other TPSx un-select |
| 0 | 0 | 1 | 0 | TPS3 On, Other TPSx un-select |
| 0 | 0 | 1 | 1 | TPS4 On, Other TPSx un-select |
| 0 | 1 | 0 | 0 | TPS5 On, Other TPSx un-select |
| 0 | 1 | 0 | 1 | TPS6 On, Other TPSx un-select |
| 0 | 1 | 1 | 0 | TPS7 On, Other TPSx un-select |
| 0 | 1 | 1 | 1 | TPS8 On, Other TPSx un-select |
| 1 | 0 | 0 | 0 | TPS9 On, Other TPSx un-select |
| 1 | 0 | 0 | 1 | TPS10 On, Other TPSx un-select |
| 1 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | X |
| 1 | 1 | 0 | 1 | X |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | TPS reference basis capacitor on |

Whenever TPSx is selected, it will auto be set to input pin. The original pin set option will be stored. Until the other TPSx is selected or TPAEN select is disabled, this pin will auto reload the previous set condition.

### 6.1.108 Bank 2 RB TPCR2 (Touch Key Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | TPAEN | TPDS1 | TPDS0 | TPR3 | TPR2 | TPR1 | TPR0 |
| 0 | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bit 7:** Not used bits, fixed to "0" all the time.

0: Disable

1: Enable

**Bit 6 (TPAEN):** Touch Key Group A Module Enable Bit

0: Disable

1: Enable

**Bits 5~4 (TPDS1~TPDS0):** Touch Key Read Time Multiplier Select Bits

| TPDS1 | TPDS0 | Read Time |
|-------|-------|-----------|
| 0 | 0 | x2 |
| 0 | 1 | x4 |
| 1 | 0 | x8 |
| 1 | 1 | x16 |

**Bits 3~0 (TPR3~TPR0):** Touch Key Read Time Select Bits.

| TPR3 | TPR2 | TPR1 | TPR0 | Read Time |
|------|------|------|------|-----------|
| 0 | 0 | 0 | 0 | 16 |
| 0 | 0 | 0 | 1 | 1 (Default) |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

### 6.1.109  Bank 2 RC TPCR3 (Touch Key Control Register 3)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|-------|-------|-------|-------|
| TPS | - | - | TPARTH | TPISE | TPMCE | TPWT1 | TPWT0 |
| R/W | 0 | 0 | R/W | R/W | R/W | R/W | R/W |

**Bit 7 (TPS):** Touch Key Conversion Start Bit

> 0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

> 1: Start the conversion

**Bits 6~5:** Not used, set to "0" all the time.

**Bit 4 (TPARTH):** TPA relaxation oscillator threshold voltage select.

> 0: Narrow range

> 1: Wide range

**Bit 3 (TPISE):** Touch Key idle with scan mode enable bit, for low consumption application.

> 0: Disable

> 1: Enable, Touch Key auto scan for sleep mode condition.

**Bit 2 (TPMCE):** Touch Key multi-pin enable bit. (Suggest for TK idle with scan mode Application)

> 0: Disable

> 1: Enable, Touch Key Group pin combine together.

**Bits 1~0 (TPWT1~TPWT0):** Touch Key Idle with scan mode auto wakeup time.

| TPWT1 | TPWT0 | Auto Wakeup Time |
|-------|-------|------------------|
| 0 | 0 | 100ms |
| 0 | 1 | 200ms |
| 1 | 0 | 500ms |
| 1 | 1 | 1s |

### 6.1.110 Bank 2 RD TPAHTH (Most Significant Byte of Group A High Wakeup Threshold)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPATH[15] | TPATH[14] | TPATH[13] | TPATH[12] | TPATH[11] | TPATH[10] | TPATH[9] | TPATH[8] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TPATH[15]~TPATH[8]):** Most Significant Byte of Group A high limit Wakeup threshold.

Wakeup, when sensing value is above threshold high limit value.

### 6.1.111 Bank 2 RE TPAHTL (Least Significant Byte of Group A High Wakeup Threshold)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPATH[7] | TPATH[6] | TPATH[5] | TPATH[4] | TPATH[3] | TPATH[2] | TPATH[1] | TPATH[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TPATH[7]~TPATH[0]):** Least Significant Byte of Group A high limit Wakeup threshold.

Wakes up when sensing value is above the threshold high limit value.

### 6.1.112 Bank 2 RF TPALTH (Most Significant Byte of Group A Lower Wakeup Threshold)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPATL[15] | TPATL[14] | TPATL[13] | TPATL[12] | TPATL[11] | TPATL[10] | TPATL[9] | TPATL[8] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TPATL[15]~TPATL[8]):** Most Significant Byte of Group A low limit Wakeup threshold.

Wakeup, when sensing value is below the threshold low limit value.

### 6.1.113 Bank 2 R10 TPALTL (Least Significant Byte of Group A Lower Wakeup Threshold)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPATL[7] | TPATL[6] | TPATL[5] | TPATL[4] | TPATL[3] | TPATL[2] | TPATL[1] | TPATL[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TPATL[7]~TPATL[0]):** Least Significant Byte of Group A low limit Wakeup threshold.

Wakeup, when sensing value is below the threshold low limit value.

### 6.1.114 Bank 2 R15 TPAH (Most Significant Byte of A Group Touch Key Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPA[15] | TPA[14] | TPA[13] | TPA[12] | TPA[11] | TPA[10] | TPA[9] | TPA[8] |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (TPA [15]~TPA[8]):** Most Significant Byte of A Group Touch Key Buffer.

### 6.1.115 Bank 2 R16 TPAL (Least Significant Byte of A Group Touch Key Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPA[7] | TPA[6] | TPA[5] | TPA[4] | TPA[3] | TPA[2] | TPA[1] | TPA[0] |
| R | R | R | R | R | R | R | R |

**Bits 7~0 (TPA[7]~TPA[0]):** Least Significant Byte of A Group Touch Key Buffer.

### 6.1.116 Bank 2 R19 TPSTH (Most Significant Byte of Sense Time)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPST[15] | TPST[14] | TPST[13] | TPST[12] | TPST [11] | TPST[10] | TPST[9] | TPST[8] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (TPST[15]~TPST[8]):** Most Significant Byte of the maximum sense time.

### 6.1.117 Bank 2 R1A TPSTL (Least Significant Byte of Sense Time)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TPST[7] | TPST[6] | TPST[5] | TPST[4] | TPST[3] | TPST[2] | TPST[1] | TPST[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

**Bits 7~0 (TPST [7]~TPST[0]):** Least Significant Byte of the maximum sense time.

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**NOTE**

*Bit 0 (TPST[0]): This is a read only bit, set to "1" all the time.*

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### 6.1.118 Bank 2 R1B~R46: (Reserved)

### 6.1.119   Bank 2 R47 LOCKPR (Lock Page Number Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LOCKPR7 | LOCKPR6 | LOCKPR5 | LOCKPR4 | LOCKPR3 | LOCKPR2 | LOCKPR1 | LOCKPR0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Bits 7~0 (LOCKPR7~ LOCKPR0):** Lock Page Number

### 6.1.120   Bank 2 R48 LOCKCR (Lock Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LOCKEN | - | - | - | - | - | - | - |
| R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7 (LOCKEN):** Enhanced Protect Control Bit

        0: Disable (Default)

        1: Enable

**Bits 6~0:** Not used, set to "0" all the time.

### 6.1.121   R50~R7F, Banks 0~3 R80~RFF

All of these are 8-bit general-purpose registers.

## 6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (6.1.29Bank 0 R22) are used to determine the ratio of the prescaler of TCC. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (6.1.28Bank 0 R21) are used to determine the prescaler of WDT. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-4 depicts the circuit diagram of TCC/WDT.

TCCD (6.1.30Bank 0 R23) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (keep in High or low level) must greater than 1CLK.

**If TCC signal source is from internal clock, the TCC will stop running when sleep mode occurs.**

**If TCC signal source is from external clock, TCC will increase by 1 at every falling edge or rising edge of the TCC pin when sleep mode occurs.**

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of WDTCR (6.1.28Bank 0 R21) register. With no prescaler, the WDT time-out period is approximately 16.5 ms[1] (one oscillator start-up timer period).

---

[1] **Note:** *VDD=5V, WDT time-out period = 16.5ms ± 5%.*
*VDD=3V, WDT time-out period = 16.5ms ± 5%.*
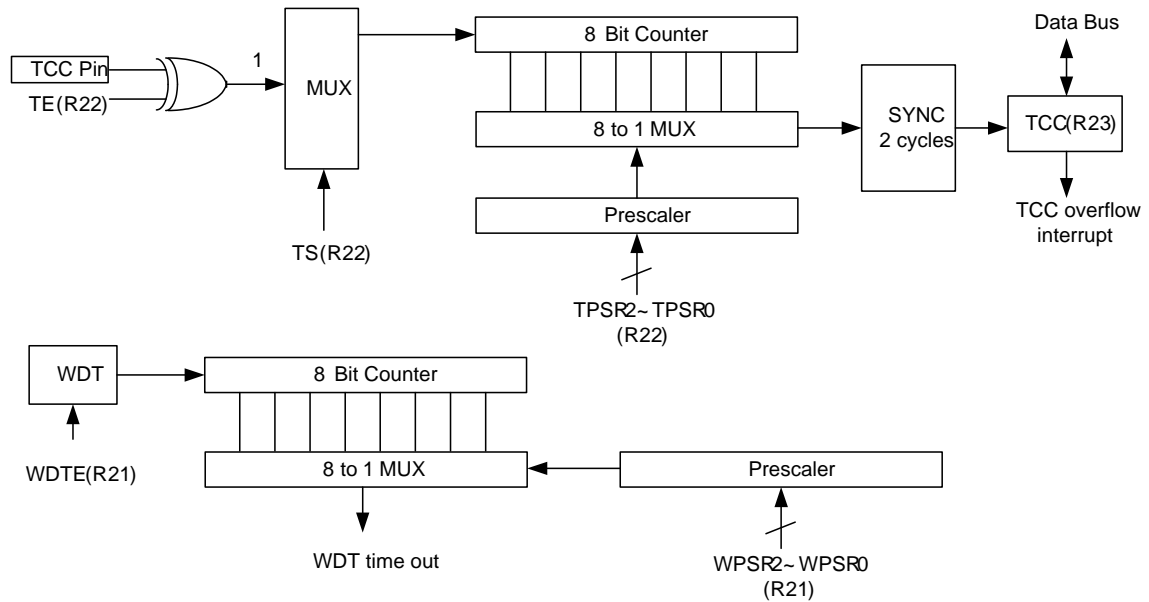
*Figure 6-4   Block Diagram of TCC and WDT*

## 6.3   I/O Ports

The I/O registers, Port 5~Port 8 are bi-directional tri-state I/O ports. All can be pulled high and pulled low internally by software. In addition, they can also have open-drain output and high sink/drive setting by software. Port 5~8 have wake up and interrupt function. Further, Ports 5~8 also have input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 is shown in the following Figure 6-5, Figure 6-6, Figure 6-7, and Figure 6-8.
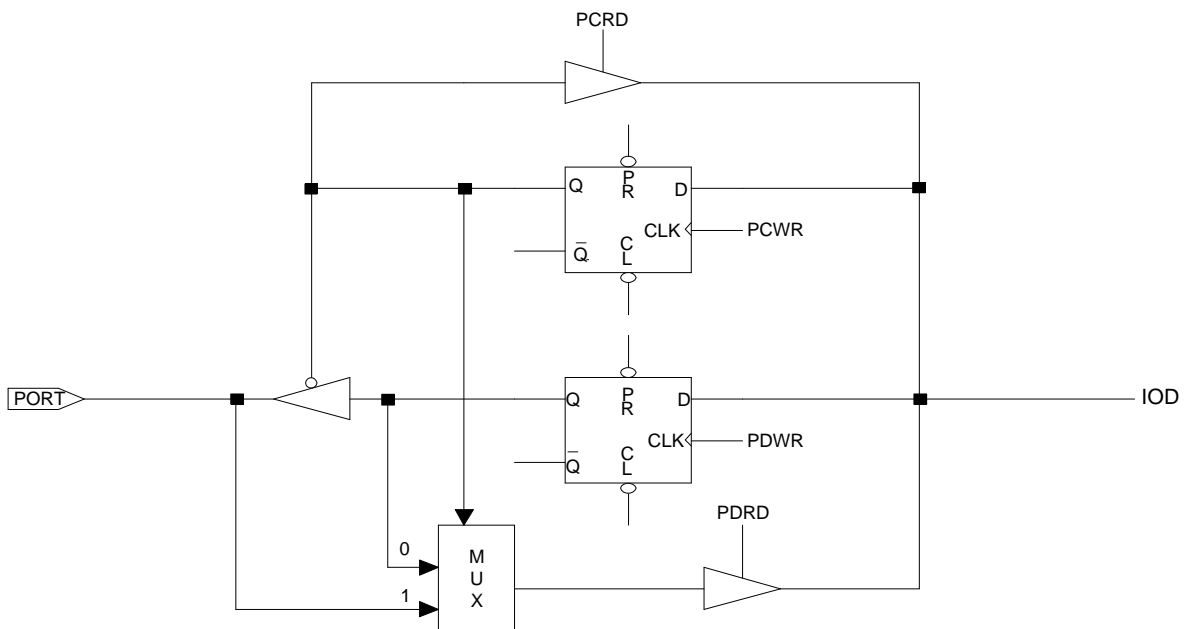


**Note**: Pull-down is not shown in the figure.

*Figure 6-5   Circuit of I/O Port and I/O Control Register for Ports 5~8*
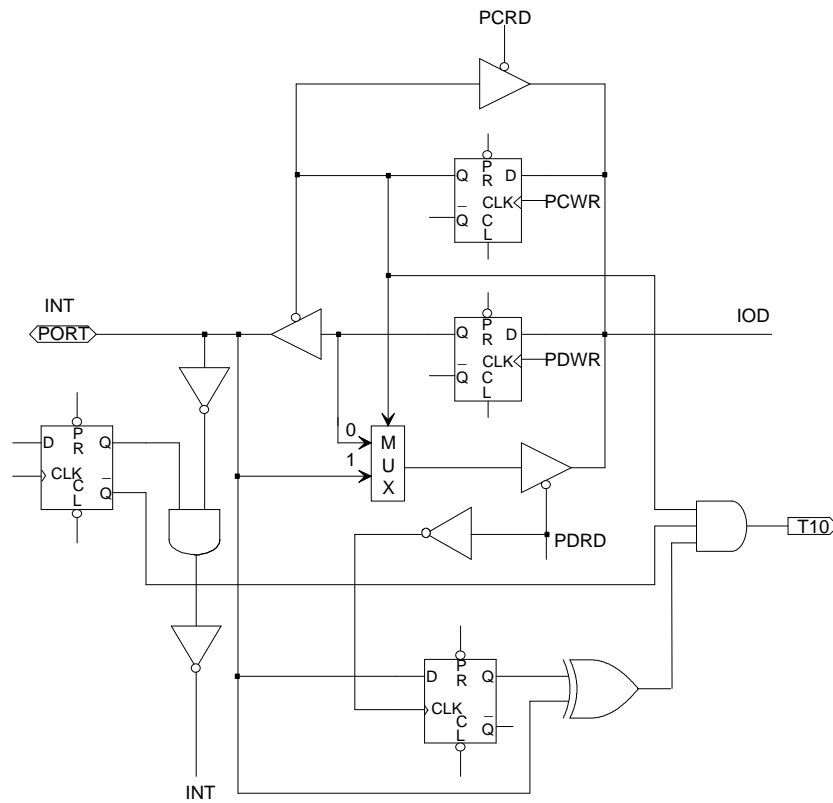
*Note: Pull-high (down) and Open-drain are not shown in the figure.*

*Figure 6-6   Circuit of I/O Port and I/O Control Register for /INT*
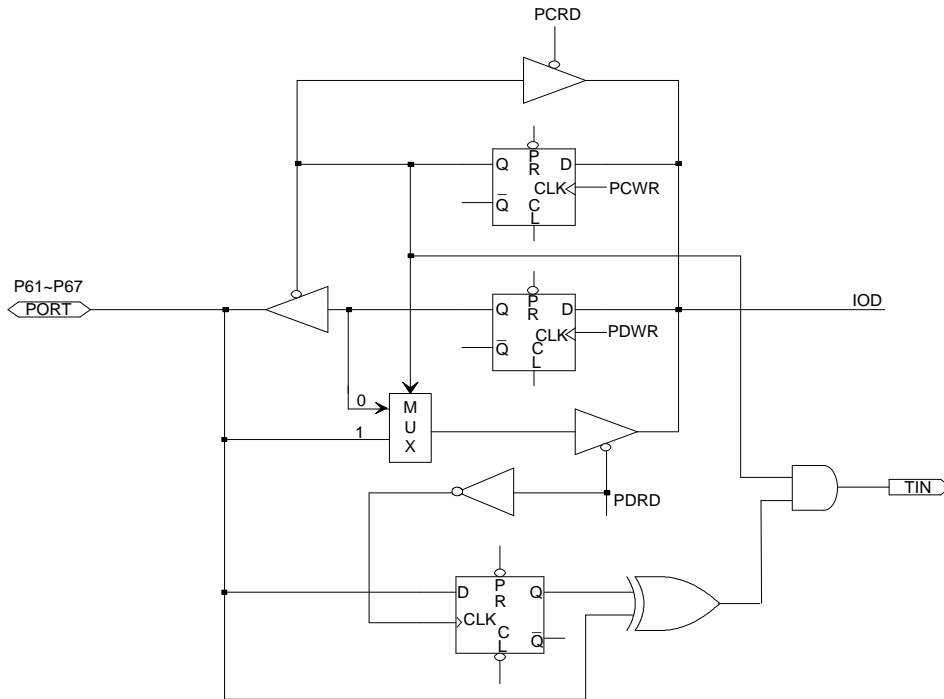
*Note: Pull-high (down) and Open-drain are not shown in the figure.*

*Figure 6-7   Circuit of I/O Port and I/O Control Register for Port 5~8*
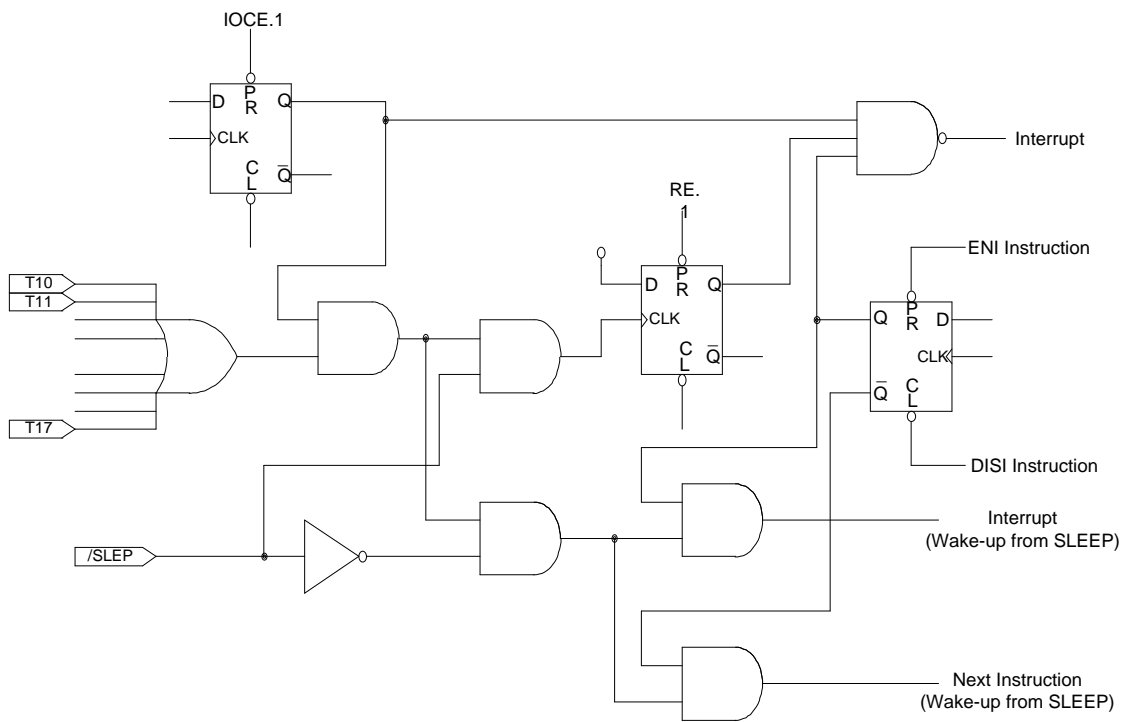
*Figure 6-8   Block Diagram of I/O Ports 5~8 with Input Change Interrupt/Wake-up*

**Table 2   Usage of Ports 5~8 Input Changed Wake-up/Interrupt Function**

| Usage of Ports 5~8 Input Status Changed Wake-up/Interrupt | |
|---|---|
| (I) Wake-up | (II) Wake-up and interrupt |
| (a) Before SLEEP | (a) Before SLEEP |
|   1. Disable WDT |   1. Disable WDT |
|   2. Read I/O Port  (MOV R6,R6) |   2. Read I/O Port (MOV R6,R6) |
|   3. Execute "ENI" or "DISI" |   3. Execute "ENI" or "DISI" |
|   4. Enable wake-up bit (Set ICWKPx*=1) <br> *x = 8~5 |   4. Enable wake-up bit (Set ICWKPx*=1) <br> *x = 8~5 |
|   5. Execute "SLEP" instruction |   5. Enable interrupt (Set ICIE =1) |
| (b) After wake-up |   6. Execute "SLEP" instruction |
| → Next instruction | (b) After wake-up |
| |   1. IF "ENI" → Interrupt vector (0004H) |
| |   2. IF "DISI" → Next instruction |

## 6.4 Reset and Wake-up

### 6.4.1 Reset

A Reset is initiated by one of the following events-

(1) Power on reset.

(2) /RESET pin input "low"

(3) WDT time-out (if enabled).

(4) LVR (if enabled).

(5) Software Reset (instruction "RESET")

The device is kept in a RESET condition for a period of approx. 16ms[2] (one oscillator start-up timer period) after the reset is detected. If the /Reset pin goes "low" or WDT time-out is active, a reset is generated, in IRC mode the reset time is WSTO and 8/32 clocks, High XTAL mode reset time is WSTO and 510 clocks. In Low XTAL mode, the reset time is WSTO and 510 clocks (Fs). Once a RESET occurs, the following functions are performed.
Refer to Figure 6-9.

- The oscillator is running, or will be started.

- The Program Counter (R2) is set to all "0".

- All I/O port pins are configured as input mode (high-impedance state).

- The Watchdog timer and prescaler are cleared.

- The bits of the control register are set in Table 3.

The sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up is generated, in IRC mode the wake-up time is WSTO and 8/32 clocks. , High XTAL mode wake-up time is WSTO and 510 clocks. In low XTAL mode, the wake-up time is WSTO and 510 clocks (Fs).The controller can be awakened by :

(1)     External reset input on /RESET pin,

(2)     WDT time-out (if enabled).

(3)     External (/INT) pin changes (if INTWE is enabled).

(4)     Port input status changes (if ICWKPx is enabled).

(5)     I2C received data when I2C act as slave device (if I2CWK is enabled)

---

[2] NOTE:  Vdd = 5V, Temp=-40~85℃,WDT time-out period = 16.5ms ± 5%
Vdd = 3V, Temp=-40~85℃,WDT time-out period = 16.5ms ± 5%

(6)    A/D conversion completed (if ADWK is enabled).

(7)    TCC Counter mode overflow occur.(if TCIE is enable)

The first two cases will cause the EM88F752N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3~7 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x02~0x40 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Only one of the Cases 3 to 7 can be enabled before entering into sleep mode. That is,

**[a]**  If WDT is enabled before SLEP, the EM88F752N can be wake-up only by Case 1 or Case 2. Refer to the section on Interrupt for further details.

**[b]**  If External (/INT0, /INT1) pin change is used to wake-up EM88F752N and EXWE bit is enabled before SLEP, WDT must be disabled. Hence, the EM88F752N can be wake-up only by Case 3.

**[c]**  If Port Input Status Change is used to wake-up EM88F752N and corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM88F752N can be wake-up only by Case 4.

**[d]**  When SPI act as slave device, after received data will wake-up EM88F752N and I2CWK bit of Bank 0 R11 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F752N can be wake-up only by Case 5.

**[e]**  If AD conversion completed is used to wake-up EM88F752N and ADWK bit of Bank0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F752N can be wake-up only by Case 6.

**[f]**  When TCC Counter mode use external signal overflow occur is used to wake-up EM88F752N and TCIE bit of Bank 0 R1B register is enabled before SLEP, WDT must be disabled by software. Hence, the EM88F752N can be waken-up only by Case 7.

**Table 3   All kinds of wake-up mode and interrupt mode are shown below:**

| Wake-up Signal | Condition Signal | Sleep Mode | | Idle Mode | | Green Mode | | Normal Mode | |
|---|---|---|---|---|---|---|---|---|---|
| | | DISI | ENI | DISI | ENI | DISI | ENI | DISI | ENI |
| External INT | INTWK = 0, EXIE = 0 | INT Pin Disable | | | | | | | |
| | INTWK = 0, EXIE = 1 | Wake-up is invalid | | | | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| | INTWK = 1, EXIE = 0 | INT Pin Disable | | | | | | | |
| | INTWK = 1, EXIE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| TCC INT | TCIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | TCIE = 1 | Wake up + Next Instruction (Counter mode) | Wake up + Interrupt Vector (Counter mode) | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| PWMA/B (When TimerA/B Match PRD A/B) | PWMxPIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | PWMxPIE = 1 | wake-up is invalid | | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| PWMA/B (When TimerA/B Match DT A/B) | PWMxDIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | PWMxDIE = 1 | wake-up is invalid | | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| TC1/2/3 Interrupt (Used as timer) | TC1/2/3IE = 0 | Wake-up is invalid | | Wake-up is invalid. | | Interrupt is invalid | | Interrupt is invalid | |
| | TC1/2/3IE = 1 | | | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| TC1/2/3 Interrupt (Used as counter) | TC1/2/3IE = 0 | Wake-up is invalid | | Wake-up is invalid. | | Interrupt is invalid | | Interrupt is invalid | |
| | TC1/2/3IE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| Watch Timer | WTIE = 0 | Wake-up is invalid. | | Wake-up is invalid. | | Interrupt is invalid | | Interrupt is invalid | |
| | WTIE = 1 | | | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |

| Wake-up Signal | Condition Signal | Sleep Mode | | Idle Mode | | Green Mode | | Normal Mode | |
|---|---|---|---|---|---|---|---|---|---|
| | | DISI | ENI | DISI | ENI | DISI | ENI | DISI | ENI |
| Pin Change INT | WKPxH/L = 0, PxICIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | WKPxH/L = 0, PxICIE = 1 | Wake-up is invalid | | | | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| | WKPxH/L = 1, PxICIE = 0 | Wake up + Next Instruction | | | | Interrupt is invalid | | | |
| | WKPxH/L = 1, PxICIE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| Low Voltage Detector INT | LVDWK = 0 LVDIE = 0 | Wake up is invalid | | | | Interrupt is invalid | | | |
| | LVDWK = 0 LVDIE = 1 | Wake up is invalid | | | | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| | LVDWK = 1 LVDIE = 0 | Wake up + Next Instruction | | Wake up + Next Instruction | | Interrupt is invalid | | | |
| | LVDWK = 1 LVDIE = 1 | Wake up + Next Instruction | Wake up + Next Instruction | Wake up + Next Instruction | Wake up + Next Instruction | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| AD INT | ADWK = 0, ADIE = 0 | Wake-up is invalid | | | | Interrupt is invalid | | | |
| | ADWK = 0, ADIE = 1 | Wake-up is invalid | | | | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| | ADWK = 1, ADIE = 0 | Wake up + Next Instruction **Fs and Fm don't stop** | | | | Interrupt is invalid | | | |
| | ADWK = 1, ADIE = 1 | Wake up + Next Instruction **Fs and Fm don't stop** | Wake up + Interrupt Vector **Fs and Fm don't stop** | Wake up + Next Instruction **Fs and Fm don't stop** | Wake up + Interrupt Vector **Fs and Fm don't stop** | Next Instruction | Interrupt + Interrupt Vector | Next Instruction | Interrupt + Interrupt Vector |
| I2C (Slave mode) | I2CWK = 0, I2CxIE = 0 | Wake-up is invalid | | | | I2C Cannot be used | | Interrupt is invalid | |
| | I2CWK = 0, I2CxIE = 1 | Wake-up is invalid | | | | I2C Cannot be used | | Next Instruction | Interrupt + Interrupt Vector |
| | I2CWK = 1, I2CxIE = 0 | Wake up + Next Instruction **I2C must be slave mode** | | | | I2C Cannot be used | | Interrupt is invalid | |
| | I2CWK = 1, I2CxIE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | I2C Cannot be used | | Next Instruction | Interrupt + Interrupt Vector |

| Wake-up Signal | Condition Signal | Sleep Mode | | Idle Mode | | Green Mode | | Normal Mode | |
|---|---|---|---|---|---|---|---|---|---|
| | | DISI | ENI | DISI | ENI | DISI | ENI | DISI | ENI |
| Idle with scan mode INT | TPISE = 1 TPCIE = 0 | Wake up + Next Instruction | | | | Interrupt is invalid | | | |
| | TPISE = 1 TPCIE = 1 | Wake up + Next Instruction | Wake up + Interrupt Vector | Wake up + Next Instruction | Wake up + Interrupt Vector | | | | |
| WDT Time out | | RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET |

After wake up:

1. If interrupt enable → interrupt+ next instruction

2. If interrupt disable → next instruction

## 6.4.2 Status of RST, T, and P of Status Register

A RESET condition is initiated by the following events:

1. A power-on condition,

2. A high-low-high pulse on /RESET pin

3. Watchdog timer time-out.

4. LVR occur

The values of T and P, listed in Table 4 are used to check how the processor wakes up. Table 5 shows the events that may affect the status of T and P.

**Table 4  Values of RST, T and P after RESET**

| Reset Type | T | P |
|---|---|---|
| Power on | 1 | 1 |
| /RESET during Operating mode | *P | *P |
| /RESET wake-up during SLEEP mode | 1 | 0 |
| WDT during Operating mode | 0 | *P |
| WDT wake-up during SLEEP mode | 0 | 0 |
| Wake-up on pin change during SLEEP mode | 1 | 0 |

*P: Previous status before reset

**Table 5   Status of T and P Being Affected by Events**

| Event | T | P |
|---|---|---|
| Power on | 1 | 1 |
| WDTC instruction | 1 | 1 |
| WDT time-out | 0 | *P |
| SLEP instruction | 1 | 0 |
| Wake-up on pin change during SLEEP mode | 1 | 0 |

*P: Previous value before reset
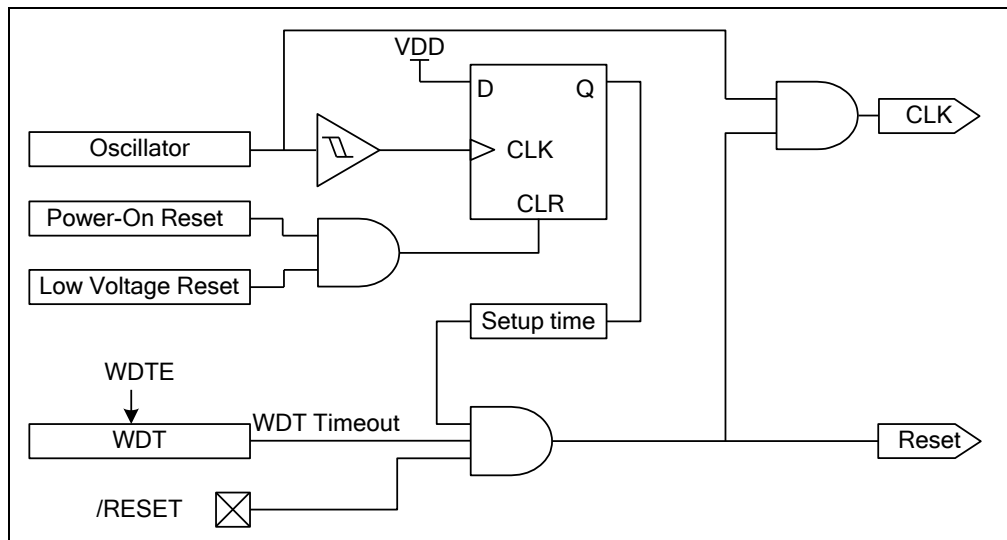


*Figure 6-9   Block Diagram of Controller Reset*

Table 6   Summary of the Initialized Values for Registers

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x00 | R0 (IAR) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-On | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0x01 | R1 (BSR) | Bit Name | - | - | SBS1 | SBS0 | - | - | GBS1 | GBS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | P | P | 0 | 0 | P | P |
| 0x02 | R2 (PCL) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0x03 | R3 (SR) | Bit Name | INT | N | OV | T | P | Z | DC | C |
| | | Power-On | 0 | U | U | 1 | 1 | U | U | U |
| | | /RESET and WDT | 0 | P | P | t | t | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | t | t | P | P | P |
| 0x04 | R4 (RSR) | Bit Name | RSR7 | RSR6 | RSR5 | RSR4 | RSR3 | RSR2 | RSR1 | RSR0 |
| | | Power-On | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X05 | Bank 0, R5 (Port 5) | Bit Name | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0x06 | Bank 0, R6 (Port 6) | Bit Name | - | - | - | P64 | P63 | P62 | P61 | P60 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x08 | Bank 0, R8 (Port 8) | Bit Name | - | - | - | P84 | P83 | P82 | P81 | P80 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0B | Bank 0, RB (IOCR5) | Bit Name | IOC57 | IOC56 | IOC55 | IOC54 | IOC53 | IOC52 | IOC51 | IOC50 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0x0C | Bank 0, RC (IOCR6) | Bit Name | - | - | - | IOC64 | IOC63 | IOC62 | IOC61 | IOC60 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0x0E | Bank 0, RE (OMCR) | Bit Name | CPUS | IDLE | - | - | - | RCM2 | RCM1 | RCM0 |
| | | Power-On | Code option (HLFS) | 1 | 0 | 0 | 0 | Code option (RCM2) | Code option (RCM1) | Code option (RCM0) |
| | | /RESET and WDT | Code option (HLFS) | 1 | 0 | 0 | 0 | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | 0 | 0 | 0 | P | P | P |
| 0X0F | Bank 0, RF EIESCR | Bit Name | - | - | - | - | EIES1 | EIES0 | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | 0 | 0 |
| 0x10 | Bank 0, R10 (WUCR1) | Bit Name | - | - | LVDWK | ADWK | INT1WK | INT0WK | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | P | P | P | P | 0 | 0 |
| 0x11 | Bank 0, R11 WUCR2 | Bit Name | - | - | - | - | - | I2CWK | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | 0 | 0 |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x12 | Bank 0, R12 WUCR3 | Bit Name | ICWKP8 | ICWKP7 | ICWKP6 | ICWKP5 | - | - | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | 0 | 0 | 0 | 0 |
| 0X14 | Bank 0, R14 SFR1 | Bit Name | - | - | LVDSF | ADSF | EXSF1 | EXSF0 | WTSF | TCSF |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | P | P | P | P | P | P |
| 0X15 | Bank 0, R15 SFR2 | Bit Name | - | - | - | - | - | TC3SF | TC2SF | TC1SF |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | P | P | P |
| 0X16 | Bank 0, R16 SFR3 | Bit Name | - | - | - | - | PWMBPSF | PWMBDSF | PWMAPSF | PWMADSF |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | P | P |
| 0X17 | Bank 0, R17 SFR4 | Bit Name | P8ICSF | - | P6ICSF | P5ICSF | - | I2CSTPSF | I2CRSF | I2CTSF |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X19 | Bank 0, R19 SFR6 | Bit Name | - | - | - | - | TPCSF | TPSESF | - | TPSF |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | 0 | P |
| 0X1B | Bank 0, R1B IMR1 | Bit Name | - | - | LVDIE | ADIE | EXIE1 | EXIE0 | WTIE | TCIE |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X1C | Bank 0, R1C IMR2 | Bit Name | - | - | - | - | - | TC3IE | TC2IE | TC1IE |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | P | P | P |
| 0X1D | Bank 0, R1D IMR3 | Bit Name | - | - | - | - | PWMBPIE | PWMBDIE | PWMAPIE | PWMADIE |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | P | P |
| 0X1E | Bank 0, R1E IMR4 | Bit Name | P8ICIE | - | P6ICIE | P5ICIE | - | I2CSTPIE | I2CRIE | I2CTIE |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X20 | Bank 0, R20 IMR6 | Bit Name | SHIE | - | - | - | TPCIE | - | TPERRIE | TPIE |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | 0 | 0 | P | 0 | P | P |
| 0X21 | Bank 0, R21 WDTCR | Bit Name | WDTE | - | - | - | PSWE | WPSR2 | WPSR1 | WPSR0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | 0 | 0 | P | P | P | P |
| 0X22 | Bank 0, R22 TCCCR | Bit Name | - | TCCS | TS | TE | PSTE | TPSR2 | TPSR1 | TPSR0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | P |
| 0X23 | Bank 0, R23 TCCD | Bit Name | TCC7 | TCC6 | TCC5 | TCC4 | TCC3 | TCC2 | TCC1 | TCC0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0X24 | Bank 0, R24 TC1CR1 | Bit Name | TC1S | TC1RC | TC1SS1 | TC1MOD | TC1FF | TC1MOS | TC1IS1 | TC1IS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X25 | Bank 0, R25 TC1CR2 | Bit Name | TC1M2 | TC1M1 | TC1M0 | TC1SS0 | TC1CK3 | TC1CK2 | TC1CK1 | TC1CK0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X26 | Bank 0, R26 TC1DA | Bit Name | TC1DA7 | TC1DA6 | TC1DA5 | TC1DA4 | TC1DA3 | TC1DA2 | TC1DA1 | TC1DA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X27 | Bank 0, R27 TC1DB | Bit Name | TC1DB7 | TC1DB6 | TC1DB5 | TC1DB4 | TC1DB3 | TC1DB2 | TC1DB1 | TC1DB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X28 | Bank 0, R28 TC2CR1 | Bit Name | TC2S | TC2RC | TC2SS1 | | TC2FF | TC2MOS | TC2IS1 | TC2IS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | 0 | P | P | P | P |
| 0X29 | Bank 0, R29 TC2CR2 | Bit Name | TC2M2 | TC2M1 | TC2M0 | TC2SS0 | TC2CK3 | TC2CK2 | TC2CK1 | TC2CK0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X2A | Bank 0, R2A TC2DA | Bit Name | TC2DA7 | TC2DA6 | TC2DA5 | TC2DA4 | TC2DA3 | TC2DA2 | TC2DA1 | TC2DA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X2B | Bank 0, R2B TC2DB | Bit Name | TC2DB7 | TC2DB6 | TC2DB5 | TC2DB4 | TC2DB3 | TC2DB2 | TC2DB1 | TC2DB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X2C | Bank 0, R2C TC3CR1 | Bit Name | TC3S | TC3RC | TC3SS1 | | TC3FF | TC3MOS | TC3IS1 | TC3IS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | 0 | P | P | P | P |
| 0X2D | Bank 0, R2D TC3CR2 | Bit Name | TC3M2 | TC3M1 | TC3M0 | TC3SS0 | TC3CK3 | TC3CK2 | TC3CK1 | TC3CK0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X2E | Bank 0, R2E TC3DA | Bit Name | TC3DA7 | TC3DA6 | TC3DA5 | TC3DA4 | TC3DA3 | TC3DA2 | TC3DA1 | TC3DA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X2F | Bank 0, R2F TC3DB | Bit Name | TC3DB7 | TC3DB6 | TC3DB5 | TC3DB4 | TC3DB3 | TC3DB2 | TC3DB1 | TC3DB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X30 | Bank 0, R30 I2CCR1 | Bit Name | Strobe/Pend | IMS | ISS | STOP | SAR_EMPTY | ACK | FULL | EMPTY |
| | | Power-On | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X31 | Bank 0, R31 I2CCR2 | Bit Name | I2CBF | GCEN | I2COPT | BBF | I2CTS2 | I2CTS1 | I2CTS0 | I2CEN |
| | | Power-On | 0 | 0 | Code option (I2COPT) | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | P | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X32 | Bank 0, R32 I2CSA | Bit Name | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | IRW |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X33 | Bank 0, R33 I2CDB | Bit Name | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X34 | Bank 0, R34 I2CDAL | Bit Name | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X35 | Bank 0, R35 I2CDAH | Bit Name | - | - | - | - | - | - | DA9 | DA8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | 0 | P | P |
| 0X3E | Bank 0, R3E ADCR1 | Bit Name | CKR2 | CKR1 | CKR0 | ADRUN | ADP | ADOM | SHS1 | SHS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X3F | Bank 0, R3F ADCR2 | Bit Name | - | VPIS2 | ADIM | ADCMS | VPIS1 | VPIS0 | VREFP | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | 0 |
| 0X40 | Bank 0, R40 ADISR | Bit Name | - | - | - | - | ADIS3 | ADIS2 | ADIS1 | ADIS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X41 | Bank 0, R41 ADER 1 | Bit Name | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X43 | Bank 0, R43 ADDL | Bit Name | ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| | | Power-On | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X44 | Bank 0, R44 ADDH | Bit Name | ADD15 | ADD14 | ADD13 | ADD12 | ADD11 | ADD10 | ADD9 | ADD8 |
| | | Power-On | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X45 | Bank 0, R45 ADCVL | Bit Name | ADCD7 | ADCD6 | ADCD5 | ADCD4 | ADCD3 | ADCD2 | ADCD1 | ADCD0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X46 | Bank 0, R46 ADCVH | Bit Name | ADCD15 | ADCD14 | ADCD13 | ADCD12 | ADCD11 | ADCD10 | ADCD9 | ADCD8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X05 | Bank 1, R5 IOCR8 | Bit Name | - | - | - | IOC84 | IOC83 | IOC82 | IOC81 | IOC80 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X08 | Bank 1, R8 P5PHCR | Bit Name | PH57 | PH56 | PH55 | PH54 | PH53 | PH52 | PH51 | PH50 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X09 | Bank 1, R9 P6PHCR | Bit Name | - | - | - | PH64 | PH63 | PH62 | PH61 | PH60 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0A | Bank 1, RA P8PHCR | Bit Name | - | - | - | - | P8HPH | P8LPH | - | - |
| | | Power-On | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | P |
| 0X0B | Bank 1, RB P5PLCR | Bit Name | PL57 | PL56 | PL55 | PL54 | PL53 | PL52 | PL51 | PL50 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0C | Bank 1, RC P6PLCR | Bit Name | - | - | - | PL64 | PL63 | PL62 | PL61 | PL60 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0D | Bank 1, RD P8PLCR | Bit Name | - | - | - | - | P8HPL | P8LPL | - | - |
| | | Power-On | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | P |
| 0X0E | Bank 1, RE P5HDSCR | Bit Name | H57 | H56 | H55 | H54 | H53 | H52 | H51 | H50 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0F | Bank 1, RF P6HDSCR | Bit Name | - | - | - | H64 | H63 | H62 | H61 | H60 |
| | | Power-On | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X10 | Bank 1, R10 P8HDSCR | Bit Name | - | - | - | - | P8HHDS | P8LHDS | - | - |
| | | Power-On | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | P |
| 0X11 | Bank 1, R11 P5ODCR | Bit Name | OD57 | OD56 | OD55 | OD54 | OD53 | OD52 | OD51 | OD50 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X12 | Bank 1, R12 P6ODCR | Bit Name | - | - | - | OD64 | OD63 | OD62 | OD61 | OD60 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X13 | Bank 1, R13 P8ODCR | Bit Name | - | - | - | - | P8HOD | P8LOD | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | P | P | P | P | P | P | P |
| 0x14 | Bank 1, R14 DeadTCR | Bit Name | - | - | - | - | DEADTP3 | DEADTP2 | DEADTP1 | DEADTP0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | P | P | P | P |
| 0x15 | Bank 1, R15 DeadTR | Bit Name | DEADTR7 | DEADTR6 | DEADTR5 | DEADTR4 | DEADTR3 | DEADTR2 | DEADTR1 | DEADTR0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X16 | Bank 1, R16 PWMSCR | Bit Name | - | - | - | DEADS | - | - | PWMBS | PWMAS |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | P | 0 | 0 | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0X17 | Bank 1, R17 PWMACR | Bit Name | PWMAE | IPWMAE | PWMAA | IPWMAA | TAEN | TAP2 | TAP1 | TAP0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X18 | Bank 1, R18 PRDAL | Bit Name | PRDA7 | PRDA6 | PRDA5 | PRDA4 | PRDA3 | PRDA2 | PRDA1 | PRDA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X19 | Bank 1, R19 PRDAH | Bit Name | PRDA15 | PRDA14 | PRDA13 | PRDA12 | PRDA11 | PRDA10 | PRDA9 | PRDA8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1A | Bank 1, R1A DTAL | Bit Name | DTA7 | DTA6 | DTA5 | DTA4 | DTA3 | DTA2 | DTA1 | DTA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1B | Bank 1, R1B DTAH | Bit Name | DTA15 | DTA14 | DTA13 | DTA12 | DTA11 | DTA10 | DTA9 | DTA8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1C | Bank 1, R1C TMRAL | Bit Name | TMRA7 | TMRA6 | TMRA5 | TMRA4 | TMRA3 | TMRA2 | TMRA1 | TMRA0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1D | Bank 1, R1D TMRAH | Bit Name | TMRA15 | TMRA14 | TMRA13 | TMRA12 | TMRA11 | TMRA10 | TMRA9 | TMRA8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X1E | Bank 1, R1E PWMBCR | Bit Name | PWMBE | IPWMBE | PWMBA | IPWMBA | TBEN | TBP2 | TBP1 | TBP0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1F | Bank 1, R1F PRDBL | Bit Name | PRDB7 | PRDB6 | PRDB5 | PRDB4 | PRDB3 | PRDB2 | PRDB1 | PRDB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X20 | Bank 1, R20 PRDBH | Bit Name | PRDB15 | PRDB14 | PRDB13 | PRDB12 | PRDB11 | PRDB10 | PRDB9 | PRDB8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X21 | Bank 1, R21 DTBL | Bit Name | DTB7 | DTB6 | DTB5 | DTB4 | DTB3 | DTB2 | DTB1 | DTB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X22 | Bank 1, R22 DTBH | Bit Name | DTB15 | DTB14 | DTB13 | DTB12 | DTB11 | DTB10 | DTB9 | DTB8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X23 | Bank 1, R23 TMRBL | Bit Name | TMRB7 | TMRB6 | TMRB5 | TMRB4 | TMRB3 | TMRB2 | TMRB1 | TMRB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X24 | Bank 1, R24 TMRBH | Bit Name | TMRB15 | TMRB14 | TMRB13 | TMRB12 | TMRB11 | TMRB10 | TMRB9 | TMRB8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X40 | Bank 1, R40 WCR | Bit Name | WTE | WTSSB1 | WTSSB0 | - | - | - | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | 0 | P | P |
| 0X44 | Bank 1, R44 FLKR | Bit Name | FLK[7] | FLK[6] | FLK[5] | FLK[4] | FLK[3] | FLK[2] | FLK[1] | FLK[0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X45 | Bank 1, R45 TBPTL | Bit Name | TB7 | TB6 | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X46 | Bank 1, R46 TBPTH | Bit Name | HLB | RDS | - | - | - | TB10 | TB9 | TB8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | 0 | P | P | P | P | P |
| 0X47 | Bank 1, R47 STKMON | Bit Name | STOV | - | - | - | STL3 | STL2 | STL1 | STL0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | 0 | 0 | P | P | P | P |
| 0X48 | Bank 1, R48 PCH | Bit Name | - | - | - | - | - | PC10 | PC9 | PC8 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | P | P | P | P | P |
| 0X49 | Bank 1, R49 LVDCR | Bit Name | LVDEN | - | LVDS1 | LVDS0 | LVDB | - | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | P | P | P | 0 | 0 | 0 |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0X4D | Bank 1, R4D TBWCR | Bit Name | - | - | - | - | - | - | - | IAPEN |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | 0 | 0 | P |
| 0X4E | Bank 1, R4E TBWAL | Bit Name | TBWA[7] | TBWA[6] | TBWA[5] | TBWA[4] | TBWA[3] | TBWA[2] | TBWA[1] | TBWA[0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X4F | Bank 1, R4F TBWAH | Bit Name | - | - | - | - | - | TBWA[10] | TBWA[9] | TBWA[8] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | P | P | P | P | P |
| 0X05 | Bank 2, R5 TPEPCR1 | Bit Name | TPAEP8 | TPAEP7 | TPAEP6 | TPAEP5 | TPAEP4 | TPAEP3 | TPAEP2 | TPAEP1 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X06 | Bank 2, R6 TPEPCR2 | Bit Name | - | - | - | - | - | - | TPAEP10 | TPAEP9 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | 0 | 0 | 0 | 0 | 0 | 0 | P | P |
| 0X09 | Bank 2, R9 TPCCR | Bit Name | - | - | - | - | TPACS3 | TPACS2 | TPACS1 | TPACS0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0A | Bank 2, RA TPCR1 | Bit Name | - | - | - | - | TPASW3 | TPASW2 | TPASW1 | TPASW0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X0B | Bank 2, RB TPCR2 | Bit Name | - | TPAEN | TPDS1 | TPDS0 | TPR3 | TPR2 | TPR1 | TPR0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0C | Bank 2, RC TPCR3 | Bit Name | TPS | - | - | TPARTH | TPISE | TPMCE | TPWT1 | TPWT0 |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | P | P | P | P | P | P |
| 0X0D | Bank 2, RD TPAHTH | Bit Name | TPATH [15] | TPATH [14] | TPATH [13] | TPATH [12] | TPATH [11] | TPATH [10] | TPATH [9] | TPATH [8] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0E | Bank 2, RE TPAHTL | Bit Name | TPATH [7] | TPATH [6] | TPATH [5] | TPATH [4] | TPATH [3] | TPATH [2] | TPATH [1] | TPATH [0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X0F | Bank 2, RF TPALTH | Bit Name | TPATL [15] | TPATL [14] | TPATL [13] | TPATL [12] | TPATL [11] | TPATL [10] | TPATL [9] | TPATL [8] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X10 | Bank 2, R10 TPALTL | Bit Name | TPATL [7] | TPATL [6] | TPATL [5] | TPATL [4] | TPATL [3] | TPATL [2] | TPATL [1] | TPATL [0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X15 | Bank 2, R15 TPAH | Bit Name | TPA[15] | TPA[14] | TPA[13] | TPA[12] | TPA[11] | TPA[10] | TPA[9] | TPA[8] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |

| Address | Bank Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X16 | Bank 2, R16 TPAL | Bit Name | TPA[7] | TPA[6] | TPA[5] | TPA[4] | TPA[3] | TPA[2] | TPA[1] | TPA[0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X19 | Bank 2, R19 TPSTH | Bit Name | TPST [15] | TPST [14] | TPST [13] | TPST [12] | TPST [11] | TPST [10] | TPST [9] | TPST [8] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X1A | Bank 2, R1A TPSTL | Bit Name | TPST [7] | TPST [6] | TPST [5] | TPST [4] | TPST [3] | TPST [2] | TPST [1] | TPST [0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | 1 |
| 0X47 | Bank 2, R47 LOCKPR | Bit Name | LOCKPR [7] | LOCKPR [6] | LOCKPR [5] | LOCKPR [4] | LOCKPR [3] | LOCKPR [2] | LOCKPR [1] | LOCKPR [0] |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | P | P | P | P | P | P | P |
| 0X48 | Bank 2, R48 LOCKCR | Bit Name | LOCKEN | - | - | - | - | - | - | - |
| | | Power-On | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-Up from Sleep/Idle | P | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*U: Unknown or don't care.   P: Previous value before reset.   C: The same with Code option   t: Check Table 6*

## 6.5 Interrupt

The EM88F752N has 21 interrupts (3 external, 17 internal) listed below:

| Interrupt Source | | Enable Condition | Int. Flag | Int. Vector | Priority |
|---|---|---|---|---|---|
| Internal/External | Reset | - | - | 0 | High 0 |
| External | INT | ENI + EXIE0=1 | EXSF0 | 2 | 1 |
| | | ENI + EXIE1=1 | EXSF1 | | |
| External | Pin Change | ENI + P5ICIE=1 | P5ICSF | 4 | 2 |
| | | ENI + P6ICIE=1 | P6ICSF | | |
| | | ENI + P7ICIE=1 | P7ICSF | | |
| | | ENI + P8ICIE=1 | P8ICSF | | |
| Internal | TCC | ENI + TCIE=1 | TCSF | 6 | 3 |
| Internal | LVD | ENI+LVDEN & LVDIE=1 | LVDSF | 8 | 4 |
| Internal | AD | ENI + ADIE=1 | ADSF | 10 | 6 |
| Internal | TC1 | ENI + TC1IE=1 | TC1SF | 12 | 7 |
| Internal | PWMPA | ENI+PWMAPIE=1 | PWMAPSF | 14 | 8 |
| Internal | PWMDA | ENI+PWMADIE=1 | PWMADSF | 16 | 9 |
| Internal | I2C Transmit | ENI+ I2CTIE | I2CTSF | 1A | 10 |
| Internal | I2C Receive | ENI+ I2CRIE | I2CRSF | 1C | 11 |
| Internal | I2C STOP | ENI+ I2CSTPIE | I2CSTPSF | 1E | 12 |
| Internal | TC2 | ENI + TC2IE=1 | TC2SF | 22 | 13 |
| Internal | PWMPB | ENI+PWMBPIE=1 | PWMBPSF | 24 | 14 |
| Internal | PWMDB | ENI+PWMBDIE=1 | PWMBDSF | 26 | 15 |
| Internal | TC3 | ENI + TC3IE=1 | TC3SF | 28 | 16 |
| Internal | Watch Timer | ENI + WTIE=1 | WTSF | 38 | 17 |
| External | System hold | ENI+SHIE | SHSF | 3A | 18 |
| Internal | Touch Key | ENI+TPIE | TPSF | 3C | 19 |
| Internal | Touch Key error | ENI+TPERRIF | TPSESF | 3E | 20 |
| Internal | Touch Key auto wakeup | ENI+TPCIE | TPCSF | 40 | 21 |

Bank 0 R14~R19 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1B~R20 is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt equipped with digital noise rejection circuit (input pulse less than **4 system clocks time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and R3 (Bits 0~6) and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3

(Bit 0~Bit 6) and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 (Bit 0~Bit 6) and R4 will be pushed back.
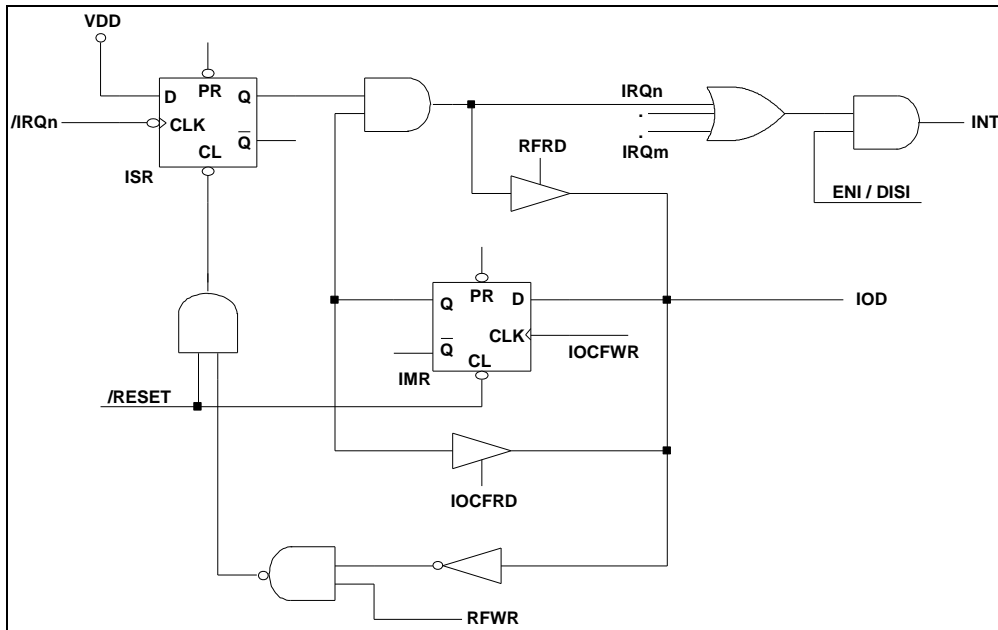


*Figure 6-10   Interrupt Input Circuit Diagram*
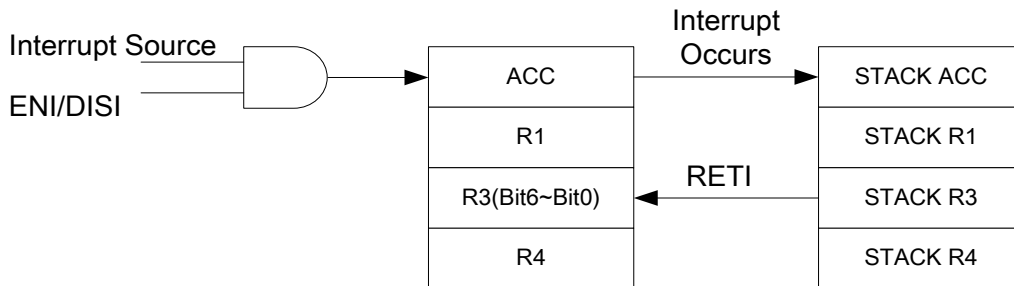


*Figure 6-11   Interrupt Backup Diagram*

## 6.6   Touch Key

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bank0 | 0x19 | SFR6 | | | | | TPCSF | TPSESF | | TPSF |
| | | | | | | | F | F | | F |
| Bank0 | 0x20 | IMR6 | | | | | TPCIE | | TPERRIE | TPIE |
| | | | | | | | R/W | | R/W | R/W |
| Bank 2 | 0x05 | TPEPCR1 | TPAEP8 | TPAEP7 | TPAEP6 | TPAEP5 | TPAEP4 | TPAEP3 | TPAEP2 | TPAEP1 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0x06 | TPEPCR2 | | | | | | | TPAEP10 | TPAEP9 |
| | | | | | | | | | R/W | R/W |
| Bank 2 | 0x09 | TPCCR | | | | | TPACS3 | TPACS2 | TPACS1 | TPACS0 |
| | | | | | | | R/W | R/W | R/W | R/W |
| Bank 2 | 0x0A | TPCR1 | | | | | TPASW3 | TPASW2 | TPASW1 | TPASW0 |
| | | | | | | | R/W | R/W | R/W | R/W |
| Bank 2 | 0x0B | TPCR2 | | TPAEN | TPDS1 | TPDS0 | TPR3 | TPR2 | TPR1 | TPR0 |
| | | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0x0C | TPCR3 | TPS | | | TPARTH | TPISE | TPMCE | TPWT1 | TPWT0 |
| | | | R/W | | | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0x0D | TPAHTH | TPATH[15:8] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x0E | TPAHTL | TPATH[7:0] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x0F | TPALTH | TPATL[15:8] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x10 | TPALTL | TPATL[7:0] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x15 | TPAH | TPAH[15:8] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x16 | TPAL | TPAH[7:0] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x19 | TPSTH | TPST[15:8] | | | | | | | |
| | | | R/W | | | | | | | |
| Bank 2 | 0x1A | TPSTL | TPST[7:1] | | | | | TPST[0] | | |
| | | | R/W | | | | | R | | |

### 6.6.1  Overview

C to F Counter is simply a counter which signal source is RC ring oscillation. User can use different capacitor sensor (pad button) and result different oscillation frequency. Then the frequency can be obtained by counting the signal. Finally the parameter we sense can be obtained by calculating the counter value in different counting mode.

### 6.6.2  Function Description

TPDS[1:0] and TPR[3:0] control the frequency detect and read time for touch key counter. The 16-bit counter is count up and counter result will be load into TPA, and then produce interrupt. If counter is overflow produce interrupt too, and TPA will be clear.

Set TPEN bit to enable the touch key function. There must be an interval of 10 µs between set TPEN and stable Bias and Bandgap. Then TPS bit can be set to begin to count and clear TPA. They were distance to TPEN, TPS and TPOUT. Refer to Figure 6-12. The 16-bit counter stops and TPS bit resets when clock overflows and generate an interrupt flag.
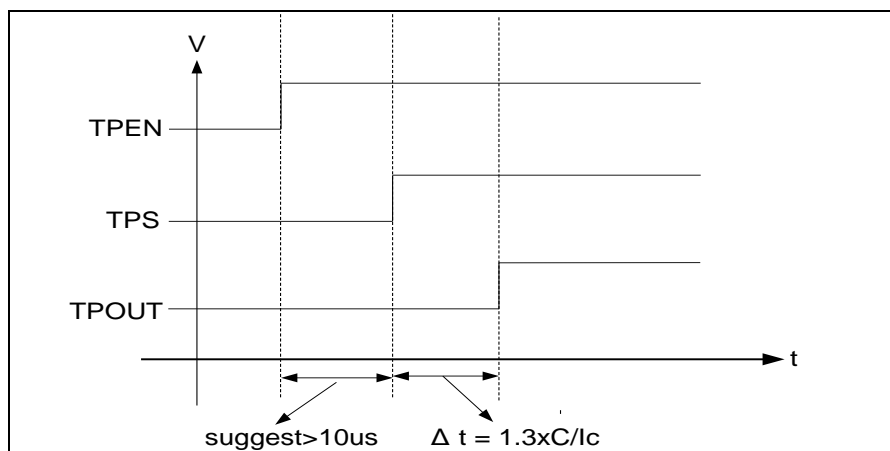


*Figure 6-12   Touch Key Operating Timing Diagram*

### 6.6.3  Normal Mode Programming

The Touch Key operates as follows:

1.  Set TPAEN to enable the touch key function.

2.  Set TPASW[3:0] and TPAEP10~TPAEP1 to select touch key sensor pin.

3.  Change TPR[3:0], TPDS[1:0] and TPACS[3:0] to select fitting TPOUT frequency.

4.  Set TPS bit to start 16-bit counter.

5.  Read TPA[15:0] value.

6.  Repeat 2~5 and then compare TPA[15:0] value.

    *The Touch key module needs 10 µs warm-up time

### 6.6.4 TK-Idle/TK-Sleep Mode Programming

The Touch Key operates as follows:

1. Set TPAEN to enable the touch key function.

2. Set TPASW[3:0] and TPAEP10~TPAEP1 to select the touch key sensor pin.

3. Change TPR[3:0], TPDS[1:0] and TPACS[3:0] to select fitting TPOUT frequency.

4. Set TPS bit to start sensing.

5. Read TPA[15:0] value, then set TPATH[15:0] and TPATL[15:0].

6. Set TPWT[1:0] to select wake-up time.

7. Set TPISE bit to enable auto-scan function

8. Execute SLEP instruction (Idle or Sleep Mode)

9. Until the TPA[15:0] value over TPATH[15:0] and TPATL[15:0], then wake-up

   *The Touch key module needs 10 μs warm-up time

## 6.7   A/D Converter

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bank 0 | 0x3E | ADCR1 | CKR2 | CKR1 | CKR0 | ADRUN | ADP | ADOM | SHS1 | SHS0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3F | ADCR2 | | VPIS2 | ADIM | ADCMS | VPIS1 | VPIS0 | VREFP | |
| | | | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Bank 0 | 0x40 | ADISR | | | | | ADIS3 | ADIS2 | ADIS1 | ADIS0 |
| | | | | | | | R/W | R/W | R/W | R/W |
| Bank 0 | 0x41 | ADER1 | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE7 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x43 | ADDL | ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x44 | ADDH | ADD15 | ADD14 | ADD13 | ADD12 | ADD11 | ADD10 | ADD9 | ADD8 |
| | | | R | R | R | R | R | R | R | R |
| Bank 0 | 0x45 | ADCVL | ADD7 | ADD6 | ADD5 | ADD4 | ADCD3 | ADCD2 | ADCD1 | ADCD0 |
| | | | R | R | R | R | R | R | R | R |

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 0 | 0x46 | ADCVH | ADCD15 | ADCD14 | ADCD13 | ADCD13 | ADCD11 | ADCD10 | ADCD9 | ADCD8 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x10 | WUCR2 | | | | ADWK | | | | |
| | | | | | | R/W | | | | |
| Bank 0 | 0x14 | SFR1 | | | | ADSF | | | | |
| | | | | | | R/W | | | | |
| Bank 0 | 0x1B | IMR1 | | | | ADIE | | | | |
| | | | | | | R/W | | | | |
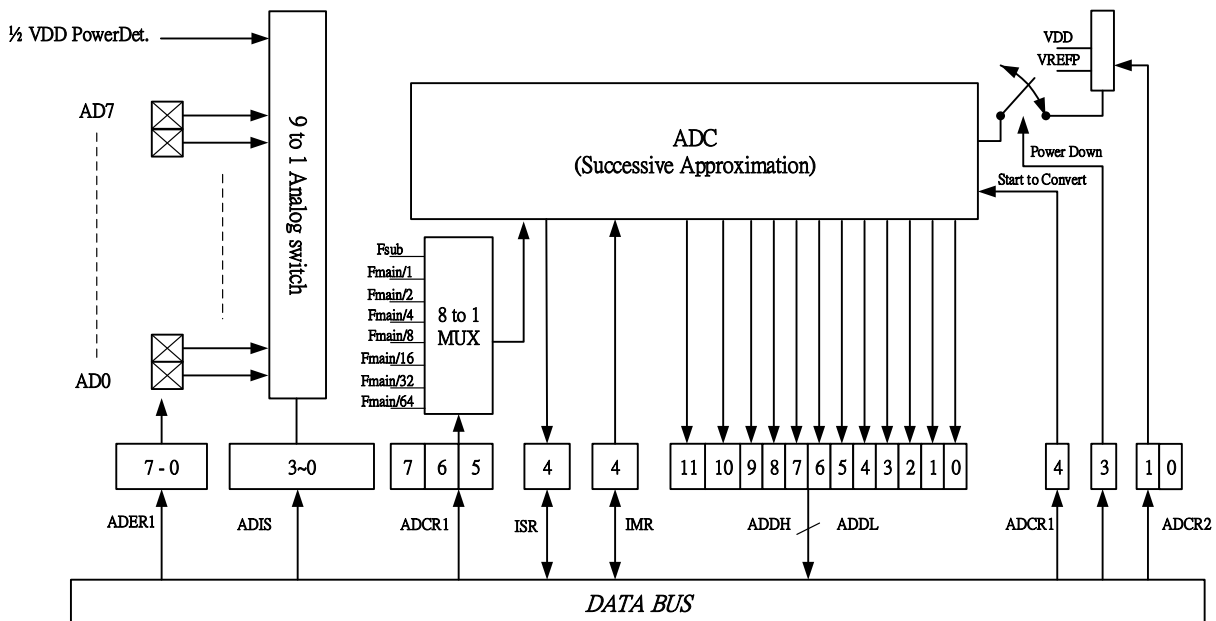


*Figure 6-13   AD Converter*

This is a 12-bit successive approximation register analog to digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFP and VPIS [1:0] bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

### 6.7.1  ADC Data Register

When the AD conversion is completed, the result is loaded to the ADDH and ADDL. And the ADSF is set if ADIE is enabled.

### 6.7.2  A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 4 µs for each kilo ohms of the analog source impedance and at least 4 µs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at VDD = 5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

### 6.7.3  A/D Conversion Time

CKR[2:0] select the conversion time ($T_{CT}$), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of AD conversion. For the EM88F752N, the conversion time per bit is about 0.5 µs. The following table shows the relationship between $T_{CT}$ and the maximum operating frequencies.

| System Mode | CKR2~0 | Clock Rate | Max. System Operation Frequency in 2.1~2.2V | Max. System Operation Frequency in 2.2~2.7V | Max. System Operation Frequency in 2.7~5V |
|---|---|---|---|---|---|
| Normal Mode | 000 | FMain/16 | 8 MHz | - | 20 MHz |
| | 001 | FMain/8 | 4 MHz | 8 MHz | 16 MHz |
| | 010 | FMain/4 | 2 MHz | 4 MHz | 8 MHz |
| | 011 | FMain/2 | 1 MHz | 2 MHz | 4 MHz |
| | 100 | FMain/64 | - | - | 20 MHz |
| | 101 | FMain/32 | - | - | 20 MHz |
| | 110 | FMain/1 | 500 kHz | 1 MHz | 2 MHz |
| | 111 | FSub | Fs | Fs | Fs |
| Green Mode | xxx | FSub | Fs | Fs | Fs |

**NOTE**

*For the system operation frequency, it's a must to refer to Table 10 of Section 6.12.*

### 6.7.4  ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TC1~3, PWMA~B timers and AD conversion.

The AD Conversion is considered completed as determined by:

1.  The ADRUN bit of the Bank 0-R3E register is cleared to "0".

2.  The ADSF bit of the Bank 0-R15 register is set to "1".

3.  The ADWK bit of the Bank 0-R10 register is set to "1". Wakes up from ADC conversion (where it remains in operation during sleep mode).

4.  Wake up and execution of the next instruction if the ADIE bit of the Bank 0-R1B is enabled and the "DISI" instruction is executed.

5.  Wake up and enters into Interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the "ENI" instruction is executed.

6.  Enters into an Interrupt vector if the ADIE bit of the Bank0-R1B is enabled and the "ENI" instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADP bit is.

### 6.7.5  Programming Process/Considerations

Follow these steps to obtain data from the ADC:

1.  Write to the sixteen bits (ADE[15:0]) on the Bank 0-R41~R42 (ADER1) register to define the characteristics of P60~P61, P63~P67 and P90~P96 (digital I/O, analog channels, or voltage reference pin)

2.  Write to the Bank 0-R3E (ADCR1) register to configure the AD module:
    a)  Select the ADC input channel (ADIS[3:0])
    b)  Define the AD conversion clock rate (CKR[2:0])
    c)  Select the VREFP input source of the ADC
    d)  Set the ADP bit to 1 to begin sampling

3.  Set the ADWK bit, if the wake-up function is employed

4.  Set the ADIE bit, if the interrupt function is employed

5.  Write "ENI" instruction, if the interrupt function is employed

6.  Set the ADRUN bit to 1

7.  Write "SLEP" instruction or Polling.

8.  Wait for wake-up or for the ADRUN bit to be cleared to "0" , status flag (ADSF) is set "1," or ADC interrupt occurs.

9.    Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to '0'.

10.   Clear the status flag (ADSF).

11.   For next conversion, go to Step 1 or Step 2 as required. At least two $T_{CT}$ is required before the next acquisition starts.

---

**NOTE**
*In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion*

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### 6.7.6  Programming Process for Detecting Internal VDD

VDD is detected within the operation, as described in the previous section the difference is that before starting the ADC conversion, the first detection of VDD is ready.  Therefore in Detecting VDD:

It should be noted that before starting the AD conversion operation, the channel has to be switched to 1/2VDD channel, the voltage divider is started, then AD can be converted.  Several points to note is that, precise conversion values can be added in the VDD Pin capacitance, or more than twice the conversion, taking the average or the last few strokes data in order to increase the reliability of the data.

Note that usually before VDD is detected, do not switch the channel to 1/2VDD channel, as it has always been a DC current consumption, must be switched to another channel analog multiplexer, and it will be shut out of the resistor divider, which requires user attention.
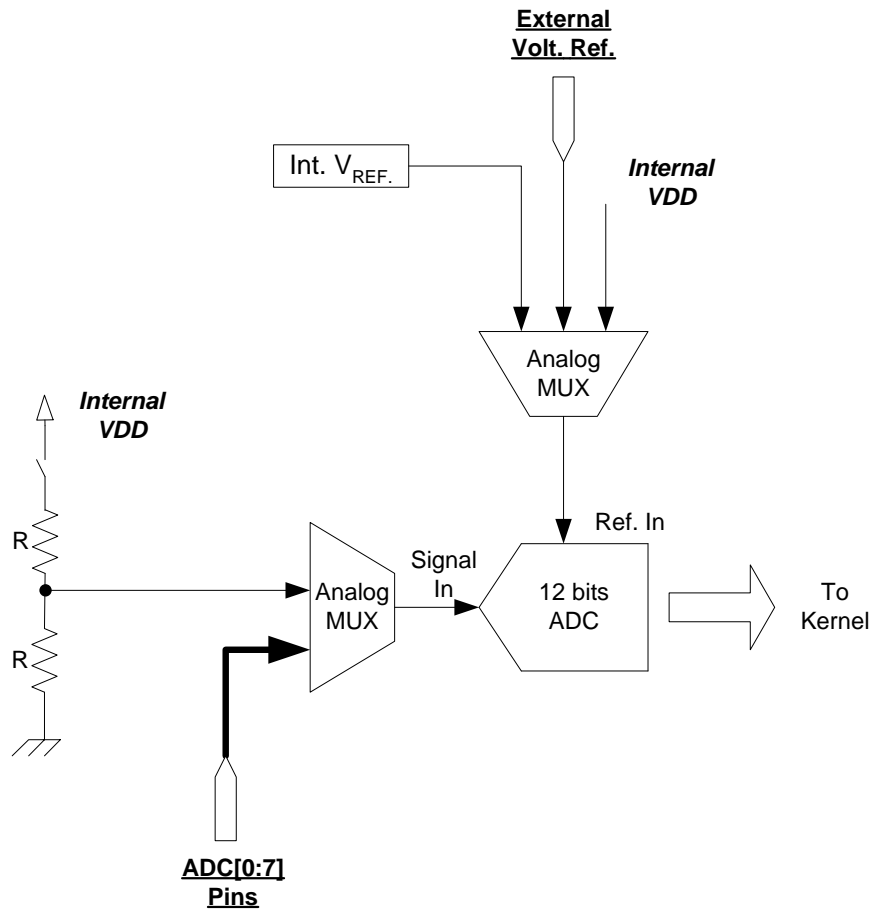
*Figure 6-14   ADC and VDD Detection Block Diagram*

## 6.8 Timer

There are three Timers in the EM88F752N. Timer 2 and Timer 3 are 8 bits up-counter. Timer 1 can be as one 8-bit up-counter or cascaded with Timer 2 as one 16-bit up-counter. If Timer 1 is used as 16-bit up-counter, the circuit resource of Timer 2 would be used. At this time, Timer 2 cannot be used.

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 0 | 0x24 | TC1CR1 | TC1S | TC1RC | TC1SS1 | TC1MOD | TC1FF | TC1OMS | TC1IS1 | TC1IS0 |
|        |         |        | R/W | R/W | R/W | R/W | R | R/W | R/W | R/W |
| Bank 0 | 0x25 | TC1CR2 | TC1M2 | TC1M1 | TC1M0 | TC1SS0 | TC1CK3 | TC1CK2 | TC1CK1 | TC1CK0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x26 | TC1DA | TC1DA7 | TC1DA6 | TC1DA5 | TC1DA4 | TC1DA3 | TC1DA2 | TC1DA1 | TC1DA0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x27 | TC1DB | TC1DB7 | TC1DB6 | TC1DB5 | TC1DB4 | TC1DB3 | TC1DB2 | TC1DB1 | TC1DB0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x28 | TC2CR1 | TC2S | TC2RC | TC2SS1 |  | TC2FF | TC2OMS | TC2IS1 | TC2IS0 |
|        |         |        | R/W | R/W | R/W |  | R | R/W | R/W | R/W |
| Bank 0 | 0x29 | TC2CR2 | TC2M2 | TC2M1 | TC2M0 | TC2SS0 | TC2CK3 | TC2CK2 | TC2CK1 | TC2CK0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3A | TC2DA | TC2DA7 | TC2DA6 | TC2DA5 | TC2DA4 | TC2DA3 | TC2DA2 | TC2DA1 | TC2DA0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3B | TC2DB | TC2DB7 | TC2DB6 | TC2DB5 | TC2DB4 | TC2DB3 | TC2DB2 | TC2DB1 | TC2DB0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3C | TC3CR1 | TC3S | TC3RC | TC3SS1 |  | TC3FF | TC3OMS | TC3IS1 | TC3IS0 |
|        |         |        | R/W | R/W | R/W |  | R | R/W | R/W | R/W |
| Bank 0 | 0x3D | TC3CR2 | TC3M2 | TC3M1 | TC3M0 | TC3SS0 | TC3CK3 | TC3CK2 | TC3CK1 | TC3CK0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3E | TC3DA | TC3DA7 | TC3DA6 | TC3DA5 | TC3DA4 | TC3DA3 | TC3DA2 | TC3DA1 | TC3DA0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x3F | TC3DB | TC3DB7 | TC3DB6 | TC3DB5 | TC3DB4 | TC3DB3 | TC3DB2 | TC3DB1 | TC3DB0 |
|        |         |        | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x15 | SFR2 |  |  |  |  |  | TC3DIF | TC2DIF | TC1DIF |
|        |         |      |  |  |  |  |  | F | F | F |
| Bank 0 | 0x1C | IMR2 |  |  |  |  |  | TC3DIE | TC2DIE | TC1DIE |
|        |         |      |  |  |  |  |  | R/W | R/W | R/W |

### 6.8.1 Timer/Counter Mode
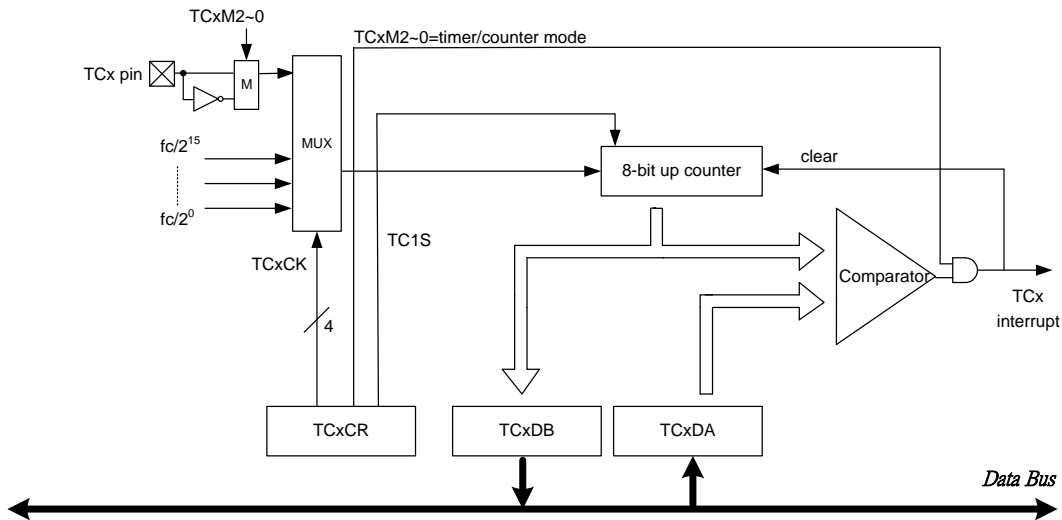


*Figure 6-15   Timer/Counter Mode*

In Timer/Counter mode, counting up is performed using internal clock or TCx pin. When the contents of up-counter are matched the TCxDA, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TCxDB by setting TCxRC to "1".
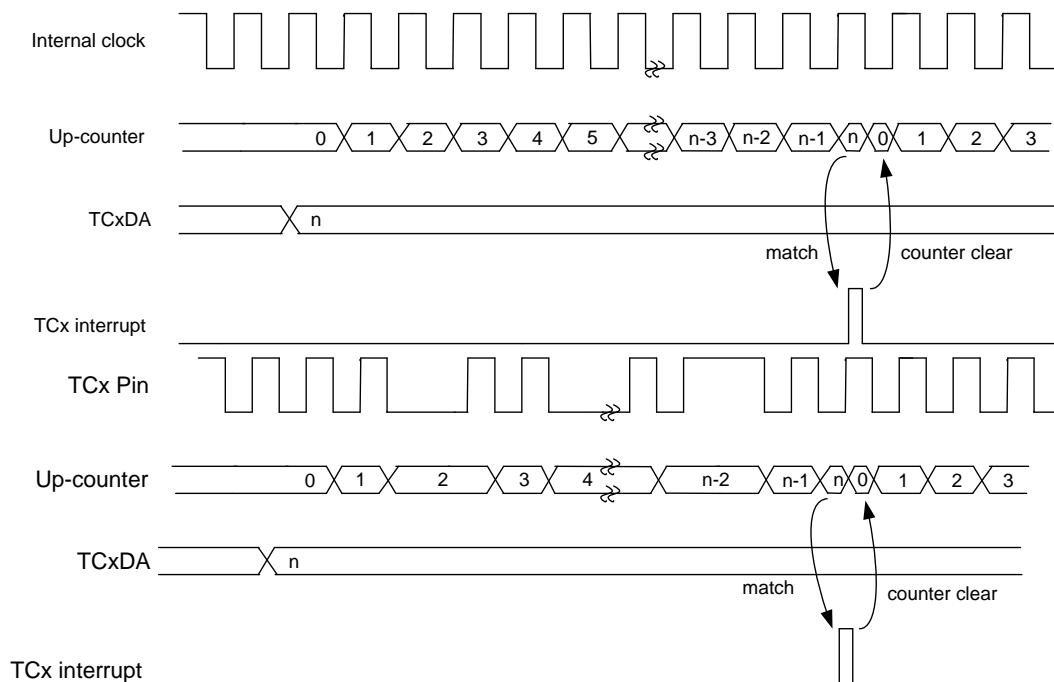


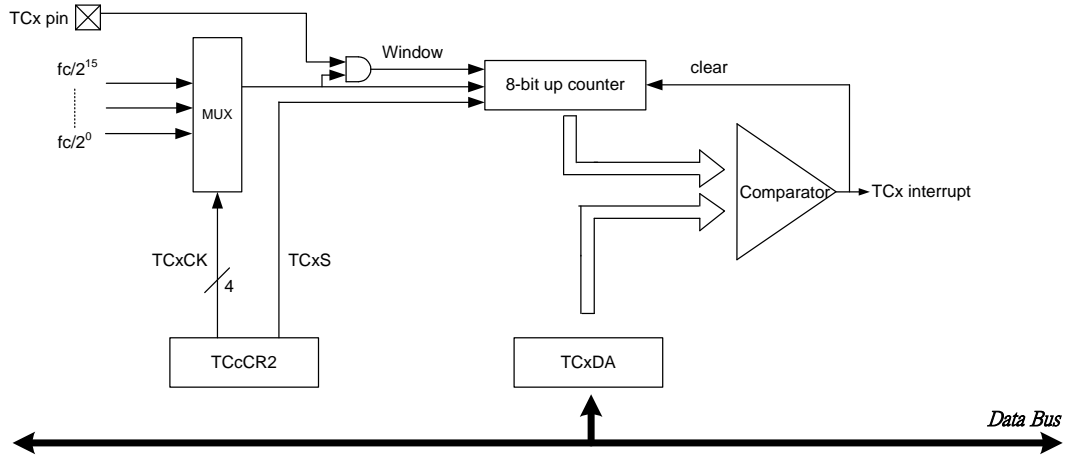*Figure 6-16   Timer/Counter Mode Waveform*

### 6.8.2 Window Mode



*Figure 6-17   Window Mode*

In Window mode, counting up is performed on rising edge of the pulse that is logical AND of an internal clock and the TCx pin (window pulse). When the contents of up-counter are matched the TCxDA, then interrupt is generated and counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.
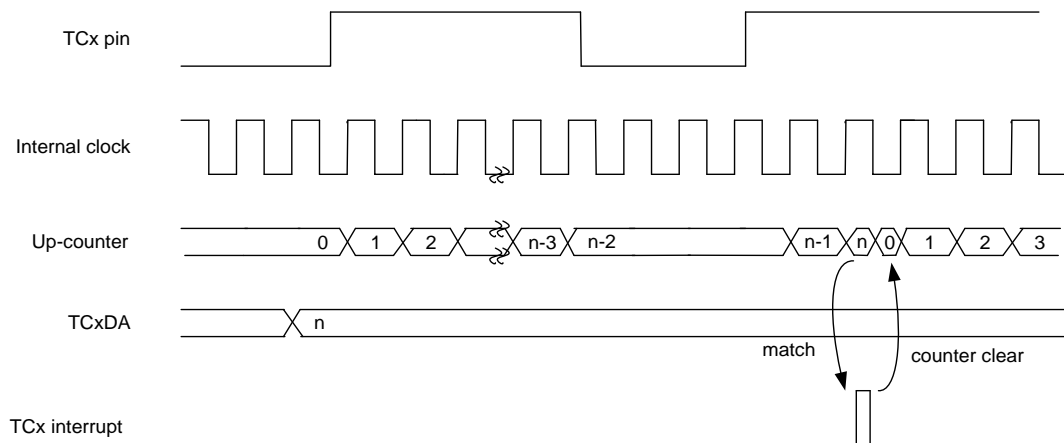


*Figure 6-18   Window Mode Waveform*

### 6.8.3 Capture Mode
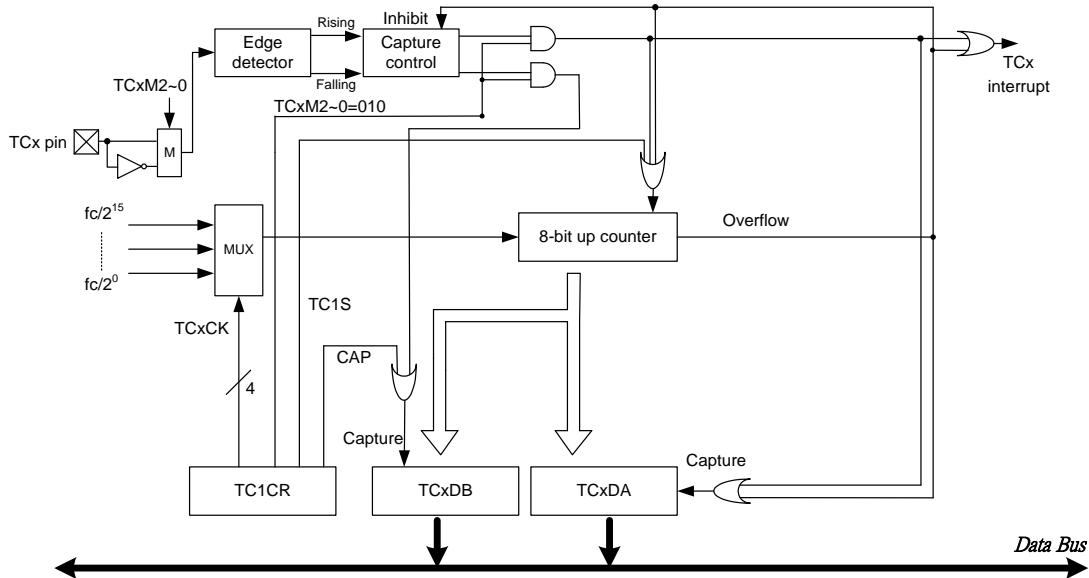


*Figure 6-19   Capture Mode*

In Capture mode, the pulse width, period and duty of the TCx input pin are measured in this mode, which can be used to decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TCx pin , the contents of counter is loaded into TCxDA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TCx pin, the contents of counter are loaded into TCxDB. At this time, the counter is still countering. Once the next rising edge of TCx pin triggers, the contents of counter are loaded into TCxDA, the counter is cleared and interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TCxDA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCxDA value is FFH. After an interrupt (capture to TCxDA or overflow detection) is generated, capture and overflow detection are halted until TCxDA is read out.
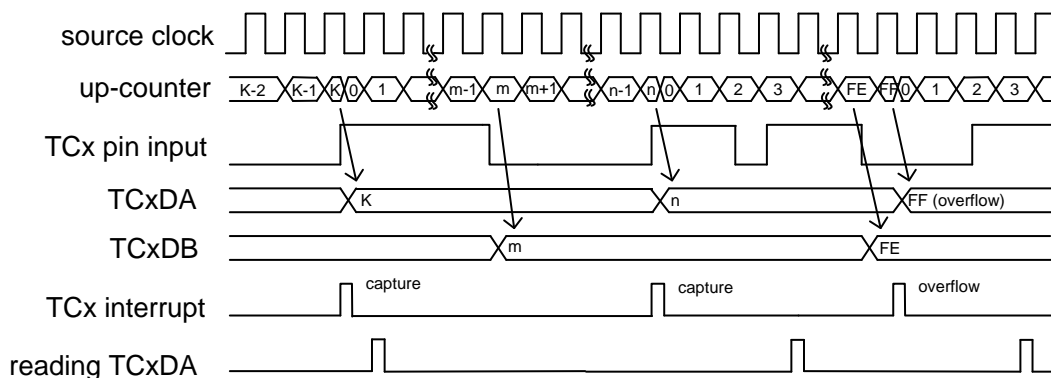


*Figure 6-20   Capture Mode Waveform*

### 6.8.4 Programmable Divider Output Mode and Pulse Width Modulation Mode
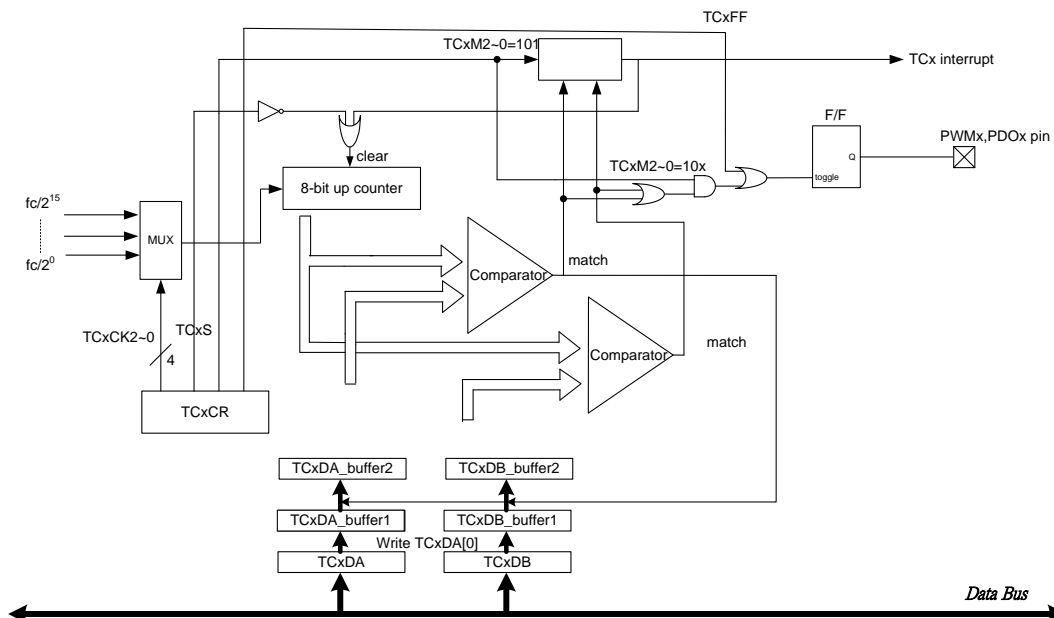


*Figure 6-21   PWM/PDO Mode*

### 6.8.5 PDO

In Programmable Divider Output (PDO) mode, counting up is performed using internal clock. The contents of TCxDA are compared with the contents of up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% duty pulse output. The PDO pin is initialized to "0" during reset. A TCx interrupt is generated each time the PDO output is toggled.
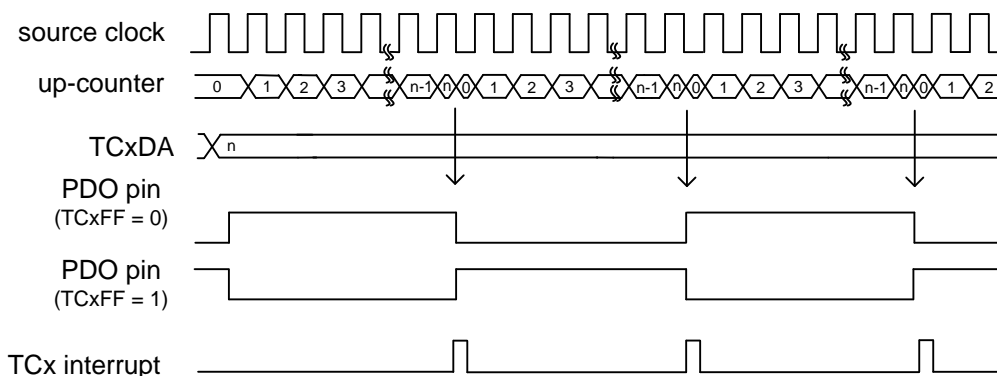


*Figure 6-22   PDO Mode Waveform*

### 6.8.6 PWM

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx control by TCxDB, and the period of PWMx control by TCxDA. The pulse at the PWMx pin is held to high level as long as TCxS=1 or Timerx matches TCxDA, while the pulse is held to low level as long as timer matches TCxDB. Once TCxFF is set to 1, the signal of PWMx is inverted. A TCx interrupt is generated and defined by TCxIS. On the other hand, the TCxDA and TCxDB can be written anytime, but the data of TCxDA and TCxDB are latched only at writing TCxDA[0]. Therefore, the new duty and new period of PWM appear at the PMW pin at the last period–match.
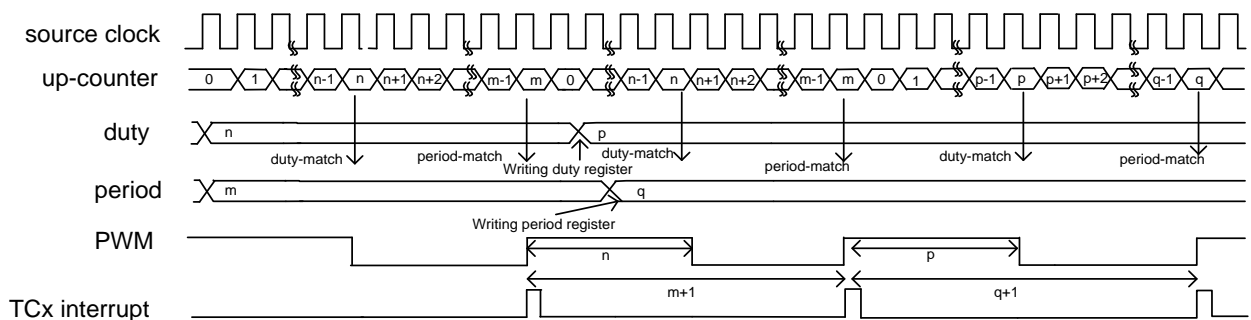


*Figure 6-23   PWM Mode Waveform*

### 6.8.7 Buzzer Mode

TCx pin output the clock after dividing frequency

## 6.9 PWM

| R_BAN | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bank 0 | 0x16 | SFR3 | | | | | PWMBPSF | PWMBDSF | PWMAPSF | PWMADSF |
| | | | | | | | F | F | F | F |
| Bank 0 | 0x1D | IMR3 | | | | | PWMBPIE | PWMBDIE | PWMAPIE | PWMADIE |
| | | | | | | | R/W | R/W | R/W | R/W |
| Bank 1 | 0x14 | DeadTCR | | | | | DEADTBE | DEADTAE | DEADTP1 | DEADTP0 |
| | | | | | | | R/W | R/W | R/W | R/W |
| Bank 1 | 0x15 | DeadTR | DEADTR[7:0] | | | | | | | |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x16 | PWMSCR | | | | DEADS | | | PWMBS | PWMAS |
| | | | | | | R/W | | | R/W | R/W |
| Bank 1 | 0x17 | PWMACR | PWMAE | IPWMAE | PWMAA | IPWMAA | TAEN | TAP2 | TAP1 | TAP0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x18 | PRDAL | PRDA[7:0] | | | | | | | |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x19 | PRDAH | | | | | | | PRDA[9:8] | |
| | | | | | | | | | R/W | R/W |
| Bank 1 | 0x1A | DTAL | DTA[7:0] | | | | | | | |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x1B | DTAH | | | | | | | DTA[9:8] | |
| | | | | | | | | | R/W | R/W |
| Bank 1 | 0x1C | TMRAL | TMRA[7:0] | | | | | | | |
| | | | R | R | R | R | R | R | R | R |
| Bank 1 | 0x1D | TMRAH | | | | | | | TMRA[9:8] | |
| | | | | | | | | | R | R |
| Bank 1 | 0x1E | PWMBCRR | PWMBE | IPWMBE | PWMBA | IPWMBA | TBEN | TBP2 | TBP1 | TBP0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x1F | PRDBL | PRDB[7:0] | | | | | | | |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x20 | PRDBH | | | | | | | PRDB[9:8] | |
| | | | | | | | | | R/W | R/W |
| Bank 1 | 0x21 | DTBL | DTB[7:0] | | | | | | | |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0x22 | DTBH | | | | | | | DTB[9:8] | |
| | | | | | | | | | R/W | R/W |
| Bank 1 | 0x23 | TMRBL | TMRB7 | | | | | | | |
| | | | R | R | R | R | R | R | R | R |
| Bank 1 | 0x24 | TMRBH | | | | | | | TMRB[9:8] | |
| | | | | | | | | | R | R |

### 6.9.1  Overview

In PWM mode, it produces up to 10-bit resolution PWM output (see. the functional block diagram). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period.  Figures 25~28 (*PWM Output Timing*) depict the relationships between a time period and a duty cycle.
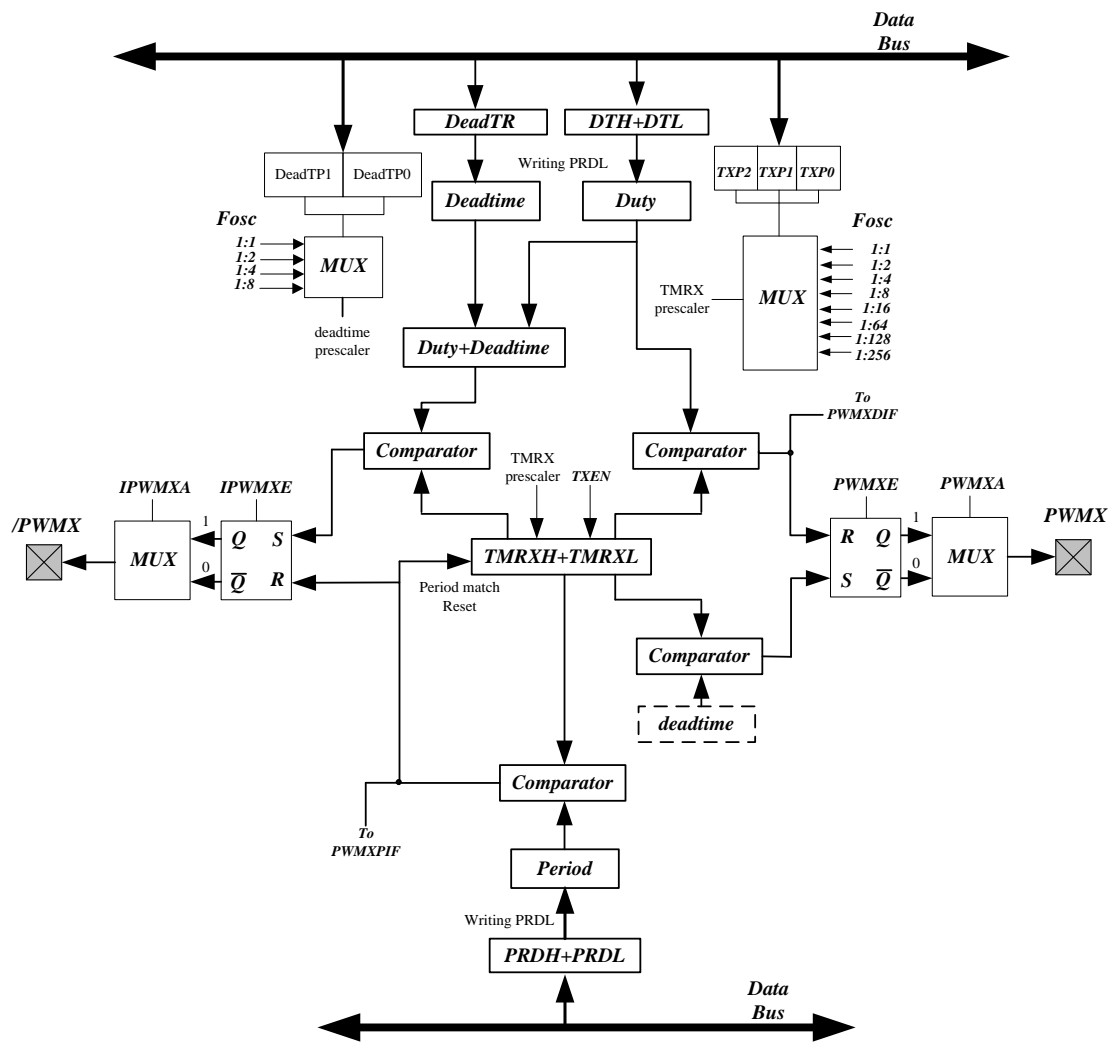


*Figure 6-24   PWM Functional Block Diagram*

PWM and /PWM (inverted PWM) can be used individually or used as dual PWM. When used individually, the definitions of active level between PWM and /PWM are somewhat different.

For example, set period and duty cycle (Period > Duty), PWMXE=1/0 and IPWMXE=0/1, PWMXA = 1/0, IPWMXA=1/0, and finally set TXEN = 1. The following figures show PWM output timing according to different PWMXA and IPWMXA settings.
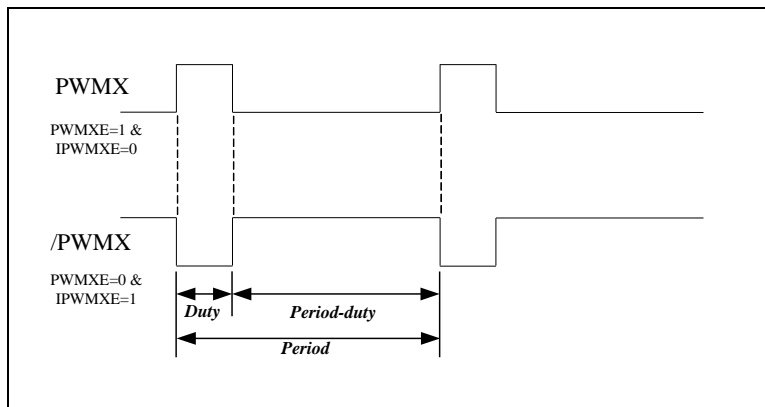


*Figure 6-25   PWM Output Timing (PWMXA=0 and IPWMXA=0)*
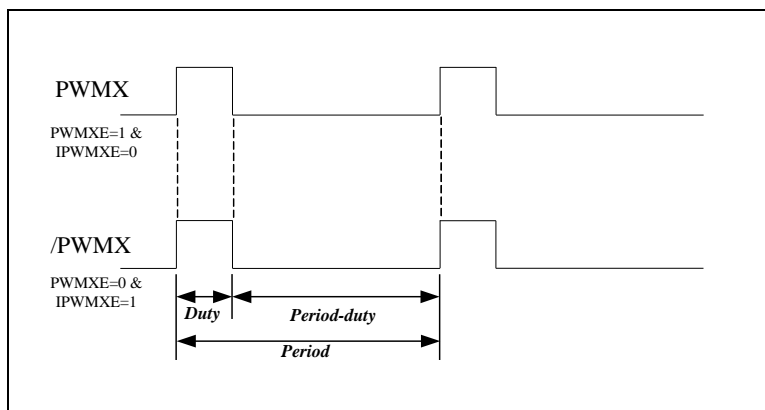


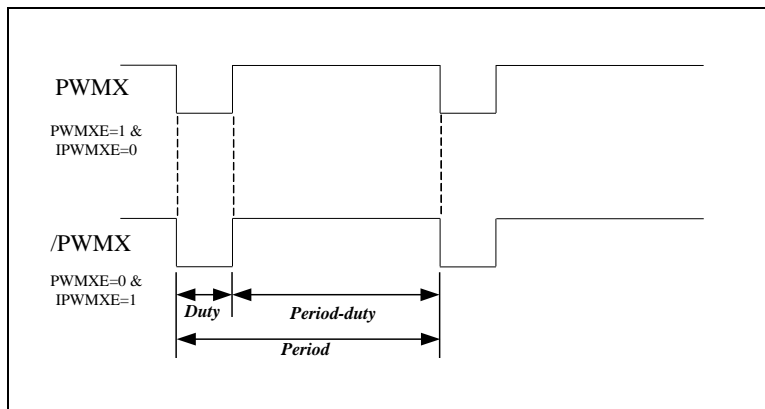*Figure 6-26   PWM Output Timing (PWMXA=0 and IPWMXA=1)*



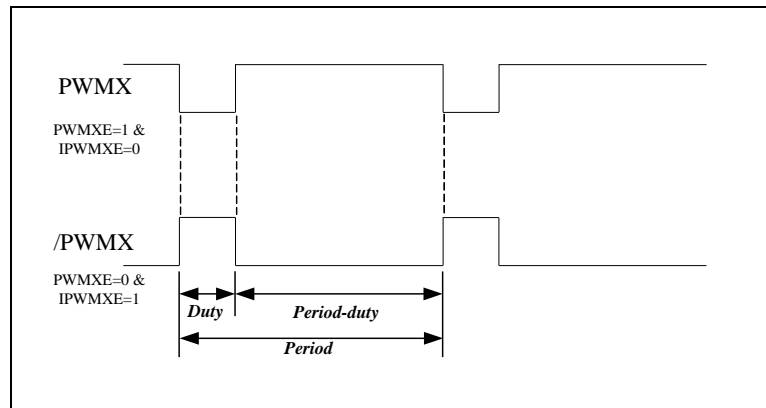*Figure 6-27   PWM Output Timing (PWMXA=1 and IPWMXA=0)*

*Figure 6-28   PWM Output Timing (PWMXA=1 and IPWMXA=1)*

### 6.9.2   Increment Timer Counter (TMRX: TMRAH/TMRAL, TMRBH/TMRBL)

TMRX are 10-bit clock counters with programmable prescaler. They are designed for the PWM module as baud rate clock generators. TMR can be read only. If employed, they can be turned off for power saving by setting the PWMACR [TAEN], or PWMBCR [TBEN] to 0.

TMRA, TMRB, and are internally designed and cannot be set.

### 6.9.3   PWM Time Period (PRDX: PRDAL/H, PRDBL/H)

The PWM period is 10-bit resolution. The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

■   TMRX is cleared

■   The PWMX pin is set to 1

---

**NOTE**

*The PWM output will not be set, if the duty cycle is 0*

---

■   The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period:

$$Period = (PRDX + 1) \times \left( \frac{1}{F_{osc}} \right) \times (TMRX\ prescale\ value)$$

**Example:**

    **PRDX = 49;**        **Fosc = 4 MHz;**        **TMRX (0, 0, 0) = 1 : 1,**

    **Then**

$$Period \ = \ \left(49+1\right) \ \times \ \left(\frac{1}{4M}\right) \ \times \ 1 \ = \ 12.5\mu s$$

### 6.9.4  PWM Duty Cycle (DTX: DTAH/DTAL or DTBH/DTBL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime.  However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty \ cycle \ = \ \left(DTX\right) \ \times \ \left(\frac{1}{F_{osc}}\right) \ \times \ \left(TMRX \ prescale \ value\right)$$

**Example:**

    **DTX = 10;**        **Fosc = 4 MHz;**        **TMRX (0, 0, 0) = 1 : 1,**

    **Then**

$$Duty \ cycle \ = \ \left(10\right) \ \times \ \left(\frac{1}{4M}\right) \ \times \ 1 \ = \ 2.5\mu s$$

### 6.9.5  Dual PWM function

It is consists of a complementary PWM (i.e. PWMX and /PWMX), one outputs PWM signal and the other outputs inverted PWM signal, It can output any pulse width signal you want by programming relative control registers.

The dead time mode is supported. It means that the complementary PWM signals can be controlled to get a time interval that the complementary PWM signals won't be intersected.

The following Figures 6-29 ~ 30 show the dual PWM output waveform.

Disable dead time control (DEADTXE = 0). Set period and duty cycle (period > duty). Set PWMXE and IPWMXE =1, PWMXA = 0/1, IPWMXA = 0/1, and finally set TXEN = 1.
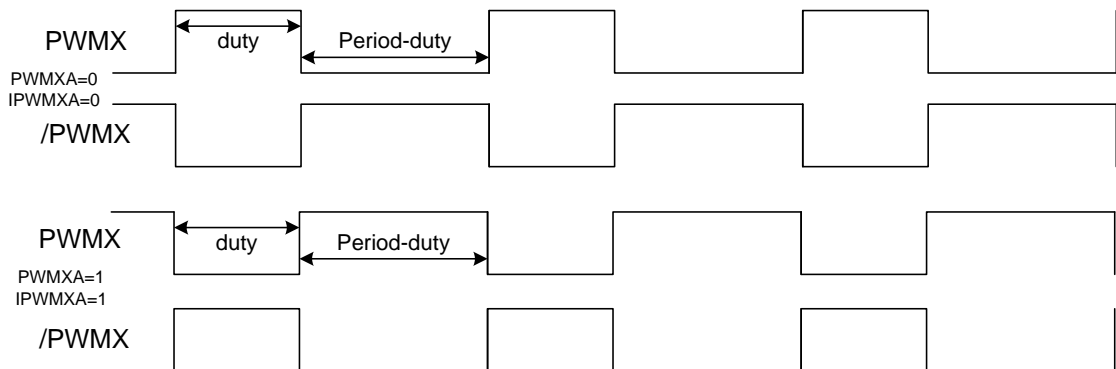


*Figure 6-29   Dual PWMX Output Waveform (DEADTXE = 0)*

Set dead time > 0 (set dead time prescaler if required). Enable dead time control (DEADTXE = 1). Set period and duty cycle (period > duty). Set PWMXE and IPWMXE =1, PWMXA = 0, IPWMXA = 0, and finally set TXEN = 1. For the loading new duty, period, and dead time value at run time, following subchapter "PWM Programming Process/Steps" makes such descriptions.
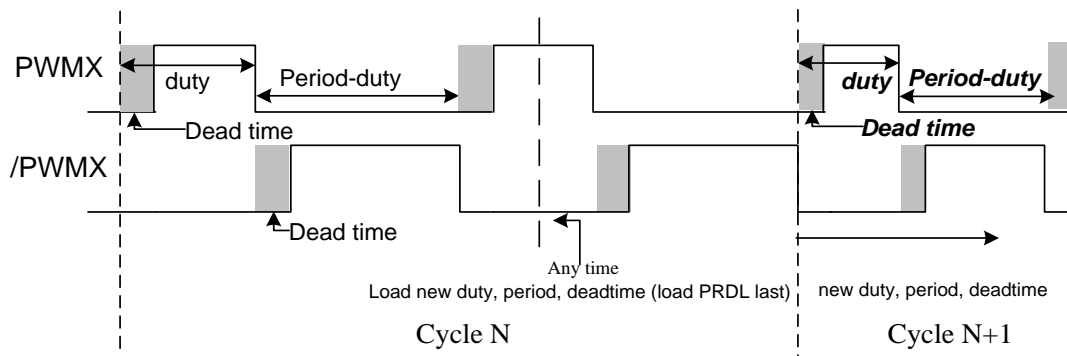


*Figure 6-30   Dual PWMX Output Waveform (DEADTXE = 1, Dead Time > 0)*

## 6.10 I2C Function

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bank 0 | 0x30 | I2CCR1 | Strobe/Pend | IMS | ISS | STOP | SAR_EMPTY | ACK | FULL | EMPTY |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x31 | I2CCR2 | I2CBF | GCEN | | BBF | I2CTS1 | I2CTS0 | | I2CEN |
| | | | R | R/W | | R | R/W | R/W | | R/W |
| Bank 0 | 0x32 | I2CSA | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | IRW |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x33 | I2CDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x34 | I2CDAL | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x35 | I2CDAH | | | | | | | DA9 | DA8 |
| | | | | | | | | | R/W | R/W |
| Bank 0 | 0x17 | SFR4 | | | | | | I2CSTPIF | I2CRSF | I2CTSF |
| | | | | | | | | R/W | R/W | R/W |
| Bank 0 | 0x1E | IMR4 | | | | | | I2CSTPIE | I2CRIE | I2CTIE |
| | | | | | | | | R/W | R/W | R/W |
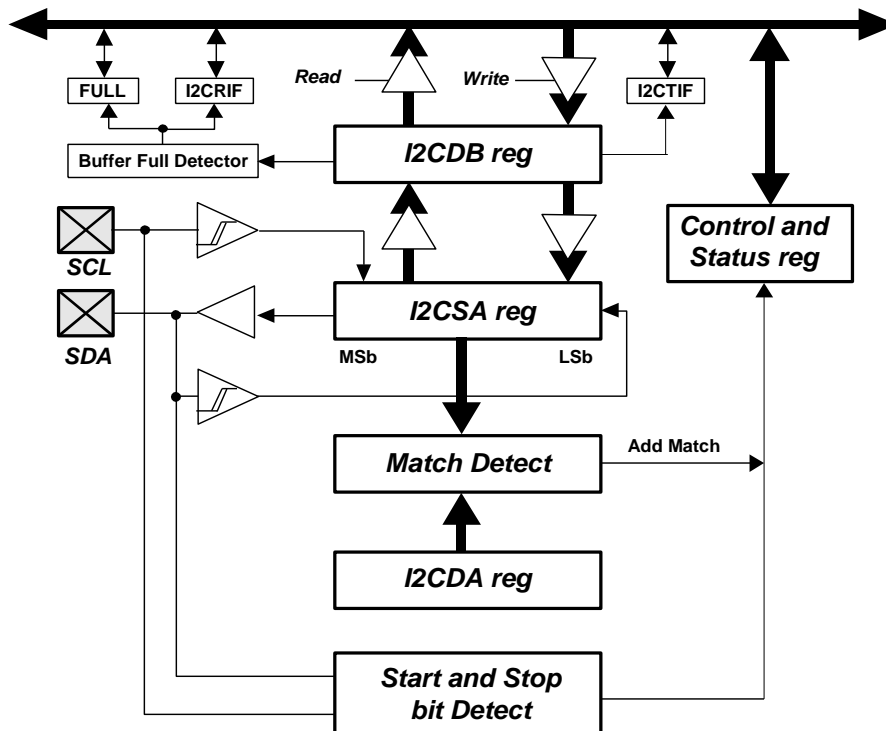


*Figure 6-31   I2C Block Diagram*

The EM88F752N supports a bidirectional, 2-wire bus, 7/10-bit addressing and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at rates of up to 100 kbps in the Standard-mode or up to 400 kbps in the Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

I2C interrupt occurs as shown below:

| Condition | Master/Slave | Transmit Address | Transmit Data | Stop |
|---|---|---|---|---|
| Master-transmitter transmits to slave-receiver | Master | Transmit interrupt | Transmit interrupt | Stop interrupt |
| | Slave | Receive interrupt | Receive interrupt | Stop interrupt |
| Master receiver read slave-transmitter | Master | Transmit interrupt | Receive interrupt | Stop interrupt |
| | Slave | Transmit interrupt | Transmit interrupt | Stop interrupt |

Within the procedure of the I2C bus, unique situations arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

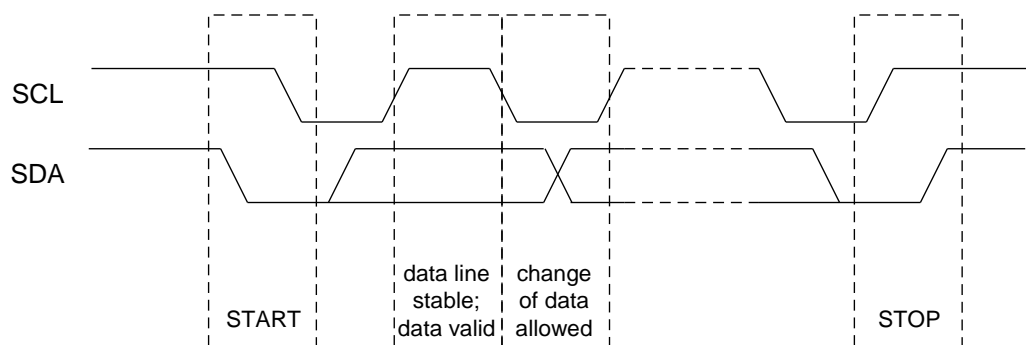A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.



*Figure 6-32   I2C Transfer Condition*

### 6.10.1  7-Bit Slave Address

Master-transmitter transmits to slave-receiver. The transfer direction is not changed.

Master reads slave immediately after first byte. At the moment of the first acknowledge, the master- transmitter becomes a master- receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The STOP condition is generated by the master, which has previously sent a not-acknowledge (A).

Master reads slave immediately after first byte. At the moment of the first acknowledge, the master- transmitter becomes a master- receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The STOP condition is generated by the master, which has previously sent a not-acknowledge (A). The difference between master transmitter with master receiver is only in R//W bit, if the R//W bit were "0", the master device would be transmitter; the other way, the master device would be receiver. The master transmitter is described by the figure 6-33" 7-Bit slave address in Master-transmitter transmits to slave -receiver", and the master receiver is described by figure 6-34" 7-Bit slave address in Master-receiver read slave -transmitter"
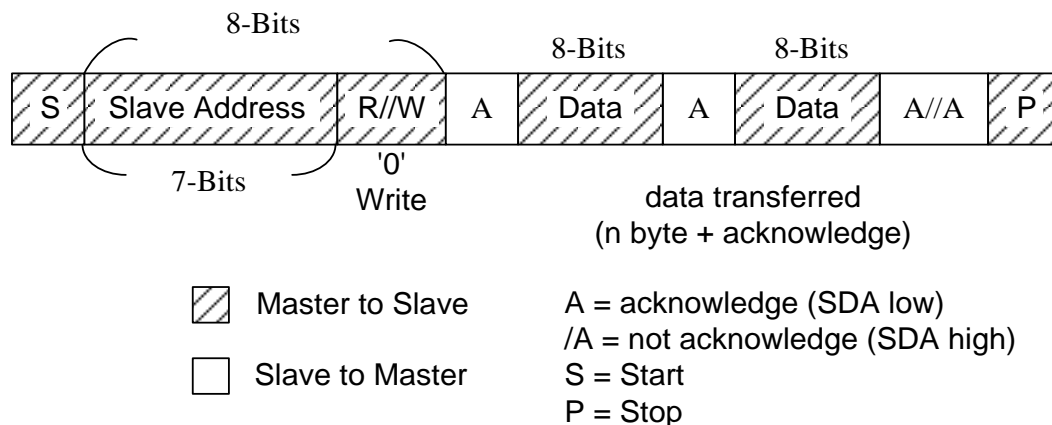


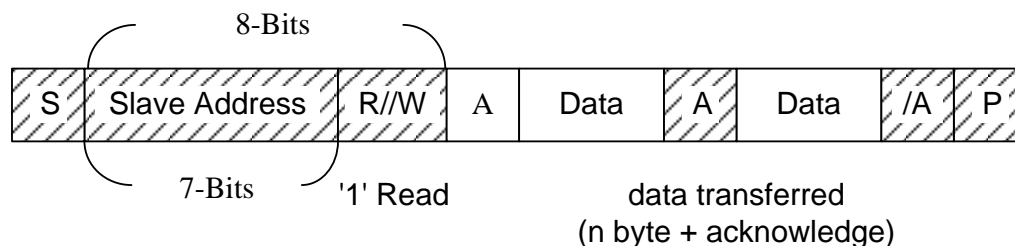*Figure 6-33   7-Bit Slave Address in Master-transmitter transmits to slave-receiver*



*Figure 6-34   7-Bit Slave Address in Master receiver read slave-transmitter*

### *6.10.2   10-Bit Slave Address*

In 10-bit slave address mode, using 10 bits for addressing exploits the reserved combination 11110XX for the first seven bits of the first byte following a START(S) or repeated START (Sr) condition. The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bits address. If the R//W bit were "0", the second byte after acknowledge would be the eight address bits of 10-bits slave address; in the other way, the second byte would just only be the next transmitted data from a slave to master device. The first bytes 11110XX be transmitted by using the slave address register (I2CSA), and the second bytes XXXXXXXX would be transmitted by using the data buffer (I2CDB).

There are few kinds of different formats that would be explained in Figure 6-35 ~ Figure 6-39 in the 10-bit slave address mode. The possible data transfer formats are:

● **Master-transmitter transmits to slave-receiver with a 10-bit slave address**

When the slave have received the first byte after START bit from master, each slave devices will compare the seven bits of the first byte (11110XX) with their own address and the eighth bit, R//W, if the R//W bit were "0", the slave would return the acknowledge (A1) and that would be possible more than one slave device return it. Then all slave device will continue to compare the second address (XXXXXXXX), if the slave device have matched, that would be only one slave device return acknowledge. The matching slave device will remain addressed by the master until it receives the STOP condition or a repeated START condition followed by the different slave address.
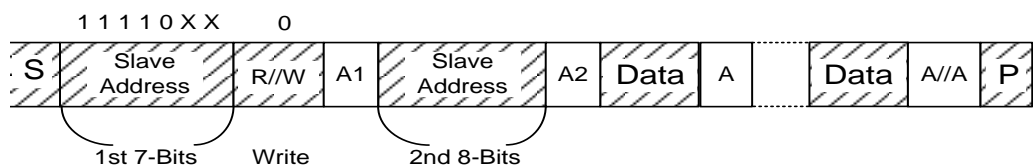


*Figure 6-35   Master-transmitter transmits to slave-receiver with a 10-bit slave address*

● **Master-receiver read slave-transmitter with a 10-bit slave address**

Up to and including acknowledge Bit A2, the procedure is the same as that described for master-transmitter addressing a slave receiver. After the acknowledge A2, a repeated START condition (Sr) followed by seven bits slave address (11110XX) but the eighth bit R//W is "1", the addressed slave device will return the acknowledge A3. If the repeated START(Sr) condition and the seven bits of first byte (11110XX) received by slave device, all the slave device would compare with their own address and test the eighth R//W, but none of all slave device return the acknowledge because R//W=1.

1 1 1 1 0 X X     0                             1 1 1 1 0 X X     1

| S | Slave Address | R//W | A1 | Slave Address | A2 | Sr | Slave Address | R//W | A3 | DATA | A | ... | DATA | /A | P |

1st 7-Bits    Write        2nd 8-Bits         1st 7-Bits    read

*Figure 6-36   Master-receiver read slave-transmitter with a 10-bit slave address*

● Master addresses a slave with 10-Bit addresses transmits and receives data in the same slave device.

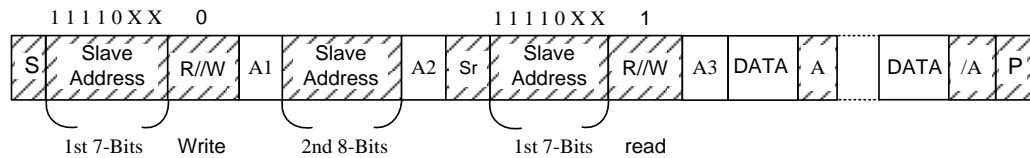At first, the transmitter procedure is the same as the section of the "Master-transmitter transmits to slave-receiver with a 10-bit slave address", then the master device can start to transmit the data to slave device. If the slave device has received an acknowledge or none acknowledge which were followed by repeat START (Sr) and repeat the procedure of the section of "Master-receiver read slave-transmitter with a 10-bit slave address".

1 1 1 1 0 X X     0

| S | Slave Address | R//W | A | Slave Address | A | Data | A | ... | Data | A//A |

1st 7-Bits    Write        2nd 8-Bits

1 1 1 1 0 X X     1

| Sr | Slave Address | R//W | A | Data | A | ... | Data | /A | P |

1st 7-Bits    Read
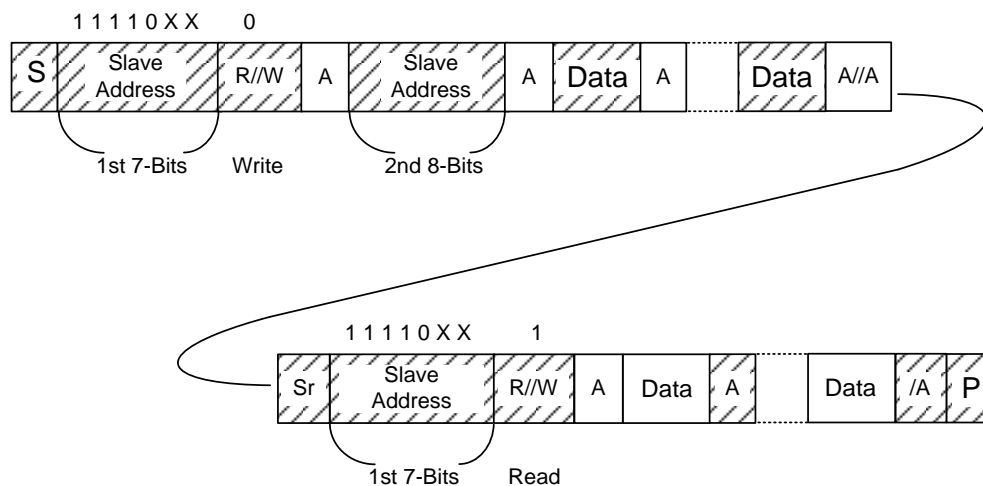
*Figure 6-37   Master addresses a slave with 10-bit addresses transmits and receives data in the same slave device*

● Master device transmit data to two or more than two slave device

The section of "Master-transmitter transmits to slave-receiver with a 10-bit slave address" describe the procedure how to transmit the data to slave device, if the master device have finished the transmittal, and want to transmit the data to another device, the master would need to address the new slave device, the address procedure is described by the section of the "Master-transmitter transmits to slave-receiver with a 10-bit slave address". If the master device wants to transmit the data in 7-bit slave address mode and transmit the data in 10-bit slave address mode in the serial transfer, after the START or repeat START conditions, a 7-bit and 10-bit address could be transmitted. Figure 6-37~6-38 shows how to transmit the data in 7-bit and 10-bit address mode in serial transfer.
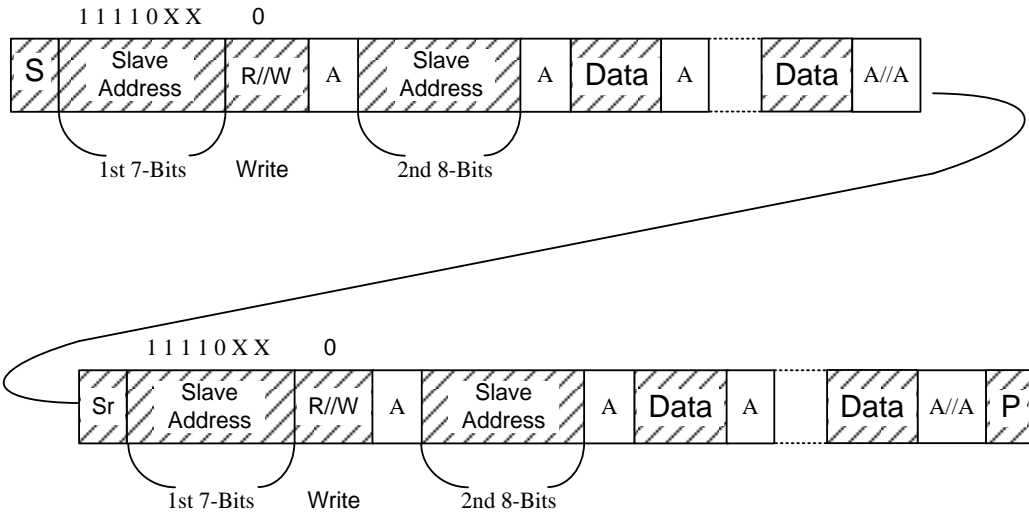
*Figure 6-38  Transmit one more device with a 10-bit Slave Address*
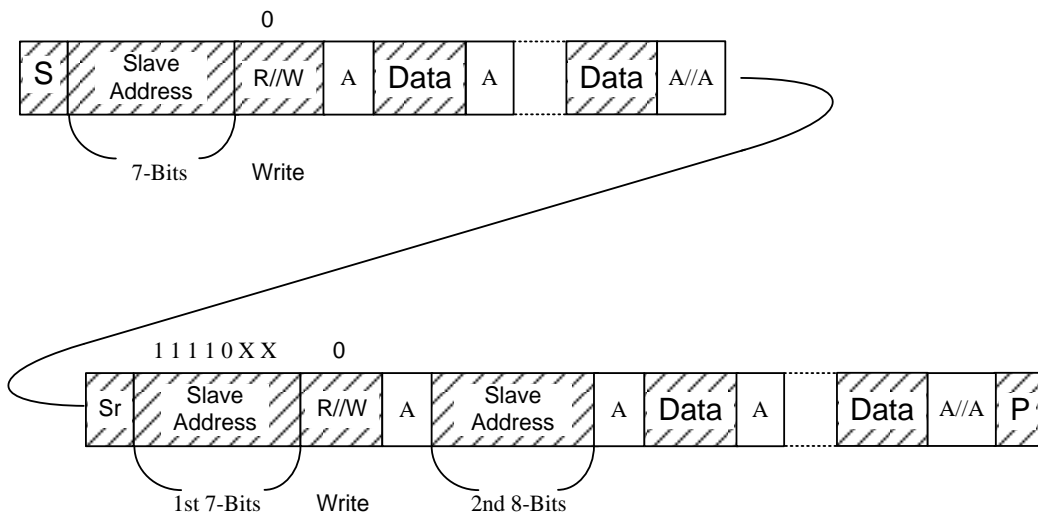


*Figure 6-39   7-bit and 10-bit Slave Address Mode*

### *6.10.3   Master Mode*

In transmitting (receiving) serial data, the I2C operates as follows:

1.   Set I2CTS1~0, and ISS bits to select I2C transmit clock source.

2.   Set I2CEN and IMS bits to enable I2C master function.

3.   Write slave address into the I2CSA register and IRW bit to select read or write.

4.   Set strobe bit will start transmit and then Check I2CTSF (I2CTSF) bit.

5.   Write 1st data into the I2CDB register, set strobe bit and Check I2CTSF (I2CRSF) bit.

6.   Write 2nd data into the I2CDB register, set strobe bit, STOP bit and Check I2CTSF (I2CRSF) bit.

### *6.10.4   Slave Mode*

In receiving (transmitting) serial data, the I2C operates as follows:

1.   Set I2CTS1~ 0 and ISS bits to select I2C transmit clock source.

2.   Set I2CEN and IMS bits to enable I2C slave function.

3.   Write device address into the I2CDA register.

4.   Check I2CRSF (I2CTSF) bit, read I2CDB register (address) and then clear Pend bit.

5.   Check I2CRSF (I2CTSF) bit, read I2CDB register (1st data) and then clear Pend bit.

6.   Check I2CRSF (I2CTSF) bit, read I2CDB register (2st data) and then clear Pend bit.

7.   Check I2CSTPSF bit, end transmission.

## 6.11  Enhance Protect

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bank 2 | 0x47 | LOCKPR | LOCKPR7 | LOCKPR6 | LOCKPR5 | LOCKPR4 | LOCKPR3 | LOCKPR2 | LOCKPR1 | LOCKPR0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0x48 | LOCKCR | LOCKEN | | | | | | | |
| | | | R/W | | | | | | | |

The EM88F752N supports a protect function to prevent the source code from overwriting or reading. When the instruction TBRDA/TBRD/TBWR be execute at protect area, it can write or read all flash ROM. When the instruction TBRDA/TBRD/TBWR be execute at normal area, it can write or read the ROM at normal area only.

### *6.11.1  Enhance Protect Programming*

The Enhance Protect operates as follows:

1.  Set LOCKEN.

2.  Write 0xC5 into FLKR.

3.  Write LOCKPR to set lock range.

    *Instruction "TBRDA/TBRD/TBWR" cannot be writing at the end of lock area

    *The base unit of LOCKPR is 128 words.

    *When use the TBWR instruction, the code option "TBWEN" must be enabled.

**EX:**
**LOCKPR=0x08**
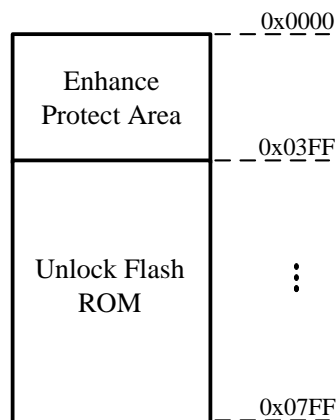


*Figure 6-40   Example of Enhance Protect Function (LOCKPR=0x08)*

## 6.12 Oscillator

### 6.12.1 Oscillator Modes

The EM88F752N can be operated in the five different oscillator modes, such as Internal RC oscillator mode (IRC) and XTAL oscillator mode (XT). User needs to set main-oscillator modes by selecting the OSC2~OSC0, and set sub-oscillator modes by selecting the FSS1~FSS0 in the CODE Option register to complete the overall oscillator mode setting. Tables 7, 8, and 9 depict how these four modes are defined.

The up-limited operation frequency of crystal/resonator on the different VDD is listed in Table 10.

**Table 7    Main-oscillator modes defined by OSC[2:0]**

| Main-oscillator mode | OSC2 | OSC1 | OSC0 |
|---|---|---|---|
| IRC (Internal RC oscillator mode) (default)<br>RCOUT (P80) acts as I/O pin | 0 | 0 | 0 |
| IRC (Internal RC oscillator mode)<br>RCOUT (P80) acts as clock output pin | 0 | 0 | 1 |
| HXT1 (High XTAL1 oscillator mode)<br>Frequency range: 12~20 MHz | 0 | 1 | 0 |
| HXT2(High XTAL2 oscillator mode)<br>Frequency range: 6~12 MHz | 0 | 1 | 1 |
| XT (XTAL oscillator mode)<br>Frequency range: 1~6 MHz | 1 | 0 | 0 |
| LXT1 (Low XTAL1 oscillator mode)<br>Frequency range: 100K~1 MHz | 1 | 0 | 1 |
| LXT2 (Low XTAL2 oscillator mode)<br>Frequency range: 32.768kHz | 1 | 1 | 0 |
| Reserve | 1 | 1 | 1 |

**Table 8    Sub-oscillator modes defined by FSS1 ~ FSS0**

| Sub-oscillator Mode | FSS1 | FSS0 |
|---|---|---|
| LXT3 (Low XTAL3) oscillator mode<br>Frequency range: 32.768kHz | 1 | x |
| Fs is 16kHz, Xin (P83) / Xout (P84) pin act as I/O (default) | 0 | 0 |
| Fs is 128kHz, Xin (P83) / Xout (P84) pin act as I/O | 0 | 1 |

*Note: WDT frequency is always 16kHz whenever the FSS[1:0] bits are set.*

**Table 9    Combination of main-oscillator and sub-oscillator modes**

| Combination | Main Clock | Sub-clock |
|:---:|:---:|:---:|
| 1 | Crystal | Crystal |
| 2 | Crystal | IRC |
| 3 | IRC | Crystal |
| 4 | IRC | IRC |

**Table 10   Summary of Maximum Operating Speeds**

| Conditions | VDD | $F_{XT}$ max. (MHz) |
|:---:|:---:|:---:|
| Two cycles with two clocks | 2.1 | 8.0 |
| | 3.5 | 16.0 |
| | 5.0 | 20.0 |

## 6.12.2   Internal RC Oscillator Mode

EM88F752N offer a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (20 MHz, 16 MHz, 12 MHz , 8 MHz, 6 MHz, 1 MHz ) that can be set by Code Option Bits RCM2 ~ RCM0.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

| Internal RC Frequency | Drift Rate | | | |
|:---:|:---:|:---:|:---:|:---:|
| | Temperature (-40°C~+85°C) | Voltage (2.1V~5.5V) | Process | Total |
| 1 MHz | ±2% | ±1% | ±1% | ±4% |
| 4 MHz | ±2% | ±1% | ±1% | ±4% |
| 6 MHz | ±2% | ±1% | ±1% | ±4% |
| 8 MHz | ±2% | ±1% | ±1% | ±4% |
| 12 MHz | ±2% | ±1% | ±1% | ±4% |
| 16 MHz | ±2% | ±1% | ±1% | ±4% |
| 20 MHz | ±2% | ±1% | ±1% | ±4% |

*Note: Theoretical values are for reference only.  Actual values may vary depending on actual process.*

## 6.13  Power−on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply has remained stabilized. The EM88F752N has an on-chip Power−on Voltage Detector (POVD) with a detecting level of 1.9V. It will work well if VDD is rising quick enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

## 6.14  External Power−on Reset Circuit

The circuit as shown in Figure 6-41 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ± 5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.
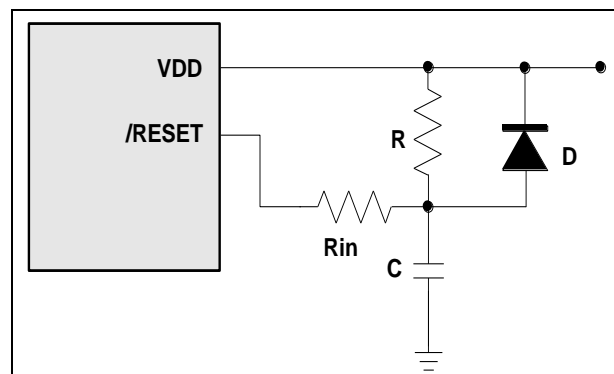


*Figure 6-41   External Power-Up Reset Circuit*

## 6.15  Residue-Voltage Protection

When battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trips below VDD minimum, but not to zero. This condition may cause a poor power on reset. Figure 6-42 and Figure 6-43 show how to build a residue-voltage protection circuit.
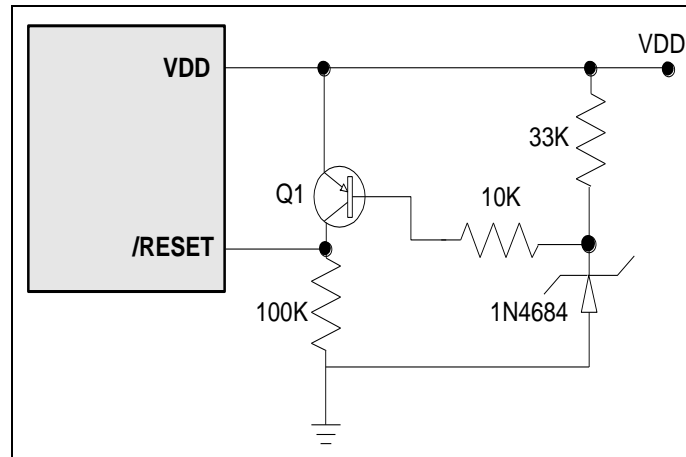
*Figure 6-42   Circuit 1 for the Residue Voltage Protection*
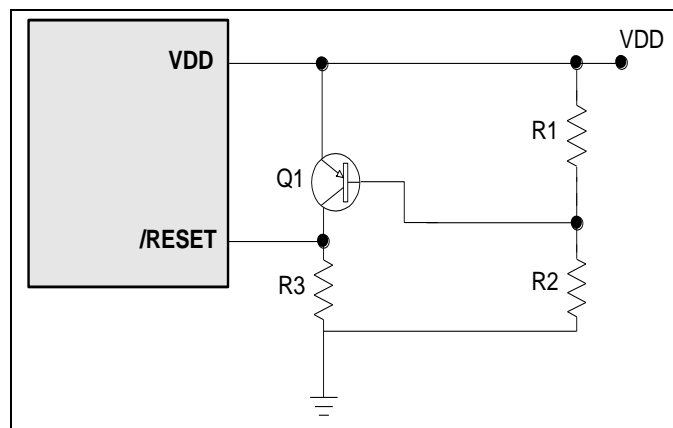


*Figure 6-43  Circuit 2 for the Residue Voltage Protection*

## 6.16 Code Option

### 6.16.1 Code Option Register (Word 0)

| Word 0 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Mnemonic** | **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit11** | **Bit10** | **Bit9** | **Bit8** |
| | - | - | IRCWUT | IODG1 | IODG0 | HLFS | HLP | LVR1 |
| 1 | High | High | 32 clks | High | High | Green | Low PWR | High |
| 0 | Low | Low | 8 clks | Low | Low | Normal | High PWR | Low |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Mnemonic** | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| | LVR0 | RESETEN | ENWDT | NRHL | NRE | - | - | - |
| 1 | High | /RST | Enable | 8/fc | Disable | High | | |
| 0 | Low | P82 | Disable | 32/fc | Enable | Low | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | | |

**Bits 15~14:** Not used, set to "0" all the time.

**Bit 13 (IRCWUT):** IRC Warm-up Time (IRC Frequency Range 1 MHz ~8 MHz)

0: 8 clocks (default)

1: 32 clocks

| CPU mode switch | IRC Frequency | Waiting Time before CPU Starts to Work |
|---|---|---|
| **Sleep → Normal** **Idle → Normal** | **12M, 16M, 20M** | **WSTO + 32 clocks (main frequency)** |
| **Green → Normal** | **1M, 4M, 6M, 8M** | **WSTO + 8/32 clocks (main frequency)** |
| **Sleep → Green** **Idle → Green** | **128kHz** | **WSTO + 8 clocks (sub frequency)** |

**Bits 12~11 (IODG1~IODG0):** I2C pin deglitch time select bits.

| IODG1~0 | SPI Pin Deglitch Time | I2C Pin Deglitch Time | OCDS Pin Deglitch Time |
|---|---|---|---|
| 00 | Typical delay = 8ns | 50ns@5V,Typical (default) | 20ns@5V,Typical (default) |
| 01 | Typical delay = 15ns | 100ns@5V,Typical | |
| 10 | Typical delay = 25ns | 150ns@5V,Typical | |
| 11 | No deglitch | No deglitch | No deglitch |

**Bit 10 (HLFS):** Reset to Normal or Green Mode Select Bit

0: CPU is selected as Normal mode when a reset occurs (default)

1: CPU is selected as Green mode when a reset occurs.

**Bit 9 (HLP):** Power Consumption Selection

0: High power consumption, apply to working frequency above 4 MHz

1: Low power consumption, apply to working frequency at 4 MHz or below 4 MHz

**Bits 8~7 (LVR1~LVR0):** Low Voltage Reset enable bit.

| LVR1, LVR0 | VDD Reset Level | VDD Release Level |
|:---:|:---:|:---:|
| 00 | NA (Power on reset) (default) | |
| 01 | 2.7V | 2.9V |
| 10 | 3.5V | 3.7V |
| 11 | 4.0V | 4.2V |

> *Note:* If VDD < 2.7V and keep about 5 μs, IC will be reset.
> If VDD < 3.5V and keep about 5 μs, IC will be reset.
> If VDD < 4.0V and keep about 5 μs, IC will be reset.

**Bit 6 (RESETEN):** P82/RESET pin selection bit

       0: Disable, P82 as I/O pin (default)

       1: Enable, P82 as RESET pin.

**Bit 5 (ENWDT):** WDT enable bit

       0: Disable (default)

       1: Enable

**Bit 4 (NRHL):** Noise rejection high/low pulse define bit (For the INT Pin)

       0: pulses equal to 32/Fc [s] is regarded as signal (default)

       1: pulses equal to 8/Fc [s] is regarded as signal

**<Note>** In Low XTAL oscillator (LXT) mode the noise rejection high/low pulses always 8/Fm.

**Bit 3 (NRE):** Noise Rejection Enable bit

       0: Enable (default) .**But in Green, Idle, and Sleep modes, the noise rejection circuit is always disabled.**

       1: Disable

**Bits 2~0:** Not used, set to "0" all the time.

### *6.16.2 Code Option Register (Word 1)*

| Word 1 | | | | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| **Mnemonic** | **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit11** | **Bit10** | **Bit9** | **Bit8** |
| | - | FSS1 | FSS0 | - | - | - | - | - |
| 1 | High | High | High | High | High | High | High | High |
| 0 | Low | Low | Low | Low | Low | Low | Low | Low |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Mnemonic** | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| | - | RCM2 | RCM1 | RCM0 | OSC2 | OSC1 | OSC0 | RCOUT |
| 1 | High | High | High | High | High | High | High | High |
| 0 | Low | Low | Low | Low | Low | Low | Low | Low |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 15:** Not used, set to "0" all the time.

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    **● 135**
*(This specification is subject to change without prior notice)*

**Bits 14~13 (FSS1~FSS0):** Sub-oscillator mode selection bits

| Sub-oscillator mode | FSS1 | FSS0 |
|---|---|---|
| LXT3 (Low XTAL3) oscillator mode<br>Frequency range: 32.768kHz | 1 | x |
| Fs is 16kHz, Xin (P83) / Xout (P84) pin act as I/O (default) | 0 | 0 |
| Fs is 128kHz, Xin (P83) / Xout (P84) pin act as I/O | 0 | 1 |

*Note: WDT frequency is always 16kHz, whatever the FSS bits are set.*

**Bits 12~7:** Not used, set to "0" all the time.

**Bits 6~4 (RCM2~RCM0):** IRC frequency selection.

 \* Corresponding with control register Bank0 RE RCM2~RCM0

| RCM2 | RCM1 | RCM0 | Frequency (MHz) |
|---|---|---|---|
| 0 | 0 | 0 | 4 (default) |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 12 |
| 1 | 0 | 1 | 16 |
| 1 | 1 | 0 | 20 |
| 1 | 1 | 1 | N/A |

**Bits 3~1 (OSC2~OSC0):** Main-oscillator mode selection bits.

| Main-oscillator mode | OSC2 | OSC1 | OSC0 |
|---|---|---|---|
| IRC (Internal RC oscillator mode) (default)<br>RCOUT (P80) acts as I/O pin | 0 | 0 | 0 |
| IRC (Internal RC oscillator mode)<br>RCOUT (P80) acts as clock output pin | 0 | 0 | 1 |
| HXT1 (High XTAL1 oscillator mode)<br>Frequency range: 12~20 MHz | 0 | 1 | 0 |
| HXT2(High XTAL2 oscillator mode)<br>Frequency range: 6~12 MHz | 0 | 1 | 1 |
| XT (XTAL oscillator mode)<br>Frequency range: 1~6 MHz | 1 | 0 | 0 |
| LXT1 (Low XTAL1 oscillator mode)<br>Frequency range: 100K~1MHz | 1 | 0 | 1 |
| LXT2 (Low XTAL2 oscillator mode)<br>Frequency range: 32.768kHz | 1 | 1 | 0 |
| Reserve | 1 | 1 | 1 |

**Bit 0 (RCOUT):** System Clock Output Enable Bit in IRC mode

      0: RCOUT output instruction cycle time (default)

      1: RCOUT pin is open drain

### 6.16.3  Code Option Register (Word 2)

| Mnemonic | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit11 | Bit10 | Bit9 | Bit8 |
|---|---|---|---|---|---|---|---|---|
| | **Word 2** | | | | | | | |
| | - | SHEN | - | - | - | - | - | - |
| 1 | High | Disable | - | - | - | - | - | - |
| 0 | Low | Enable | - | - | - | - | - | - |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Mnemonic | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | IRCPSS | - | - | I2COPT | - | - | - | - |
| 1 | VDD | - | - | High | - | - | - | - |
| 0 | Int. Vref | - | - | Low | - | - | - | - |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 15:** Not used, set to "0" all the time.

**Bit 14 (SHEN):** System hold enable bit.

> 0: Enable

> 1: Disable

**Bits 13~8:** Not used, set to "0" all the time.

**Bit 7 (IRCPSS):** IRC Power Source Selection

> 0: Internal reference (default)

> 1: VDD

**Bits 6~5:** Not used, set to "0" all the time.

**Bit 4 (I2COPT):** I2C optional bit. It is used to switch the pin position of I2C function.

> 0: Placed I2C pins in P62 (SDA0) and P82 (SCL0) (default)

> 1: Placed I2C pins in P84 (SDA1) and P83 (SCL1).

> *Corresponding with control register Bank 0 R31 I2COPT

**Bits 3~0:** Not used, set to "0" all the time.

### 6.16.4  Code Option Register (Word 3)

| Mnemonic | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit11 | Bit10 | Bit9 | Bit8 |
|---|---|---|---|---|---|---|---|---|
| | **Word 3** | | | | | | | |
| | - | EFTIM | - | - | ADFM | - | - | - |
| 1 | High | Heavy | High | High | High | High | High | High |
| 0 | Low | Light | Low | Low | Low | Low | Low | Low |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Mnemonic | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | - | TBWEN | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 1 | High | Enable | | | | | | |
| 0 | Low | Disable | | | Customer ID | | | |
| Default | 0 | 0 | | | | | | |

**Bit 15:** Not used, set to "0" all the time.

**Bit 14 (EFTIM):** Low Pass Filter (0: heavy, 1: light)

  0: Pass ~ 25 MHz (light LPS) (default)

  1: Pass ~ 10 MHz (heavy LPS)

**Bits 13~12:** Not used, set to "0" all the time.

**Bit 11 (ADFM):** This bit controls the format of AD data buffer (ADDH and ADDL), Refer to the following table

| ADFM | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 12 bits | 0 | ADDH | | | | | ADD11 | ADD10 | ADD9 | ADD8 |
| | | ADDL | ADD7 | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| | 1 | ADDH | ADD11 | ADD10 | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 |
| | | ADDL | | | | | ADD3 | ADD2 | ADD1 | ADD0 |

*Note: There is no use to have the hardware bit set to 0. As ADFM=0 and when*

  *12-bit resolution, ADDH<7:4> = 0000.*

**Bits 10~7:** Not used, set to "0" all the time.

**Bit 6 (TBWEN):** Table Write Enable bit.

  0: Disable (default)

  1: Enable

**Bits 5~0 (ID5~ID0):** Customer's ID Code

## 6.17 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

"LCALL", "LJMP" , or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA","SJC","SJNC","SJZ","SJNZ") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

| Mnemonic | Operation | Status Affected |
|----------|-----------|-----------------|
| NOP | No Operation | None |
| DAA | Decimal Adjust A | C |
| SLEP | 0 → WDT, Stop oscillator | T, P |
| WDTC | 0 → WDT | T, P |
| ENI | Enable Interrupt | None |
| DISI | Disable Interrupt | None |
| RET | [Top of Stack] → PC | None |
| RETI | [Top of Stack] → PC, Enable Interrupt | None |
| RESET | Software Device Reset | ALL Registers = Reset Value Flags* = Reset Value |

| Mnemonic | Operation | Status Affected |
|---|---|---|
| TBWR | Table Writer Start instruction | None |
| INT k | PC+1 → [SP], k*2 → PC | None |
| BTG R,b | Bit Toggle R ; /(R<b>)->R<b> *Range R5~RA | None |
| MOV R,A | A → R | None |
| CLRA | 0 → A | Z |
| CLR R | 0 → R | Z |
| SUB A,R | R-A → A | Z,C,DC,OV,N |
| SUB R,A | R-A → R | Z,C,DC,OV,N |
| DECA R | R-1 → A | Z,C,DC,OV,N |
| DEC R | R-1 → R | Z,C,DC,OV,N |
| OR A,R | A ∨ R → A | Z, N |
| OR R,A | A ∨ R → R | Z, N |
| AND A,R | A & R → A | Z, N |
| AND R,A | A & R → R | Z, N |
| XOR A,R | A ⊕ R → A | Z, N |
| XOR R,A | A ⊕ R → R | Z, N |
| ADD A,R | A + R → A | Z, C, DC, OV, N |
| ADD R,A | A + R → R | Z, C, DC, OV, N |
| MOV A,R | R → A | Z |
| MOV R,R | R → R | Z |
| COMA R | /R → A | Z, N |
| COM R | /R → R | Z, N |
| INCA R | R+1 → A | Z, C, DC, OV, N |
| INC R | R+1 → R | Z, C, DC, OV, N |
| DJZA R | R-1 → A, skip if zero | None |
| DJZ R | R-1 → R, skip if zero | None |
| RRCA R | R(n) → A(n-1), R(0) → C, C → A(7) | C, N |
| RRC R | R(n) → R(n-1), R(0) → C, C → R(7) | C, N |
| RLCA R | R(n) → A(n+1), R(7) → C, C → A(0) | C, N |

| Mnemonic | Operation | Status Affected |
|----------|-----------|-----------------|
| RLC R | R(n) → R(n+1), <br> R(7) → C, C → R(0) | C, N |
| SWAPA R | R(0-3) → A(4-7), <br> R(4-7) → A(0-3) | None |
| SWAP R | R(0-3) ↔ R(4-7) | None |
| JZA R | R+1 → A, skip if zero | None |
| JZ R | R+1 → R, skip if zero | None |
| BC R,b | 0 → R(b) | None <Note 2> |
| BS R,b | 1 → R(b) | None <Note 3> |
| JBC R,b | if R(b)=0, skip | None |
| JBS R,b | if R(b)=1, skip | None |
| CALL k | PC+1 → [SP], <br> (Page, k) → PC | None |
| JMP k | (Page, k) → PC | None |
| MOV A,k | k → A | None |
| JE R | Compare R with ACC, Skip = | None |
| JGE R | Compare R with ACC, Skip > | None |
| JLE R | Compare R with ACC Skip < | None |
| OR A,k | A ∨ k → A | Z, N |
| JE k | Compare K with ACC, Skip = | None |
| TBRDA R | ROM[(TABPTR)] → R, A <br> A ← program code (low byte) ; <br> R ← program code (high byte) | None |
| AND A,k | A & k → A | Z, N |
| SJC k | Jump to K if Carry <br> *Range [Address+127~-128] | None |
| SJNC k | Jump to K if Not Carry <br> *Range [Address+127~-128] | None |
| SJZ k | Jump to K if Zero <br> *Range [Address+127~-128] | None |
| XOR A,k | A ⊕ k → A | Z, N |
| SJNZ k | Jump to K if Not Zero <br> *Range [Address+127~-128] | None |

| Mnemonic | Operation | Status Affected |
|----------|-----------|-----------------|
| RRA R | R(n) → A(n-1), R(0) → A(7) | N |
| RR R | R(n) → R(n-1), R(0) → R(7) | N |
| RETL k | k → A,<br>[Top of Stack] → PC | None |
| XCH R | R ⟷ A | None |
| RLA R | R(n) → A(n+1), R(7) → A(0) | N |
| RL R | R(n) → R(n+1), R(7) → R(0) | N |
| SUB A,k | k-A → A | Z, C, DC, OV, N |
| SUBB A,R | R-A-/C → A | Z, C, DC, OV, N |
| SUBB R,A | R-A-/C → R | Z, C, DC, OV, N |
| SBANK k | K->R1(5:4) | None |
| GBANK k | K->R1(1:0) | None |
| LCALL k | Next instruction : k kkkk kkkk kkkk<br>PC+1→[SP], k→PC | None |
| LJMP k | Next instruction : k kkkk kkkk kkkk<br>K→PC | None |
| TBRD R | ROM[(TABPTR)] → R | None |
| ADD A,k | k+A → A | Z,C,DC,OV,N |
| NEG R | 2's complement, /R +1 → R | Z,C,DC,OV,N |
| ADC A,R | A+R+C → A | Z,C,DC,OV,N |
| ADC R,A | A+R+C → R | Z,C,DC,OV,N |

# 7 Absolute Maximum Ratings

| Items | Rating | | |
|---|---|---|---|
| Storage temperature | -65°C | to | 150°C |
| Input voltage | Vss-0.3V | to | Vdd+0.5V |
| Output voltage | Vss-0.3V | to | Vdd+0.5V |
| Working Voltage | 2.1V$^{(1)}$ | to | 5.5V |
| | 2.4V$^{(2)}$ | to | 5.5V |
| Working Frequency | DC | to | 20 MHz |

$^{(1)}$ 2.1V~5.5V at 0°C ~70°C (Commercial)
$^{(2)}$ 2.4V~5.5V at -40°C ~85°C (Industrial)

# 8 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Fxt | XTAL: VDD to 3V | Two cycles with two clocks | DC | 16 | – | MHz |
| | XTAL: VDD to 5V | | DC | 20 | – | MHz |
| | IRC: VDD to 5V | 4 MHz, 1 MHz, 6MHz, 8MHz, 16 MHz, 20 MHz | – | F | – | Hz |
| IRCE | Internal RC oscillator error per stage | – | – | ±1 | – | % |
| IRC1 | IRC:VDD to 5V | RCM2~RCM0=000 | – | 4 | – | MHz |
| IRC2 | IRC:VDD to 5V | RCM2~RCM0=001 | – | 1 | – | MHz |
| IRC3 | IRC:VDD to 5V | RCM2~RCM0=010 | – | 6 | – | MHz |
| IRC4 | IRC:VDD to 5V | RCM2~RCM0=011 | – | 8 | – | MHz |
| IRC5 | IRC:VDD to 5V | RCM2~RCM0=100 | – | 12 | – | MHz |
| IRC6 | IRC:VDD to 5V | RCM2~RCM0=101 | – | 16 | – | MHz |
| IRC7 | IRC:VDD to 5V | RCM2~RCM0=110 | – | 20 | – | MHz |
| IIL | Input Leakage Current for input pins | VIN = VDD, VSS | -1 | 0 | 1 | µA |
| VIH1 | Input High Voltage (Schmitt trigger) | Ports 5, 6, 7, 8, 9, A | 0.7VDD | – | VDD+0.3V | V |
| VIL1 | Input Low Voltage (Schmitt trigger) | Ports 5, 6, 7, 8, 9, A | -0.3V | – | 0.3VDD | V |
| VIHT1 | Input High Threshold Voltage (Schmitt trigger ) | /RESET | 0.7VDD | – | VDD+0.3V | V |
| VILT1 | Input Low Threshold Voltage (Schmitt trigger ) | /RESET | -0.3V | – | 0.3VDD | V |
| IOH1 | Output High Voltage (Ports 5, 6, 7, 8, 9, A) | VOH = VDD-0.1VDD | -2.6 | -3.7 | – | mA |
| | Output High Voltage (Ports 5, 6, 8, 9, A) | VOH = VDD-0.3VDD | – | -8 | – | mA |
| IOH2 | Output High Voltage(Hi Drive) (Ports 5, 6, 8) | VOH = VDD-0.1VDD | -7.3 | -11 | – | mA |
| | Output High Voltage(Hi Drive) (Ports 5, 6, 8) | VOH = VDD-0.3VDD | – | -24 | – | mA |
| IOL1 | Output Low Voltage (Ports 5, 6, 8) | VOL = GND+0.1VDD | 12.6 | 18 | – | mA |
| | Output Low Voltage (Ports 5, 6, 8) | VOL = GND+0.3VDD | – | 32 | – | mA |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| IOL2 | Output Low Voltage(Hi Sink) (Ports 50-57, 60) | VOL = GND+0.1VDD | 28 | 41 | – | mA |
| | Output Low Voltage(Hi Sink) (Ports 61-64, 80-84) | | 35 | 50 | – | mA |
| | Output Low Voltage(Hi Sink) (Ports 50-57, 60) | VOL = GND+0.3VDD | – | 90 | – | mA |
| | Output Low Voltage(Hi Sink) (Ports 61-64, 80-84) | | – | 100 | – | mA |
| IPH | Pull-high current | Pull-high active, input pin at VSS | *33* | 51.5 | 70 | µA |
| IPL | Pull-low current | Pull-low active, input pin at VDD | 11 | 17 | 23 | µA |
| ISB1 | Power down current (Sleep mode) | /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT disabled | – | 1 | – | µA |
| ISB2 | Power down current (Sleep mode) | /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT enabled | – | 5 | – | µA |
| ISB3 | Power down current (Idle mode) | /RESET= 'High', Fm off, Fs=128kHz (IRC type) output pin floating, WDT disabled, | – | 7.5 | – | µA |
| ISB4 | Power down current (Idle mode) | /RESET= 'High', Fm off, Fs=128kHz (IRC type), output pin floating, WDT enabled | – | 7.5 | – | µA |
| ICC1 | Operating supply current (Green mode) | /RESET= 'High', Fm off, Fs=128KHz (IRC type), output pin floating, WDT disabled | – | 90 | – | µA |
| ICC2 | Operating supply current (Green mode) | /RESET= 'High', Fm off, Fs=128kHz (IRC type), output pin floating, WDT enabled | – | 90 | – | µA |
| ICC3 | Operating supply current (Green mode) | /RESET= 'High', Fm off, HLP=0,Fs=32.768KHz (Crystal type), output pin floating, WDT enabled | – | 30 | – | µA |
| ICC4 | Operating supply current (Normal mode) | /RESET= 'High', Fm=4 MHz (IRC type), Fs on, output pin floating, WDT enabled | – | 1200 | – | µA |
| ICC5 | Operating supply current (Normal mode) | /RESET= 'High', Fm =4 MHz (Crystal type), Fs on, output pin floating, WDT enabled | – | 1500 | – | µA |
| ICC6 | Operating supply current (Normal mode) | /RESET= 'High', Fm =12 MHz (IRC type), Fs on, output pin floating, WDT enabled | – | 3000 | – | µA |
| ICC7 | Operating supply current (Normal mode) | /RESET= 'High', Fm =16 MHz (IRC type), Fs on, output pin floating, WDT enabled | – | 3700 | – | µA |
| ICC8 | Operating supply current (Normal mode) | /RESET= 'High', Fm=16 MHz (Crystal type), Fs on, output pin floating, WDT enabled | – | 5000 | – | µA |

*Note:* These parameters are theoretical values and have not been tested. Such parameters are for design reference only.

Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C.

**Program Flash Memory Electrical Characteristics** (VDD=2.4V to 5.5V, VSS=0V,
Ta = -40 to 85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| Tprog | Erase/Write cycle time | | - | 1 | - | ms |
| Treten | Data Retention | Vdd = 5.0V | - | 10 | - | Years |
| Tendu | Endurance time | | - | 100K | - | Cycles |

**A/D Converter Characteristics** (VDD=2.4V to 5.5V, VSS=0V, Ta = -40 to 85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| Operating Range | Vdd | For 5.5V Fs=100kHz, Fin=2kHz, For 2.4V Fs=50kHz, Fin=1kHz | 2.4 | - | 5.5 | V |
| | $V_{REFT}$ | | 2.4 | - | Vdd | V |
| Current Consumption | Ivdd | $V_{REFT}$= Vdd=5.5v, Fs=100kHz, Fin=2kHz | - | - | 0.7 | mA |
| | Iref | | - | - | 100 | μA |
| Standby Current | Isb | | - | - | 0.1 | μA |
| ZAI | ZAI | | - | - | 10k | Ω |
| SNR | SNR | $V_{REFT}$= Vdd=3.3V Fs=100kHz, Fin=2kHz | 70 | - | - | dBc |
| THD | THD | $V_{REFT}$= Vdd=3.3V Fs=100kHz, Fin=2kHz | - | - | -70 | dBc |
| SNDR | SNDR | $V_{REFT}$= Vdd=3.3V, Fs=100kHz, Fin=2kHz | 68 | - | - | dBc |
| Worst Harmonic | WH | $V_{REFT}$= Vdd=3.3V Fs=100KHz, Fin=2kHz | - | - | -73 | dBc |
| SFDR | SFDR | $V_{REFT}$= Vdd=3.3V, Fs=100kHz, Fin=2kHz | 73 | - | - | dBc |
| Offset Error | OE | $V_{REFT}$= Vdd=3.3V Fs=100kHz | - | - | ±4 | LSB |
| Gain Error | GE | $V_{REFT}$= Vdd=3.3V Fs=100kHz | - | - | ±8 | LSB |
| DNL | DNL | $V_{REFT}$= Vdd=3.3V Fs=100KHz, Fin=2kHz | - | - | ±1 | LSB |
| INL | INL | $V_{REFT}$= Vdd=3.3V Fs=100KHz, Fin=2kHz | - | - | ±4 | LSB |
| Conversion Rate | Fs1 | Vdd=2.7~5.5V, Fin=2kHz | 100 | - | - | KSPS |
| | Fs2 | Vdd=2.2~2.7V, (Ta = 0 to 70°C) Fin=1kHz | 50 | - | - | KSPS |
| | Fs3 | Vdd=2.1~2.2V, (Ta = 0 to 70°C) Fin=1kHz | 25 | - | - | KSPS |
| Power Supply Rejection Ratio | PSRR | $V_{REFT}$=2.1V Vdd=2.1V ~ 5.5V Fs=50kHz, Vin=0V ~ 2.1V (Ta = 0 to 70°C) | - | - | 2 | LSB |

**Note:** [1]*These parameters are hypothetical (not tested) and are provided for design reference only.*
[2]*There is no current consumption when ADC is off other than minor leakage current.*
[3]*The A/D conversion result will not decrease with an increase in the input voltage, and has no missing code.*
[4]*These parameters are subject to change without prior notice.*

**Touch Key Characteristics** (VDD=2.4V to 5.5V, VSS=0V, Ta = -40 to 85°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| VDD | Supply voltage | - | 2.4 | 5 | 5.5 | V |
| Iss | Supply current | VDD=5V, 10pF, 10.5μA Charge Discharge Current | - | 660 | - | μA |
| Top | Operating temperature | - | -40 | 25 | 85 | C |
| Iarray | Current source | VDD=5V | 3 | - | 36 | μA |
| Ftpout | Oscillator Output frequency | C$_s$@50pf+Imin~5pF+Imax VDD=5V | 65k | - | 36M | Hz |
| Cs | Capacitance of sensor | Total capacitance | 5 | | 50 | pF |

**Note:** These parameters are theoretical values and have not been tested.  Such parameters are for design
reference only.

Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on
characterization results at 25°C.

# 9 AC Electrical Characteristics

EM88F752N, (-40 $\leq$ Ta $\leq$ 85$^{\circ}$C, VDD=5V, VSS=0V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| Dclk | Input CLK duty cycle | – | 45 | 50 | 55 | % |
| Tins | Instruction cycle time | Crystal type | 100 | – | DC | ns |
|      |                        | RC type | 100 | – | DC | ns |
| Ttcc | TCC input period | – | (Tins+20)/N* | – | – | ns |
| Tdrh | Device reset hold time | – | 11.8 | 16.8 | 21.8 | ms |
| Trst | /RESET pulse width | Ta = 25$^{\circ}$C | 2000 | – | – | ns |
| Twdt | Watchdog timer period | Ta = 25$^{\circ}$C | 11.8 | 16.8 | 21.8 | ms |
| Tset | Input pin setup time | – | – | 0 | – | ns |
| Thold | Input pin hold time | – | – | 20 | – | ns |
| Tdelay | Output pin delay time | Cload=20pF | – | 50 | – | ns |

*Note: These parameters are theoretical values and have not been tested. Such parameters are for design reference only.*

*Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25$^{\circ}$C.*

*\* N = selected prescaler ratio*

# APPENDIX

## A    Ordering and Manufacturing Information

EM88F752ND20UJ

**Material Type**
UJ: RoHS complied

**Pin Number**

**Package Type**
D  : DIP
SO: SOP
SS: SSOP

**Specific Annotation**
N: Industrial Grad

**Product Number**

**Product Type**
F: Flash

**Elan 8-bit Product**
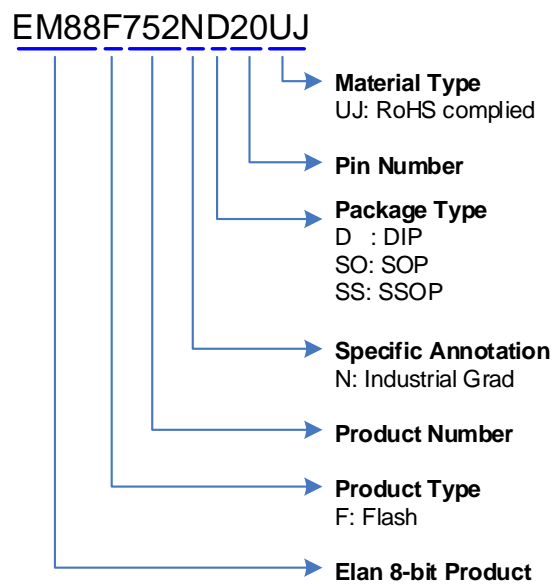
For example:

EM88F752ND20UJ

is EM88F752N with Flash program memory, industrial grade product,
in 20-pin DIP package with RoHS complied

EM88Faaaa
1041 bbbbbb

**Elan Product Number**

**Batch Number**

**Manufacture Date**
"YYWW"
YY is year and WW is week
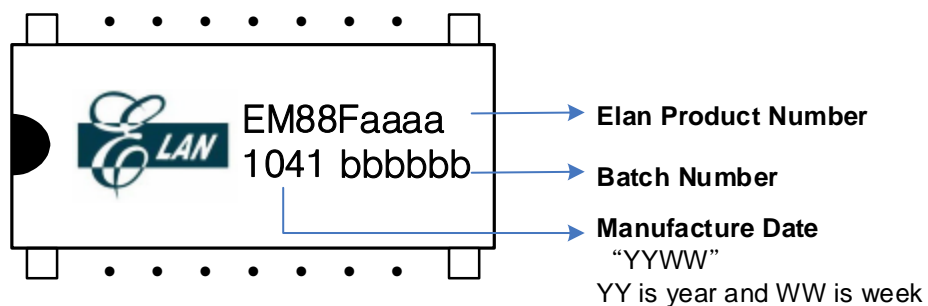
# B   Package Type

| Flash MCU | Package Type | Pin Count | Package Size |
|---|---|---|---|
| EM88F752NSO20UJ | SOP | 20 | 300mil |
| EM88F752ND20UJ | DIP | 20 | 300mil |
| EM88F752NSS20UJ | SSOP | 20 | 209mil |
| EM88F752ND16UJ / AD16UJ | DIP | 16 | 300mil |
| EM88F752NSS16UJ / ASS16UJ | SSOP | 16 | 150mil |
| EM88F752NSO16UJ / ASO16UJ | SOP | 16 | 150mil |

For Product Code "J" or "U".

These are Green products and comply with RoHS specifications.

| Part No. | EM88F752NxJ |
|---|---|
| Electroplate type | Pure Tin |
| Ingredient (%) | Sn:100% |
| Melting point (°C) | 232°C |
| Electrical resistivity ( μΩ-cm ) | 11.4 |
| Hardness (hv) | 8~10 |
| Elongation (%) | >50% |

# C   Package Information

## C.1   EM88F752NSO20UJ



| Symbol | Min. | Normal | Max. |
|--------|------|--------|------|
| A | 2.350 | | 2.650 |
| A1 | 0.102 | | 0.300 |
| b | | 0.406(TYP) | |
| c | 0.230 | | 0.320 |
| E | 7.400 | | 7.600 |
| H | 10.000 | | 10.650 |
| D | 12.600 | | 12.900 |
| L | 0.630 | 0.838 | 1.100 |
| e | | 1.27(TYP) | |
| θ | 0 | | 8 |

TITLE:
SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO20

Edtion: A

Unit : mm

Scale: Free

Material:

Sheet:1 of 1
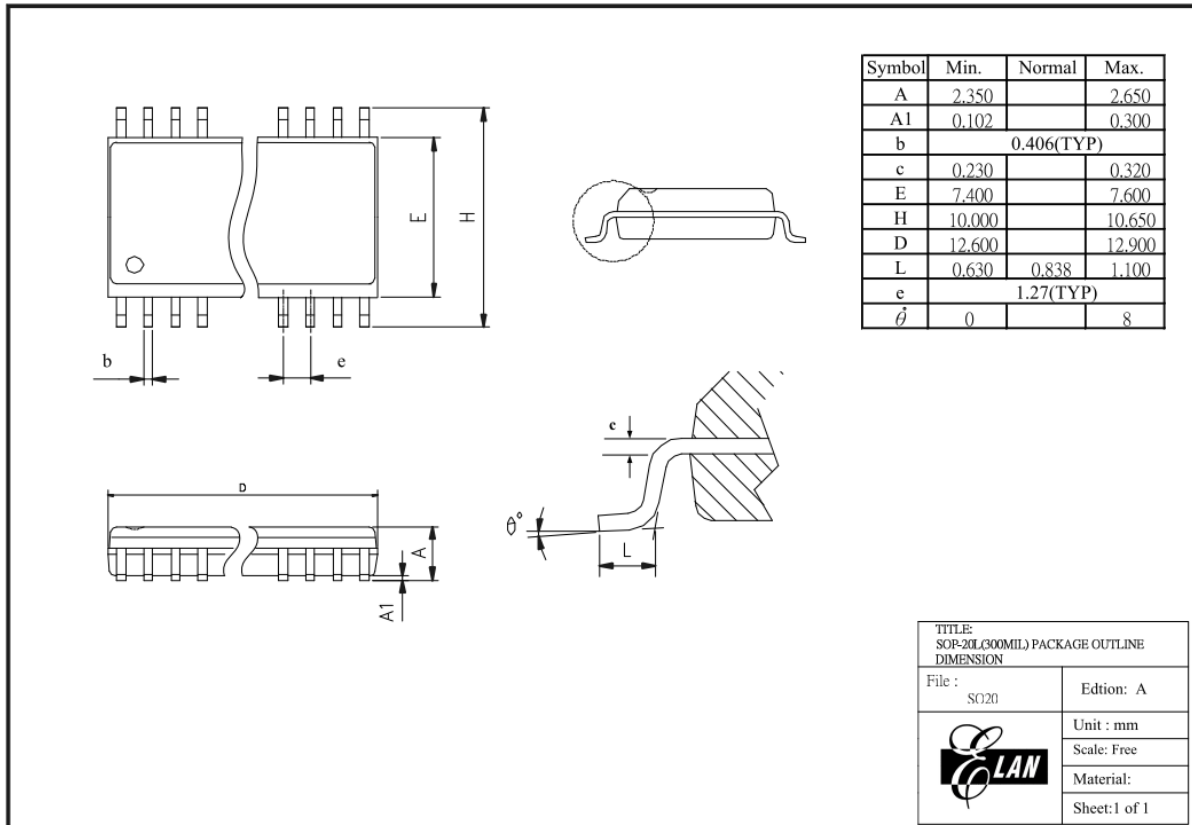
*Figure C-1   EM88F752N 20-pin SOP Package Type*

## C.2    EM88F752ND20UJ



| Symbol | Min | Normal | Max |
|--------|-----|--------|-----|
| A | | | 4.450 |
| A1 | 0.381 | | |
| A2 | 3.175 | 3.302 | 3.429 |
| c | 0.203 | 0.254 | 0.356 |
| D | 25.883 | 26.060 | 26.237 |
| E1 | 6.220 | 6.438 | 6.655 |
| E | 7.370 | 7.620 | 7.870 |
| eB | 8.510 | 9.020 | 9.530 |
| B | 0.356 | 0.457 | 0.559 |
| B1 | 1.143 | 1.524 | 1.778 |
| L | 3.048 | 3.302 | 3.556 |
| e | 2.540(TYP) | | |
| θ | 0 | | 15 |

TITLE:
PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION

File :
D20

Edtion:  A

Unit : mm

Scale: Free

Material:

Sheet:1 of 1
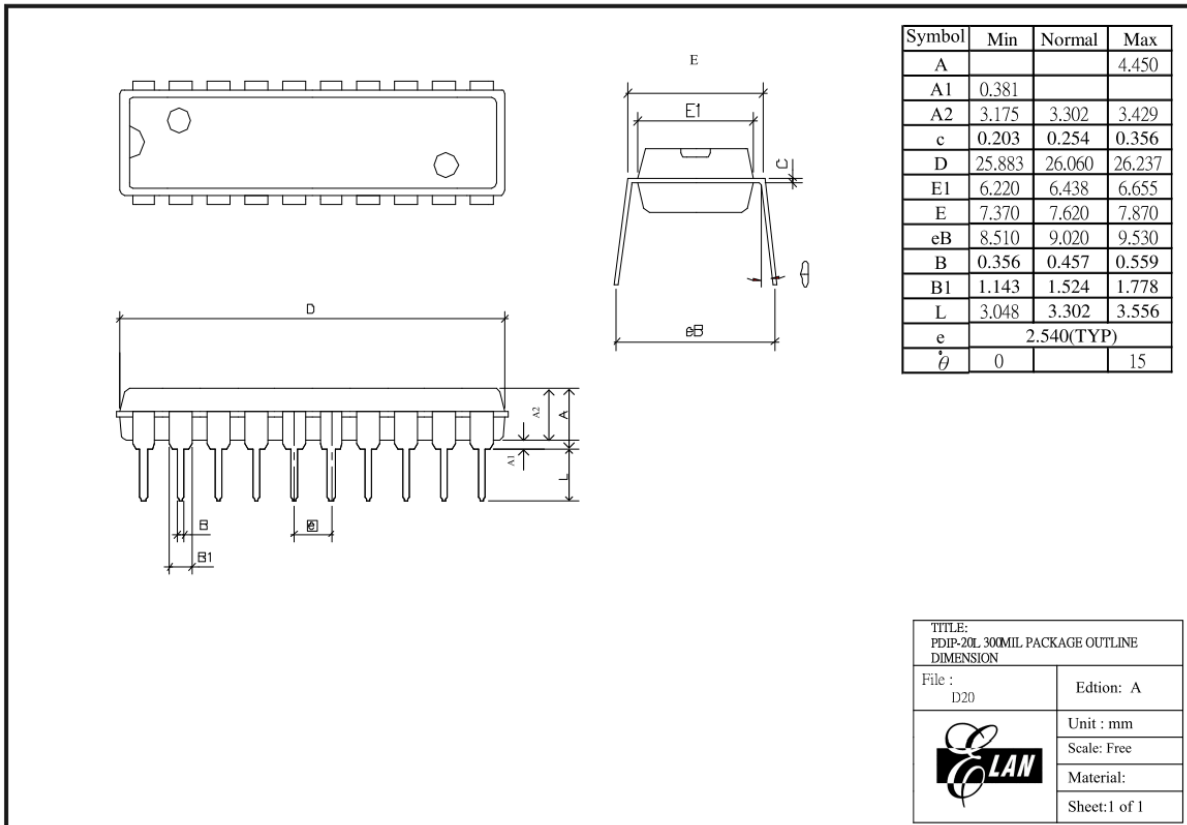
*Figure C-2    EM88F752N 20-pin DIP Package Type*

## C.3   EM88F752NSS20UJ



| Symbol | Min. | Normal | Max. |
|--------|------|--------|------|
| A | | | 2.130 |
| A1 | 0.050 | | 0.250 |
| A2 | 1.620 | 1.750 | 1.880 |
| b | 0.220 | | 0.380 |
| c | 0.090 | | 0.200 |
| E | 7.400 | 7.800 | 8.200 |
| E1 | 5.000 | 5.300 | 5.600 |
| D | 6.900 | 7.200 | 7.500 |
| L | 0.650 | 0.750 | 0.850 |
| L1 | 1.250(REF ) | | |
| e | 0.650(TYP) | | |
| $\theta$ | 0 | 4 | 8 |

TITLE:
SSOP-20L(209MIL) PACKAGE OUTLINE DIMENSION

File : SSOP20

Edtion:  A

Unit : mm

Scale: Free

Material:

Sheet:1 of 1
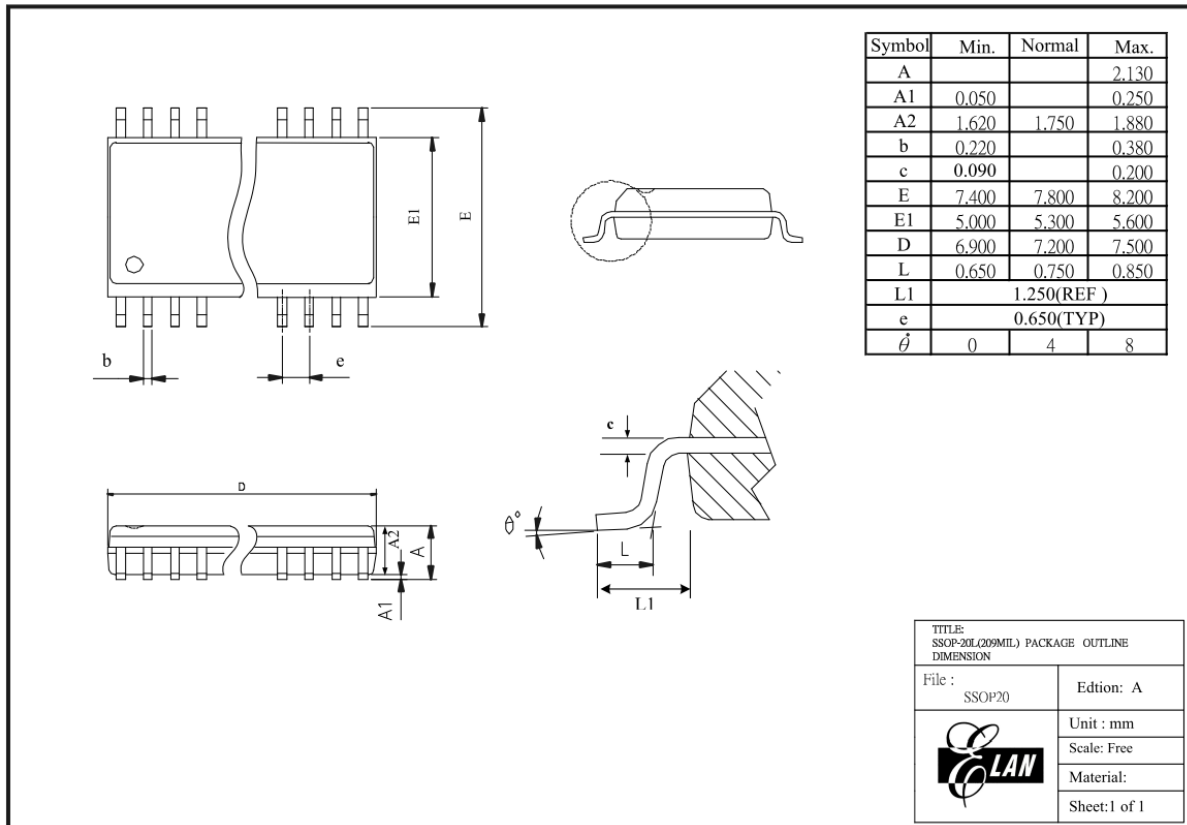
*Figure C-3   EM88F752N 20-pin SSOP Package Type*

## C.4   EM88F752ND16UJ/AD16UJ



| Symbol | Min | Normal | Max |
|--------|-----|--------|-----|
| A | | | 4.318 |
| A1 | 0.381 | | |
| A2 | 3.175 | 3.302 | 3.429 |
| c | 0.203 | 0.254 | 0.356 |
| D | 19.000 | 19.050 | 19.100 |
| E | 6.174 | 6.401 | 6.628 |
| E1 | 7.370 | 7.620 | 7.870 |
| eB | 8.510 | 9.020 | 9.530 |
| B | 0.356 | 0.457 | 0.559 |
| B1 | 1.143 | 1.524 | 1.778 |
| L | 3.048 | 3.302 | 3.556 |
| e | 2.540(TYP) | | |
| $\theta$ | 0 | | 15 |

TITLE:
PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION

| File : ID16 | Edtion:  A |
|-------------|------------|
| | Unit : mm |
| | Scale: Free |
| | Material: |
| | Sheet:1 of 1 |
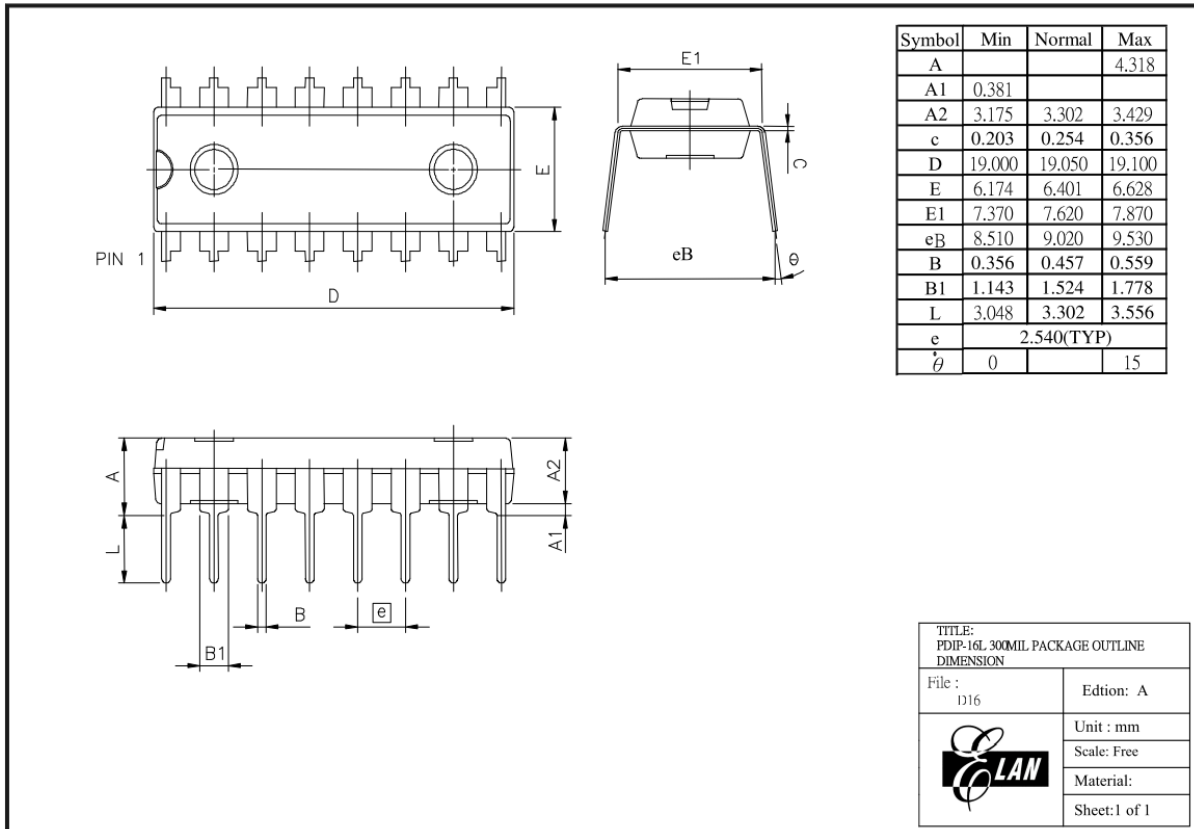
*Figure C-4   EM88F752N 16-pin DIP Package Type*

## C.5   EM88F752NSO16UJ/ASO16UJ



| Symbol | Min. | Normal | Max. |
|--------|------|--------|------|
| A | 1.350 | | 1.750 |
| A1 | 0.100 | | 0.250 |
| A2 | 1.300 | 1.400 | 1.500 |
| b | 0.330 | | 0.510 |
| c | 0.190 | | 0.250 |
| E | 3.800 | | 4.000 |
| H | 5.800 | | 6.200 |
| D | 9.800 | | 10.000 |
| L | 0.600 | | 1.270 |
| e | | 1.27 (TYP) | |
| θ° | 0 | | 8 |

TITLE:
SOP-16L(150MIL) PACKAGE OUTLINE DIMENSION

File : NSO16       Edtion:  A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1
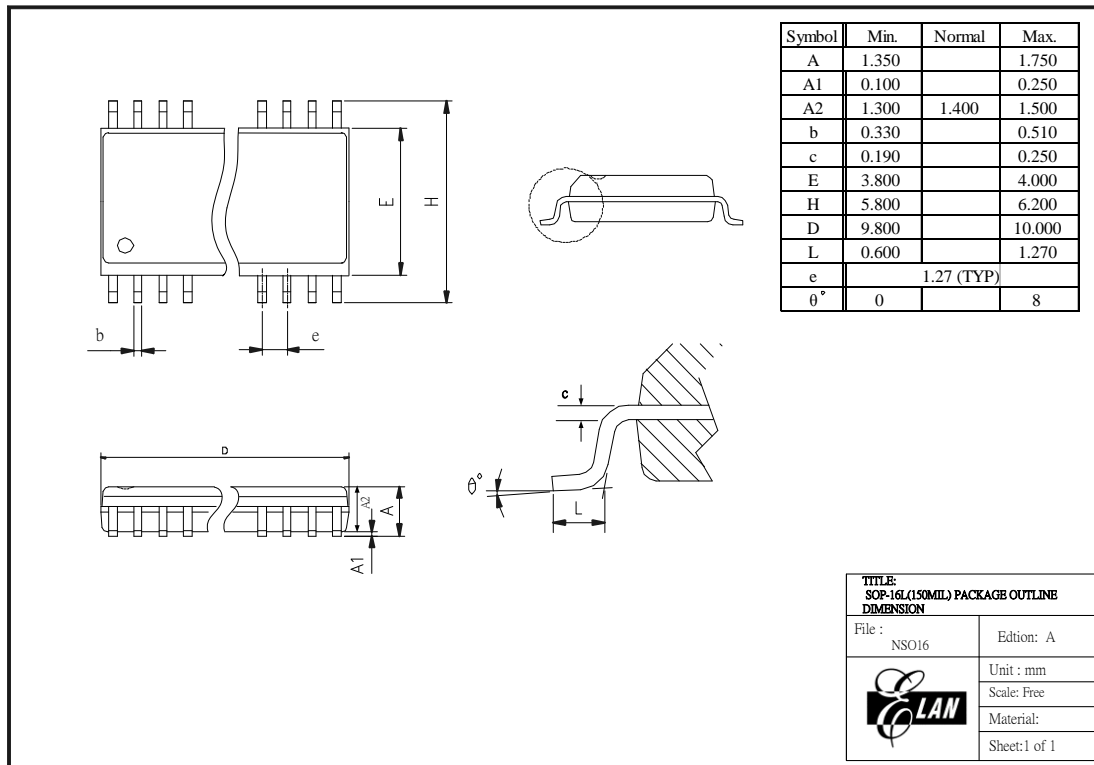
*Figure C-5   EM88F752N 16-pin SOP Package Type*

## C.6    EM88F752NSS16UJ/ASS16UJ



Package Type : SSOP-16L

| Symbol | EMC(mm ) | | |
|--------|------|--------|------|
| | Min | Normal | Max |
| A | 1.35 | 1.63 | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | - | - | 1.50 |
| b | 0.20 | - | 0.30 |
| b1 | 0.20 | 0.25 | 0.28 |
| c | 0.18 | - | 0.25 |
| c1 | 0.18 | 0.20 | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.79 | 5.99 | 6.20 |
| E1 | 3.81 | 3.91 | 3.99 |
| L | 0.41 | 0.64 | 1.27 |
| e | 0.635BASIC | | |
| θ | 0° | - | 8° |

TITLE:
SSOP 16L (150MIL)PACKAGE OUTLINE DIMENSION

| File :<br>SSOP 16L | Edtion:  A |
|---|---|
| | Unit : mm |
| | Scale: Free |
| | Material: |
| | Sheet:1 of 1 |

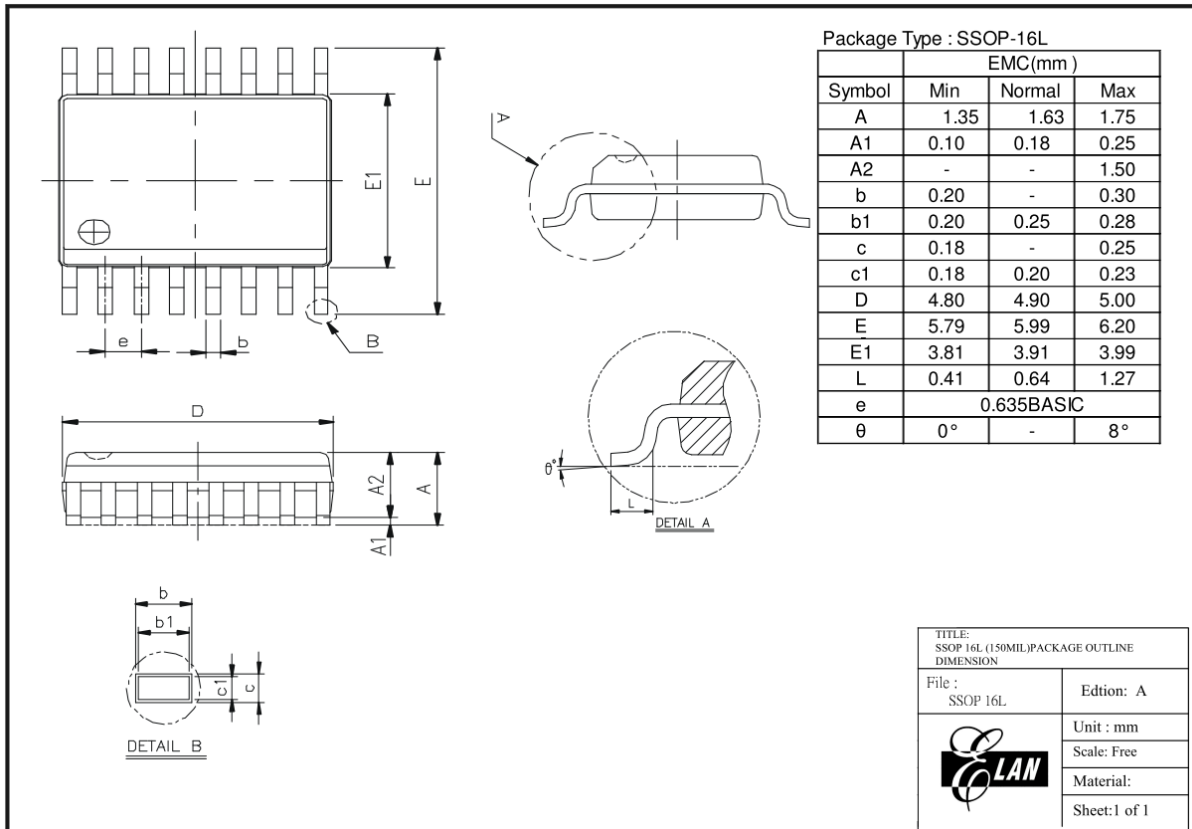*Figure C-6    EM88F752N 16-pin SSOP Package Type*

# D  Quality Assurance and Reliability

| Test Category | Test Conditions | Remarks |
|---|---|---|
| Solderability | Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux | |
| Pre-condition | Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles<br>Step 2: Bake at 125°C, TD (endurance)=24 hrs<br>Step 3: Soak at 30°C/60% , TD (endurance)=192 hrs<br>Step 4: IR flow 3 cycles<br>(Pkg thickness $\geq$ 2.5mm or<br>Pkg volume $\geq$ 350 mm$^3$ ----225±5°C)<br>(Pkg thickness $\leq$ 2.5 mm or<br>Pkg volume $\leq$ 350 mm$^3$ ----240±5°C ) | For SMD IC (such as SOP, QFP, SOJ, etc) |
| Temperature cycle test | -65°C (15mins)~150°C (15min), 200 cycles | |
| Pressure cooker test | TA =121°C, RH=100%, pressure = 2 atm,<br>TD (endurance)= 96 hrs | |
| High temperature / High humidity test | TA=85°C , RH=85% , TD (endurance)=168 , 500 hrs | |
| High-temperature storage life | TA=150°C, TD (endurance)=500, 1000 hrs | |
| High-temperature operating life | TA=125°C, VDD=Max. operating voltage,<br>TD (endurance) =168, 500, 1000 hrs | |
| Latch-up | TA=25°C, VDD=Max. operating voltage, 800mA/40V | |
| ESD (HBM) | TA=25°C, $\geq$ \| ± 4KV \| | IP_ND,OP_ND,IO_ND<br>IP_NS,OP_NS,IO_NS |
| ESD (MM) | TA=25°C, $\geq$ \| ± 400V \| | IP_PD,OP_PD,IO_PD,<br>IP_PS,OP_PS,IO_PS,<br>VDD-VSS(+),<br>VDD_VSS(-) mode |

## D.1  Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

# E   EM88F752N Program Pin List

UWTR is used to program the EM88F752N IC's. The UWTR connector is selected through Table E-1. The software is selected by EM88F752N.

| UWTR-ADP | | UWTR-ADP109 | UWTR-ADP112 | UWTR-ADP113 |
|---|---|---|---|---|
| Program Pin Name | IC Pin Name | EM88F752NSO20UJ /D20UJ/SS20UJ Pin Number | EM88F752NSO16UJ /D16UJ/SS16UJ Pin Number | EM88F752NASO16UJ /D16UJ/SS16UJ Pin Number |
| 2W_SCL | P64 | 7 | 7 | 5 |
| 2W_SDA | P63 | 8 | 8 | 6 |
| VDD | VDD | 20 | 16 | 16 |
| VSS | VSS | 1 | 1 | 1 |

*Table E-1 EM88F752N Program Pin List*