

# 74LS393

## Counter

Dual 4-Bit Binary Ripple Counter  
*Product Specification*

### Logic Products

#### FEATURES

- Two 4-bit binary counters
- Divide-by any binary module up to 28 in one package
- Two Master Resets to clear each 4-bit counter individually

#### DESCRIPTION

The '393 is a Dual 4-bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock ( $\overline{CP}_a$  and  $\overline{CP}_b$ ) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74LS393	35MHz	15mA

#### ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS393N
Plastic SO-14	N74LS393D

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

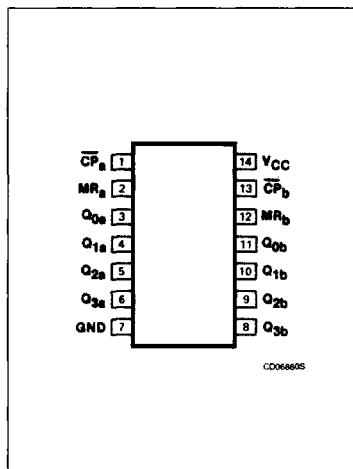
#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
MR	Master Reset input	1LSul
$\overline{CP}$	Clock input	4LSul
Q	Output	10LSul

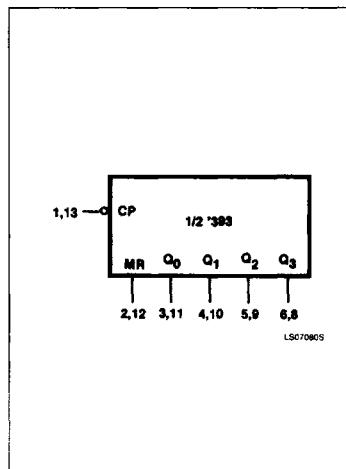
#### NOTE:

Where a 74LS unit load (LSul) is  $20\mu A$   $I_{IH}$  and  $-0.4mA$   $I_{IL}$ .

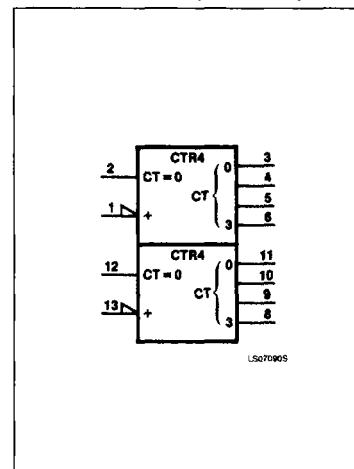
#### PIN CONFIGURATION



#### LOGIC SYMBOL



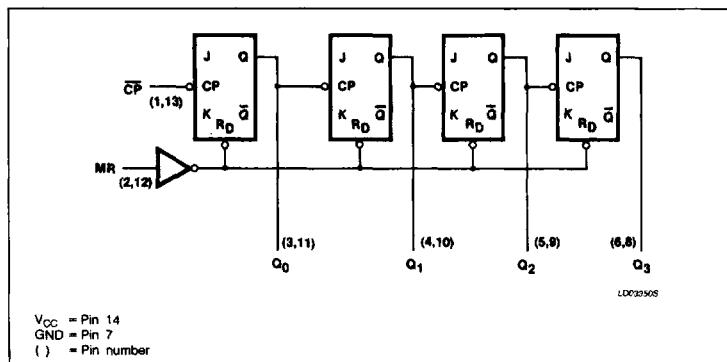
#### LOGIC SYMBOL (IEEE/IEC)



## Counter

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## LOGIC DIAGRAM



The Master Resets ( $MR_a$  and  $MR_b$ ) are active-HIGH asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

COUNT SEQUENCE  
FOR  $\frac{1}{2}$  THE '393

COUNT	OUTPUTS			
	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level

L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
$V_{CC}$	Supply voltage	7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +1	mA
$V_{OUT}$	Voltage applied to output in HIGH output state	-0.5 to + $V_{CC}$	V
$T_A$	Operating free-air temperature range	0 to 70	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			UNIT
	Min	Nom	Max	
$V_{CC}$	4.75	5.0	5.25	V
$V_{IH}$	HIGH-level input voltage	2.0		V
$V_{IL}$	LOW-level input voltage		+0.8	V
$I_{IK}$	Input clamp current		-18	mA
$I_{OH}$	HIGH-level output current		-400	μA
$I_{OL}$	LOW-level output current		8	mA
$T_A$	Operating free-air temperature	0	70	°C

## Counter

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**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>			74LS393		UNIT	
				Min	Typ <sup>2</sup>		
V <sub>OH</sub> HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>iH</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = MAX			2.7	3.4	V	
V <sub>OL</sub> LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>iH</sub> = MIN, V <sub>IL</sub> = MAX	I <sub>OL</sub> = MAX			0.35	V	
		I <sub>OL</sub> = 4mA (74LS)			0.25	0.4	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>i</sub> = I <sub>IK</sub>				-1.5	V	
I <sub>i</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX	V <sub>i</sub> = 7.0V	MR input		0.1	mA	
		V <sub>i</sub> = 5.5V	CP input		0.2	mA	
I <sub>iH</sub> HIGH-level input current	V <sub>CC</sub> = MAX, V <sub>i</sub> = 2.7V		MR input		20	μA	
			CP input		100	μA	
I <sub>iL</sub> LOW-level input current	V <sub>CC</sub> = MAX, V <sub>i</sub> = 0.4V		MR input		-0.4	mA	
			CP input		-1.6	mA	
I <sub>OS</sub> Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-20	-100	mA	
I <sub>CC</sub> Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX				15	26	mA

**NOTES:**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
3. I<sub>OS</sub> is tested with V<sub>OUT</sub> = +0.5V and V<sub>CC</sub> = V<sub>CC</sub> MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I<sub>CC</sub> with both MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and all outputs open.

**AC ELECTRICAL CHARACTERISTICS** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C <sub>L</sub> = 15pF, R <sub>L</sub> = 2kΩ		
		Min	Max	
f <sub>MAX</sub> CP input count frequency	Waveform 1	25		MHz
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay CP to Q <sub>0</sub>	Waveform 1		20 20	ns
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay CP to Q <sub>3</sub>	Waveform 1		60 60	ns
t <sub>PHL</sub> Propagation delay, MR to Q	Waveform 2		39	ns

**NOTE:**

Per industry convention, f<sub>MAX</sub> is the worst case value of the maximum device operating frequency with no constraints on t<sub>r</sub>, t<sub>f</sub>, pulse width or duty cycle.

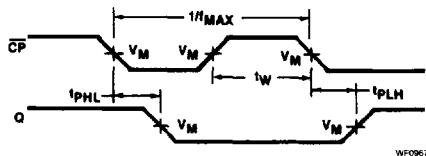
**AC SET-UP REQUIREMENTS** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		Min	Max	
t <sub>w</sub> CP pulse width	Waveform 1	20		ns
t <sub>w</sub> MR pulse width	Waveform 2	20		ns
t <sub>rec</sub> Recovery time, MR to CP	Waveform 2	25		ns

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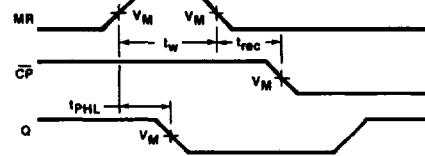
74LS393

## AC WAVEFORMS



$V_M = 1.5V$  for 74 and 74LS;  $V_M = 1.3V$  for 74LS.  
The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the appropriate Function Table.

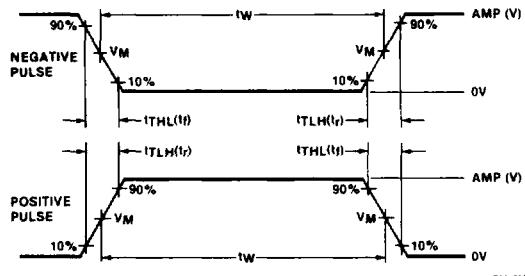
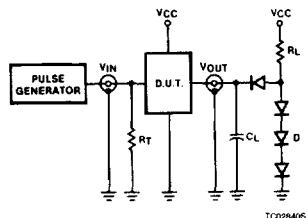
Waveform 1



$V_M = 1.5V$  for 74 and 74LS;  $V_M = 1.3V$  for 74LS.  
The number of clock pulses required between the  $t_{PLH}$  and  $t_{PHL}$  measurements can be determined from the appropriate Function Table.

Waveform 2

## TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$  for 74LS;  $V_M = 1.5V$  for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

## DEFINITIONS

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance;  
see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$   
of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$t_{PLH}$ ,  $t_{PHL}$  Values should be less than or equal to the table  
entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{PLH}$	$t_{PHL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns