SPECIFICATION

Customer: _____

Model Name: SAT040HS54DHY0-A0

SPEC NO.: _____

Date: _____

Version: _____

■Preliminary Specification

□Final Specification

Approved by	Comment

Approved by	Reviewed by	Prepared by
视安通 2014.09.09 吴金荣		

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2014/09/09		Initial Release

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	4.0 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	320 × 3(RGB) ×240	
4	Display mode	Normally White, Transmissive	
5	Pixel pitch	0.2565(H) X 0.2565(V) mm	
6	Active area	82.08(H) X 61.56(V) mm	
7	Outline dimensions	96.0(H) X 76.0(V) X 3.2(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	RGB/CCIR656/601	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

2. Pin Assignment

FPC Connector is used for the module electronics interface. The recommended model is FH12A-54S-0.5SH manufactured by Hirose

No	Symbol	I/O	Description	Remarks
1	LED_Cathode	P	LED_Cathode	
2	LED_Cathode	P	LED_Cathode	
3	LED_Anode	P	LED_ Anode	
4	LED_Anode	P	LED_Anode	
5	NC	--	No Connection	
6	NC	--	No Connection	
7	NC	--	No Connection	
8	RESET	I	Reset	
9	SPENA	I	Serial Port Data Enable Signal	
10	SPCK	I	SPI Serial Clock	
11	SPDA	I	SPI Serial Data Input	
12	DATA0	I	Data Bus	
13	DATA1	I	Data Bus	
14	DATA2	I	Data Bus	
15	DATA3	I	Data Bus	
16	DATA4	I	Data Bus	
17	DATA5	I	Data Bus	
18	DATA6	I	Data Bus	
19	DATA7	I	Data Bus	
20	DATA8	I	Data Bus	
21	DATA9	I	Data Bus	
22	DATA10	I	Data Bus	
23	DATA11	I	Data Bus	
24	DATA12	I	Data Bus	
25	DATA13	I	Data Bus	
26	DATA14	I	Data Bus	
27	DATA15	I	Data Bus	
28	DATA16	I	Data Bus	
29	DATA17	I	Data Bus	
30	DATA18	I	Data Bus	
31	DATA19	I	Data Bus	
32	DATA20	I	Data Bus	

33	DATA21	I	Data Bus	
34	DATA22	I	Data Bus	
35	DATA23	I	Data Bus	
36	HSYNC	I	Horizontal Synchronous Signal	
37	VSYNC	I	Vertical Synchronous Signal	
38	DOTCLK	I	Data Clock	
39	NC	--	No Connection	
40	NC	--	No Connection	
41	VDD	P	Digital Power Supply	
42	VDD	P	Digital Power Supply	
43	NC	--	No Connection	
44	NC	--	No Connection	
45	NC	--	No Connection	
46	NC	--	No Connection	
47	NC	--	No Connection	
48	NC	--	No Connection	
49	NC	--	No Connection	
50	NC	--	No Connection	
51	NC	--	No Connection	
52	DEN	I	Data Enabling Signal	
53	GND	P	Ground	
54	GND	P	Ground	

I: input, O: output, P: Power

Note1: I/O definition:

I----Input O----Output P----Power/Ground

Note2: Interface controlled by SPI, please refer to the SPI command list.

Mode	D(23:16)	D(15:8)	D(7 : 0)	HSYNC	VSYNC	DEN
CCIR 656	DATA(23:16)	GND	GND	NC	NC	NC
CCIR 601	DATA(23:16)	GND	GND	HSYNC	VSYNC	NC
8 Bit RGB	DATA(23:16)	GND	GND	HSYNC	VSYNC	NC for HV Mode
						DEN for DEN Mode
24 Bit RGB	DATA(23:16)	DATA(15:8)	DATA(7:0)	HSYNC	VSYNC	NC for HV Mode
						DEN for DEN Mode

3. Operation Specifications

3.1. Absolute Maximum Ratings

Items	Symbol	Condition	Min.	Max.	Unit	Note
Power Voltage	VCC	GND=0	-0.3	4.6	Volt	
	VCI	AGND=0	-0.3	4.6	Volt	
	IOVCC	GND=0	-0.3	4.6	Volt	
Operation Temperature	Topa	-	-40	85	°C	Ambient temperature
Storage Temperature	Tstg	-	-55	125	°C	Ambient temperature

Note:

(1) All the voltages listed above are with respective to GND=0V.

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

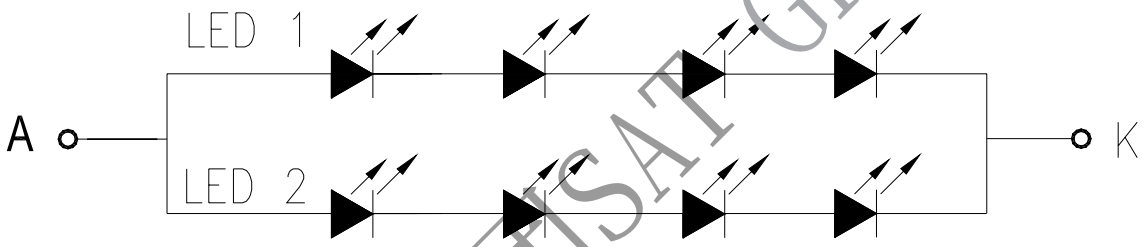
3.1.1 . Typical Operation Conditions

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Power voltage	Vcc	2.7	3.3	3.6	Volt	
	Vci	2.7	3.3	3.6	Volt	
	IOVcc	1.65	3.3	3.6	Volt	
Output signal high voltage	V_{OH}	0.8*IOVcc	-	IOVCC	Volt	
Output signal low voltage	V_{OL}	GND	-	0.2*IOVcc	Volt	
Input signal high voltage	V_{IH}	0.7*IOVc	-	IOVcc	Volt	
Input signal low voltage	V_{IL}	GND	-	0.3*IOVcc	Volt	
Input leakage current	I_{IN}	-1	-	1	uA	
Digital standby current	I_{ST}	-	10	50	uA	DCLK stop and inputs are default
Digital operating current	I_{CC}	-	TBD	TBD	mA	DCLK=25MHz, VCC=3.3V
Pull high/low resistor	R_P	150K	200K	300K	ohm	Digital input pads

3.1.2. Backlight Driving Conditions (8 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	11.6	13.2	14.0	V	Note 1
Current for LED backlight	IL	30	40	50	mA	
Luminance (on the module surface,BM-7)	L	350	400	-	cd/m^2	
LED life time	-	20,000	-	-	Hr	Note 2

Note 1 :There are 2 Groups LED

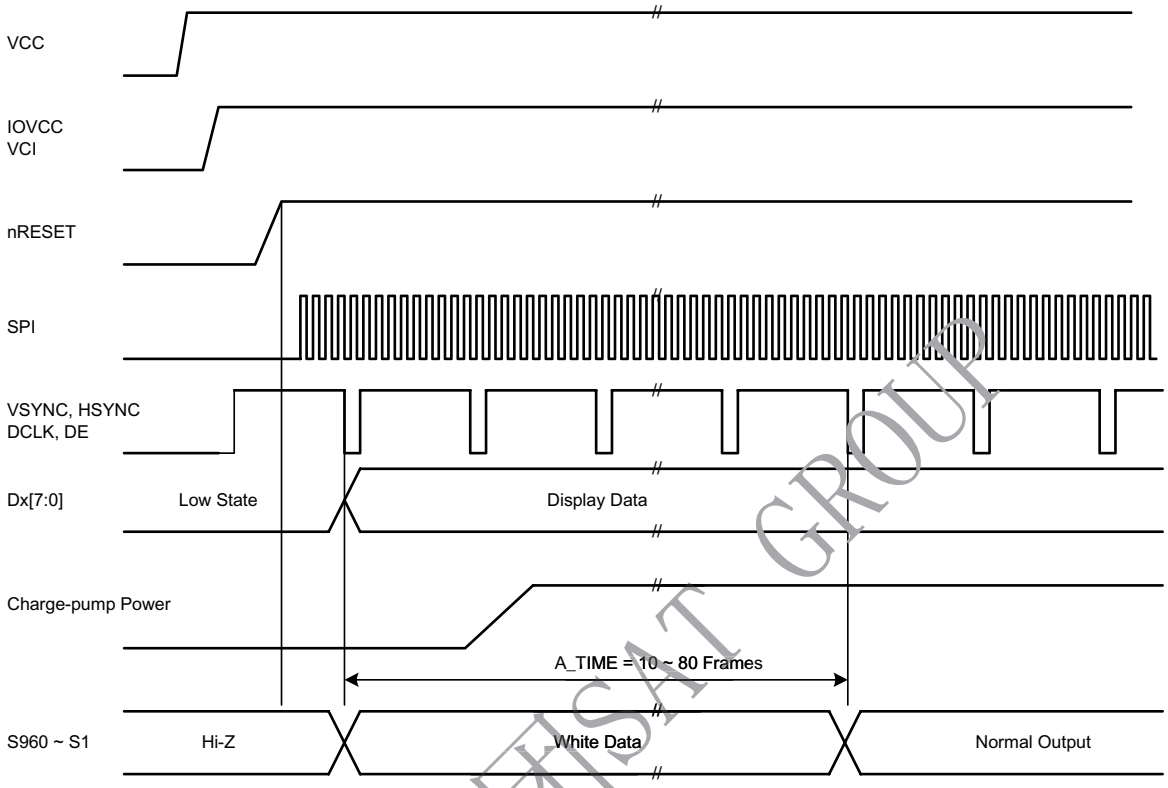


Note 2 : Ta = 25

Note 3 : Brightess to be decreased to 50% of the initial value

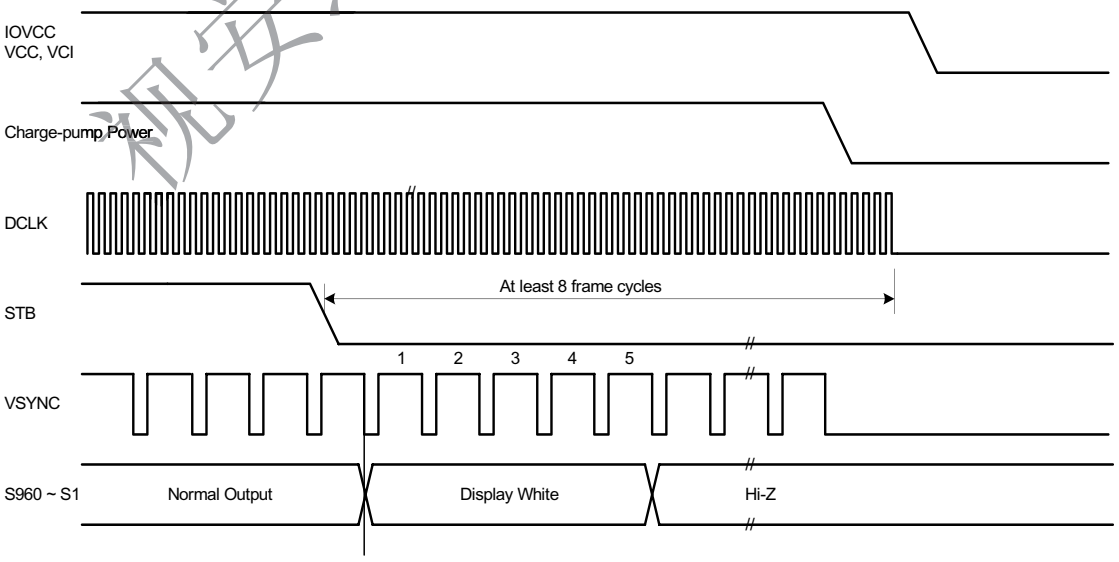
3.2. Power Sequence

3.2.1. Power-On Timing Sequence



Power On Sequence

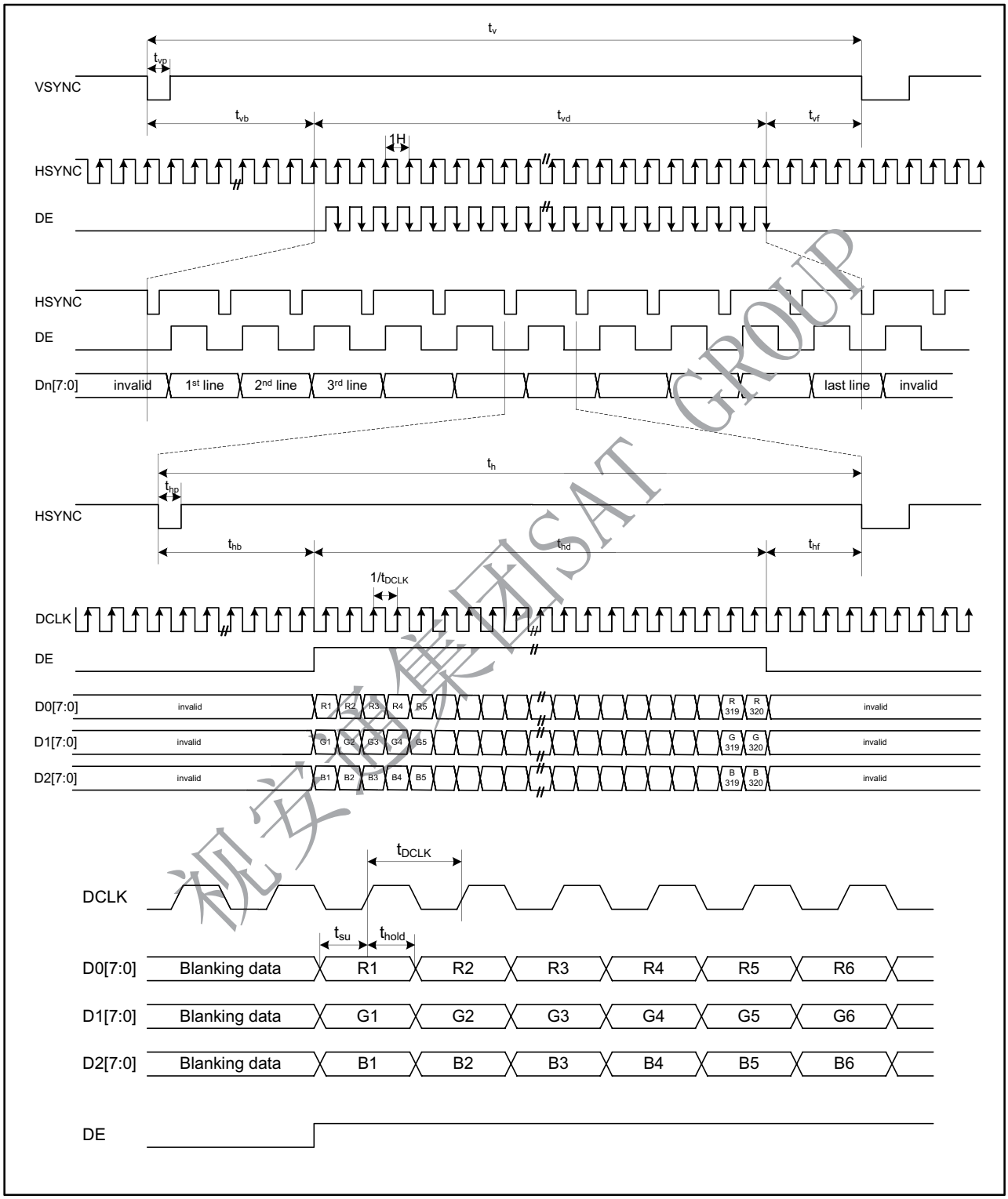
3.2.2 Power-Off Timing Sequence



Power Off Sequence Flow Chart

3.3. Timing Characteristics

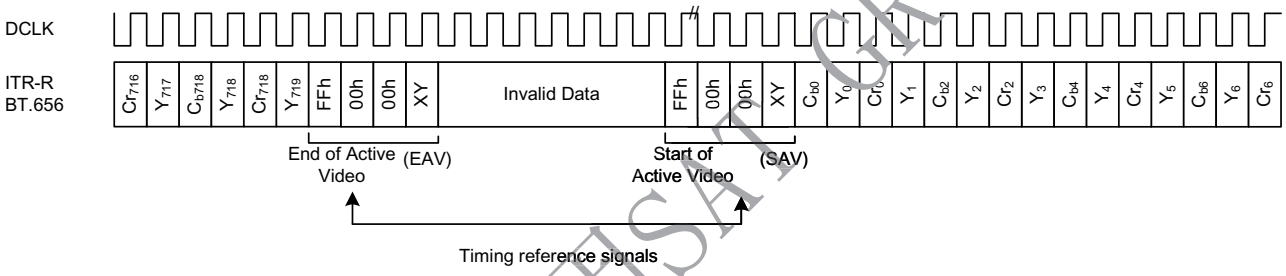
3.3.1 24-bit Parallel RGB Interface



Parallel RGB Input Signal Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
DCLK Frequency	$1/t_{DCLK}$	-	6.4	11	MHz	
Horizontal Period	t_h	-	408	-	t_{DCLK}	
Horizontal Display Period	t_{hd}	320	320	320	t_{DCLK}	
Horizontal Back Porch	t_{hb}	2	38	-	t_{DCLK}	
Horizontal Front Porch	t_{hf}	2	-	-	t_{DCLK}	
Horizontal Pulse Width	t_{hp}	1	1	-	t_{DCLK}	
Vertical Period	t_v	-	262	-	t_h	
Vertical Display Period	t_{vd}	240	240	240	t_h	
Vertical Back Porch	t_{vb}	2	18	-	t_h	
Vertical Front Porch	t_{vf}	2	4	-	t_h	
Vertical Pulse Width	t_{vp}	1	1	-	t_h	
Data setup time	t_{su}	12	-	-	ns	
Data hold time	t_{hold}	12	-	-	ns	

3.3.2. ITU-R BT.656 Interface



ITR-R BT.656 Input Signal

Note:

1. FFh, 00h, 00h, XY signals are involved with the HSYNC, VSYNC and Field signals

   F: field indication

   V: Vertical blanking indication

   H: Horizontal blanking indication

   P3 ~ P0: protection bits

   P3=V⊕H, P2=F⊕H, P1=F⊕V, P0=F⊕V⊕H

Data bit number	First Word (FFh)	Second Word (00h)	Third Word (00h)	Fourth Word (XY)
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0 (LSB)	1	0	0	P0

2. Horizontal blanking section consists of repeating pattern 80, 10, 80, 10.

BT.656 27 MHz (360 Mode) timing specifications:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
DCLK Frequency	$1/t_{DCLK}$	-	27	-	MHz	
Horizontal Period	t_h	-	1716	-	t_{DCLK}	
Horizontal Display Period	t_{hd}	1440	1440	1440	t_{DCLK}	
Horizontal Back Porch	t_{hb}	2	273	-	t_{DCLK}	
Horizontal Front Porch	t_{hf}	2	3	-	t_{DCLK}	
Horizontal Pulse Width	t_{hp}	1	1	-	t_{DCLK}	
Vertical Period	t_v	-	262.5 (312.5)	-	t_h	
Vertical Display Period	t_{vd}	-	240 (288)	-	t_h	
Vertical Back Porch	t_{vb}	2	18	-	t_h	
Vertical Front Porch	t_{vf}	2	4	-	t_h	
Vertical Pulse Width	t_{vp}	1	1	-	t_h	
Data setup time	t_{su}	12	-	-	ns	
Data hold time	t_{hold}	12	-	-	ns	

ITU-R BT.656 24.54 MHz (320 Mode) timing specifications:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
DCLK Frequency	$1/t_{DCLK}$	-	24.54	-	MHz	
Horizontal Period	t_h	-	1560	-	t_{DCLK}	
Horizontal Display Period	t_{hd}	1280	1280	1280	t_{DCLK}	
Horizontal Back Porch	t_{hb}	2	273	-	t_{DCLK}	
Horizontal Front Porch	t_{hf}	2	7	-	t_{DCLK}	
Horizontal Pulse Width	t_{hp}	1	1	-	t_{DCLK}	
Vertical Period	t_v	-	262.5 (312.5)	-	t_h	
Vertical Display Period	t_{vd}	-	240 (288)	-	t_h	
Vertical Back Porch	t_{vb}	2	18	-	t_h	
Vertical Front Porch	t_{vf}	2	4	-	t_h	
Vertical Pulse Width	t_{vp}	1	1	-	t_h	
Data setup time	t_{su}	12	-	-	ns	
Data hold time	t_{hold}	12	-	-	ns	

Note

1. Horizontal back porch time (H_BP) is adjustable by setting register HBP; requirement of min. back porch and min. front porch time must be satisfied.
2. Vertical back porch time (V_BP) is adjustable by setting register VBP; requirement of min. back porch and min. front porch time must be satisfied.
3. Interlace and non-interlace vertical input interfaces are acceptable.

3.3.3. Serial Peripheral Interface (SPI)

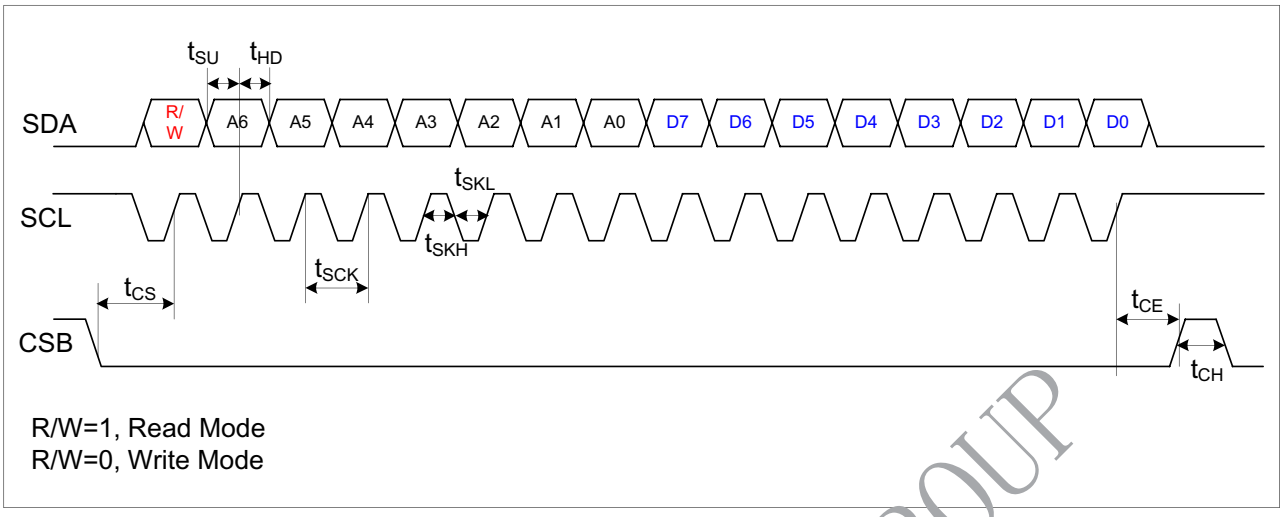


Figure8.3 SPI Interface Input Signal Timing

SPI Timing Specification

Items	Symbol	Min.	Typ.	Max.	Unit	Note
CSB to SCL Setup time	T_{CS}	50	-	-	ns	
CSB to SCL Hold time	T_{CE}	50	-	-	ns	
SCL Period	T_{SCK}	50	-	-	ns	
SCL High Period	T_{SKH}	25	-	-	ns	
SCL Low Period	T_{SKL}	25	-	-	ns	
Data Setup Time	T_{SU}	15	-	-	ns	
Data Hold Time	T_{HD}	15	-	-	ns	
CSB High Pulse Period	T_{CH}	50	-	-	ns	

3.3.4. Register

NO.	Description	D7	D6	D5	D4	D3	D2	D1	D0
R00	Chip ID	1	0	0	1	0	0	1	1
R01	VCOM Amplitude	-	-	-	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]
R02	VCOM High Voltage	-	-	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]
R03	VREG1OUT Voltage	-	-	-	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]
R04	Global Reset	-	-	-	-	-	-	-	GRESET
R05	Power Setting	-	VC[2]	VC[1]	VC[0]	-	BT[2]	BT[1]	BT[0]
R06	Entry Control	IN_SEL[3]	IN_SEL[2]	IN_SEL[1]	IN_SEL[0]	NTPAL[1]	NTPAL[0]	VDIR	HDIR
R07	Power Control	AUTO_EN	VCL_EN	VCOM_EN	-	DDVDH_EN	VGH_EN	VGL_EN	STB
R08	Vertical Back Porch	-	-	VBP[5]	VBP[4]	VBP[3]	VBP[2]	VBP[1]	VBP[0]
R09	Horizontal Back Porch	HBP[7]	HBP[6]	HBP[5]	HBP[4]	HBP[3]	HBP[2]	HBP[1]	HBP[0]
R0A	Polarity	-	REV	Formula	CbCr/BGR	DE_POL	VS_POL	HS_POL	DK_POL
R0B	Display	-	-	-	-	RGBIF[1]	RGBIF[0]	-	F/L
R0C	DC/DC	-	DC2[2]	DC2[1]	DC2[0]	-	DC1[2]	DC1[1]	DC1[0]
R0D	Driving	-	AP[1]	AP[0]	-	GAP[1]	GAP[0]	SAP[1]	SAP[0]
R0E	CONTRAST	-	-	-	-	CONTRAST[3:0]			
R0F	BRIGHT	BRIGHTNESS[7:0]							
R10	Gamma1	Neg_Gamma_1[3:0]				Pos_Gamma_1[3:0]			
R11	Gamma2	Neg _Gamma_2[3:0]				Pos_Gamma_2[3:0]			
R12	Gamma3	Neg _Gamma_3[3:0]				Pos_Gamma_3[3:0]			
R13	Gamma4	Neg _Gamma_4[3:0]				Pos_Gamma_4[3:0]			
R14	Gamma5	Neg _Gamma_5[3:0]				Pos_Gamma_5[3:0]			
R15	Gamma6	Neg _Gamma_6[3:0]				Pos_Gamma_6[3:0]			
R16	Gamma7	Neg _Gamma_7[3:0]				Pos_Gamma_7[3:0]			
R17	Gamma8	Neg _Gamma_8[3:0]				Pos_Gamma_8[3:0]			
R30	Power	-	POL_OUT	-	-	AUTO_DP	DISP_ON	A_TIME[1]	A_TIME[0]
R42	OTP Program	OTP_ PGM_EN	VCM_EN	VCM_ OTP5	VCM_ OTP4	VCM_ OTP3	VCM_ OTP2	VCM_ OTP1	VCM_ OTP0
R43	OTP Status	PGM_ CNT1	PGM_ CNT0	VCM_ D5	VCM_ D4	VCM_ D3	VCM_ D2	VCM_ D1	VCM_ D0
R44	OTP Key	OTP_ KEY7	OTP_ KEY6	OTP_ KEY5	OTP_ KEY4	OTP_ KEY3	OTP_ KEY2	OTP_ KEY1	OTP_ KEY0

Device ID (R00h)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	1	0	1	1	0

When reading this register, the Chip_ID will be read back (0x96).

VCOM AC Voltage (R01h)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]

VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.32 x VREG1OUT.

VDV[4:0]	VCOM Amplitude	VDV[4:0]	VCOM Amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0a	VREG1OUT x 0.90	5'h1a	VREG1OUT x 1.22
5'h0b	VREG1OUT x 0.92	5'h1b	VREG1OUT x 1.24
5'h0c	VREG1OUT x 0.94	5'h1c	VREG1OUT x 1.26
5'h0d	VREG1OUT x 0.96	5'h1d	VREG1OUT x 1.28
5'h0e	VREG1OUT x 0.98	5'h1e	VREG1OUT x 1.30
5'h0f	**VREG1OUT x 1.00 (Default)**	5'h1f	VREG1OUT x 1.32

VCOM High Voltage (R02h)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	0	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]

VCM[5:0] Set the VCOMH voltage from 0.37 to 1.00 x VREG1OUT.

VCM[5:0]	VCOMH	VCM[5:0]	VCOMH
6'h00	VREG1OUT x 0.37	6'h20	VREG1OUT x 0.69
6'h01	VREG1OUT x 0.38	6'h21	VREG1OUT x 0.70
6'h02	VREG1OUT x 0.39	6'h22	VREG1OUT x 0.71
6'h03	VREG1OUT x 0.40	6'h23	VREG1OUT x 0.72
6'h04	VREG1OUT x 0.41	6'h24	VREG1OUT x 0.73
6'h05	VREG1OUT x 0.42	6'h25	VREG1OUT x 0.74
6'h06	VREG1OUT x 0.43	6'h26	VREG1OUT x 0.75
6'h07	VREG1OUT x 0.44	6'h27	VREG1OUT x 0.76
6'h08	VREG1OUT x 0.45	6'h28	VREG1OUT x 0.77
6'h09	VREG1OUT x 0.46	6'h29	VREG1OUT x 0.78
6'h0a	VREG1OUT x 0.47	6'h2a	VREG1OUT x 0.79

6'h0b	VREG1OUT x 0.48	6'h2b	VREG1OUT x 0.80
6'h0c	VREG1OUT x 0.49	6'h2c	VREG1OUT x 0.81
6'h0d	VREG1OUT x 0.50	6'h2d	VREG1OUT x 0.82
6'h0e	VREG1OUT x 0.51	6'h2e	**VREG1OUT x 0.83 (Default)**
6'h0f	VREG1OUT x 0.52	6'h2f	VREG1OUT x 0.84
6'h10	VREG1OUT x 0.53	6'h30	VREG1OUT x 0.85
6'h11	VREG1OUT x 0.54	6'h31	VREG1OUT x 0.86
6'h12	VREG1OUT x 0.55	6'h32	VREG1OUT x 0.87
6'h13	VREG1OUT x 0.56	6'h33	VREG1OUT x 0.88
6'h14	VREG1OUT x 0.57	6'h34	VREG1OUT x 0.89
6'h15	VREG1OUT x 0.58	6'h35	VREG1OUT x 0.90
6'h16	VREG1OUT x 0.59	6'h36	VREG1OUT x 0.91
6'h17	VREG1OUT x 0.60	6'h37	VREG1OUT x 0.92
6'h18	VREG1OUT x 0.61	6'h38	VREG1OUT x 0.93
6'h19	VREG1OUT x 0.62	6'h39	VREG1OUT x 0.94
6'h1a	VREG1OUT x 0.63	6'h3a	VREG1OUT x 0.95
6'h1b	VREG1OUT x 0.64	6'h3b	VREG1OUT x 0.96
6'h1c	VREG1OUT x 0.65	6'h3c	VREG1OUT x 0.97
6'h1d	VREG1OUT x 0.66	6'h3d	VREG1OUT x 0.98
6'h1e	VREG1OUT x 0.67	6'h3e	VREG1OUT x 0.99
6'h1f	VREG1OUT x 0.68	6'h3f	VREG1OUT x 1.00

Polarity Control (R0Ah)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	REV	Formula	CbCr/BGR	DE_POL	VS_POL	HS_POL	DK_POL

DCLK_POL	Function
0	Negative Polarity
1	Positive Polarity **(default)**

VSYNC_POL	Function
0	Negative Polarity **(default)**
1	Positive Polarity

HSYNC_POL	Function
0	Negative Polarity **(default)**
1	Positive Polarity

DE_POL	Function
0	Negative Polarity
1	Positive Polarity **(default)**

CbCr/BGR	Function
0	YCbCr Mode: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3 **(default)**

Interface Control (R0Bh)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	0	0	0	RGBIF[1]	RGBIF[0]	0	F/L

F/L	Function
0	Frame inversion.
1	Line Inversion. **(default)**

RGBIF[1:0]	Function
00	HSYNC+VSYNC Mode
01	HSYNC+VSYNC+DE Mode **(default)**
10	DE Only Mode
11	Setting disabled

Power Control 1 (R0Ch)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	DC2[2]	DC2[1]	DC2[0]	0	DC1[2]	DC1[1]	DC1[0]

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2]	DC1[1]	DC1[0]	Frequency
0	0	0	DCLK/8
0	0	1	DCLK/16
0	1	0	DCLK/32
0	1	1	DCLK/64
1	0	0	DCLK/128 **(Default)**
1	0	1	DCLK/256
1	1	0	DCLK/512
1	1	1	Disable

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC2[2]	DC2[1]	DC2[0]	Frequency
0	0	0	DCLK/32
0	0	1	DCLK/64
0	1	0	DCLK/128
0	1	1	DCLK/256
1	0	0	DCLK/512 **(Default)**
1	0	1	DCLK/1024
1	1	0	DCLK/2048
1	1	1	Disable

Note: Be sure fDCDC1≥fDCDC2 when setting DC0[2:0] and DC1[2:0].

Power Control 2(R0Dh)

R/W	D7	D6	D5	D4	D3	D2	D1	D0
W	0	AP[1]	AP[0]	0	GAP[1]	GAP[1]	SAP[1]	SAP[0]

AP[1]	AP[0]	Driving Current
0	0	X1.0 **(Default)**
0	1	X0.75
1	0	X1.25
1	1	X 1.5

GAP[1]	GAP[0]	Driving Current
0	0	X0.8
0	1	X0.9
1	0	X1.0 (**Default)**
1	1	X 1.1

SAP[1]	SAP[0]	Driving Current
0	0	X0.8
0	1	X0.9
1	0	X1.0 (**Default)**
1	1	X 1.1

4. Optical Specifications

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing angle (CR≥ 10)		θ_L	Φ=180°(9 o'clock)	65	75	-	degree	Note 1
		θ_R	Φ=0°(3 o'clock)	65	75	-		
		θ_T	Φ=90°(12 o'clock)	50	60	-		
		θ_B	Φ=270°(6 o'clock)	60	70	-		
Response time		T_{ON}	Normal θ=Φ=0°	-	3	6	msec	Note 3
		T_{OFF}		-	7	14	msec	Note 3
Contrast ratio		CR		480	600	-	-	Note 4
Color Chromaticity	White	W_X		0.280	0.310	0.340	-	Note 2 Note 5 Note 6
		W_Y		0.319	0.349	0.379	-	
	Red	R_X		0.596	0.626	0.656	-	
		R_Y		0.316	0.346	0.376	-	
	Green	G_X		0.292	0.322	0.352	-	
		G_Y		0.522	0.552	0.582	-	
	Blue	B_X		0.119	0.149	0.179	-	
		B_Y		0.153	0.183	0.213	-	
Luminance		L		350	400	--	cd/m^2	Note 6
Luminance uniformity		Y_U		75	80	--	%	Note 7

Test Conditions:

1. DV_{DD}=3.3V, I_L =40mA(Backlight current),the amblent temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

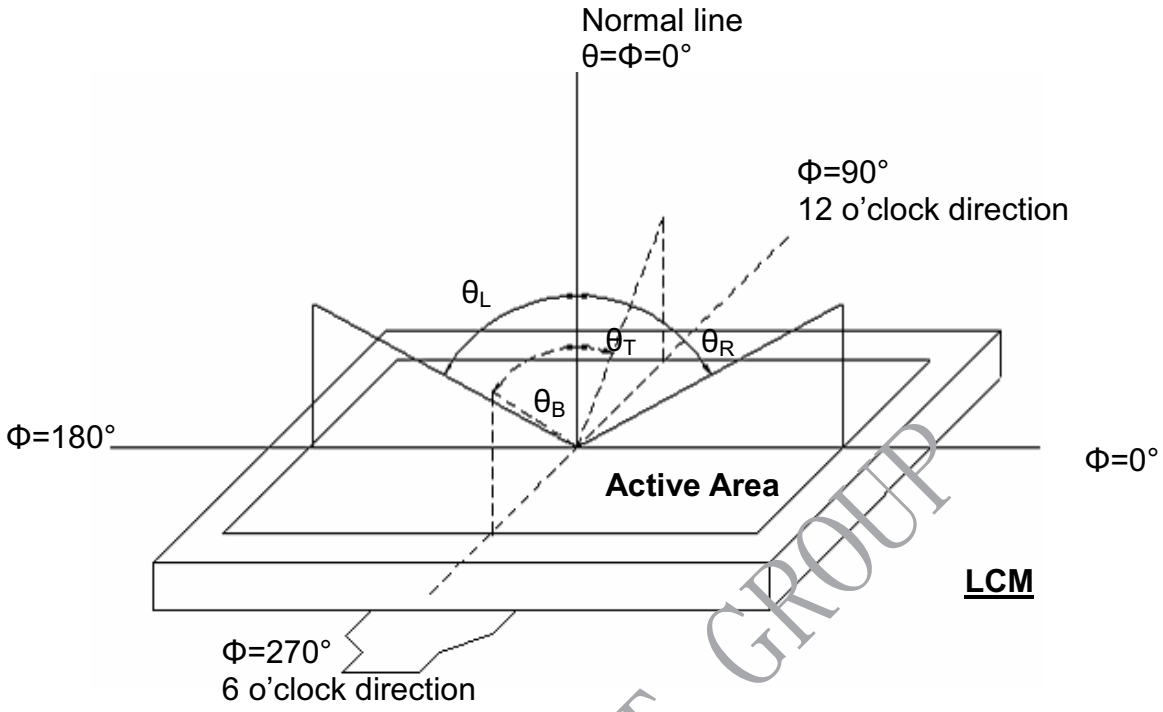


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

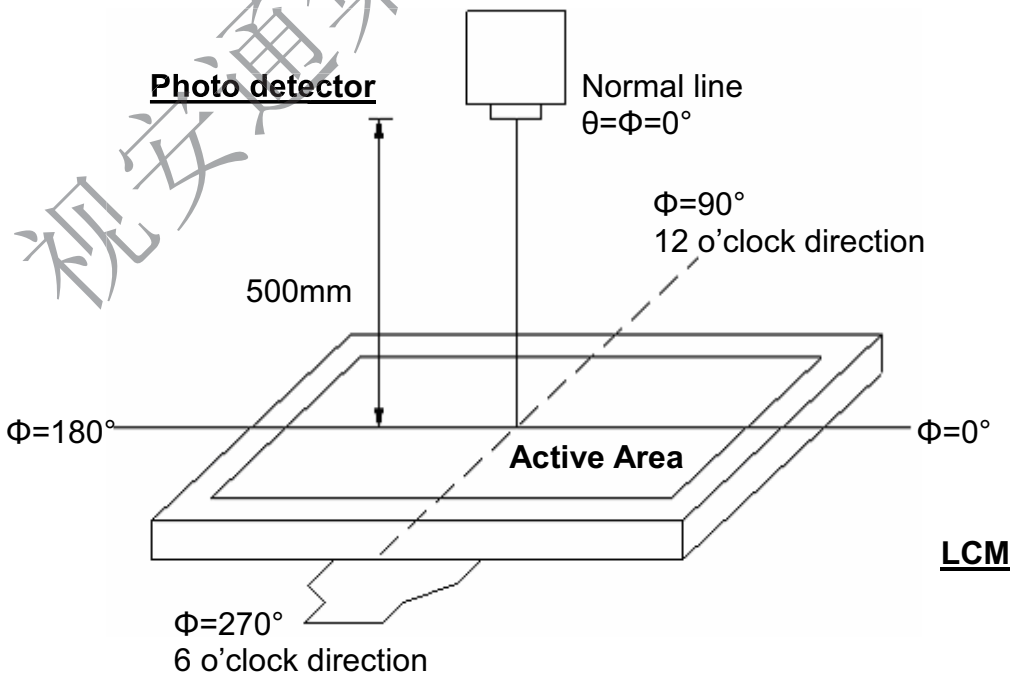


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

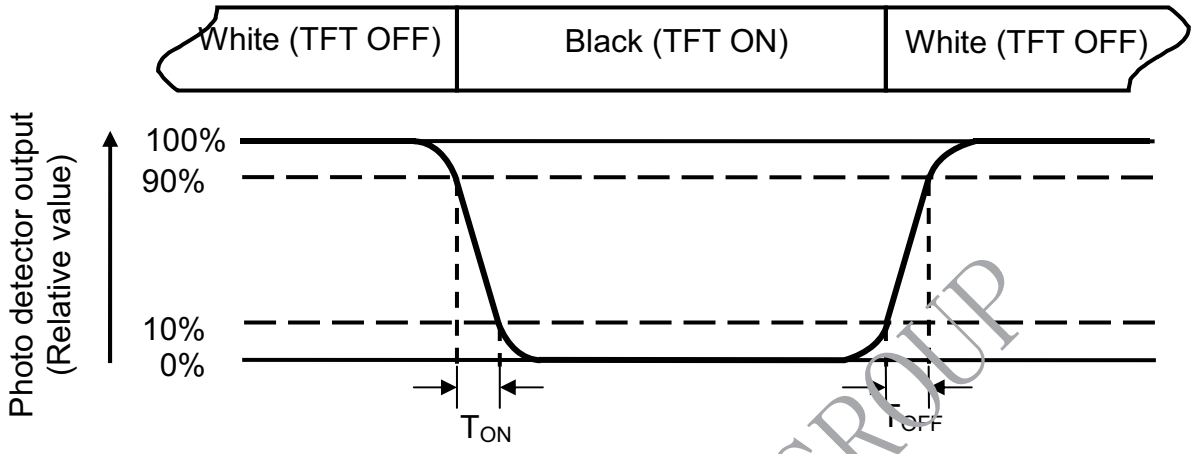


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

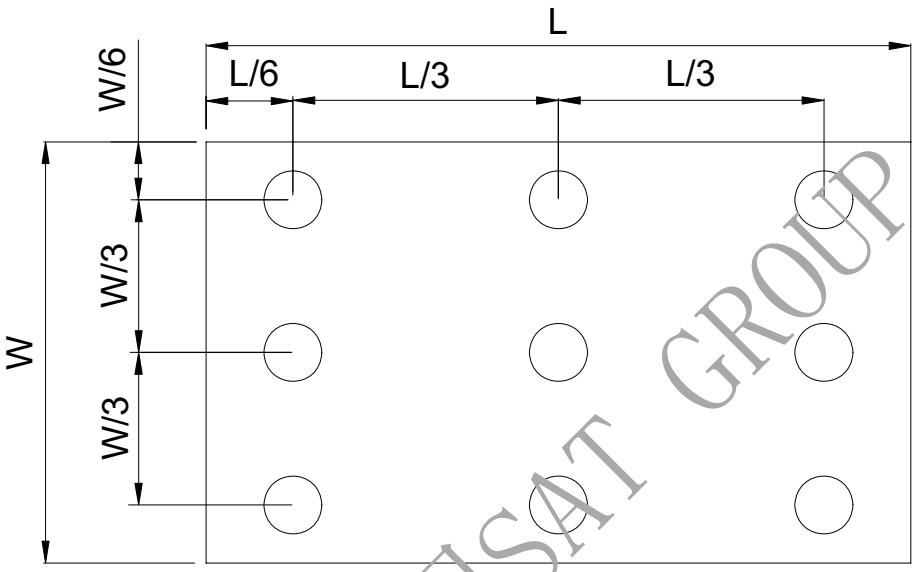


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

5. Reliability Test Items

(Note3)

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80℃ 240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -30℃ 240hrs	Note 1，Note 4
High Temperature Operation	Ts = 70℃ 240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -20℃ 240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH 240hrs	Note 4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

6. General Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

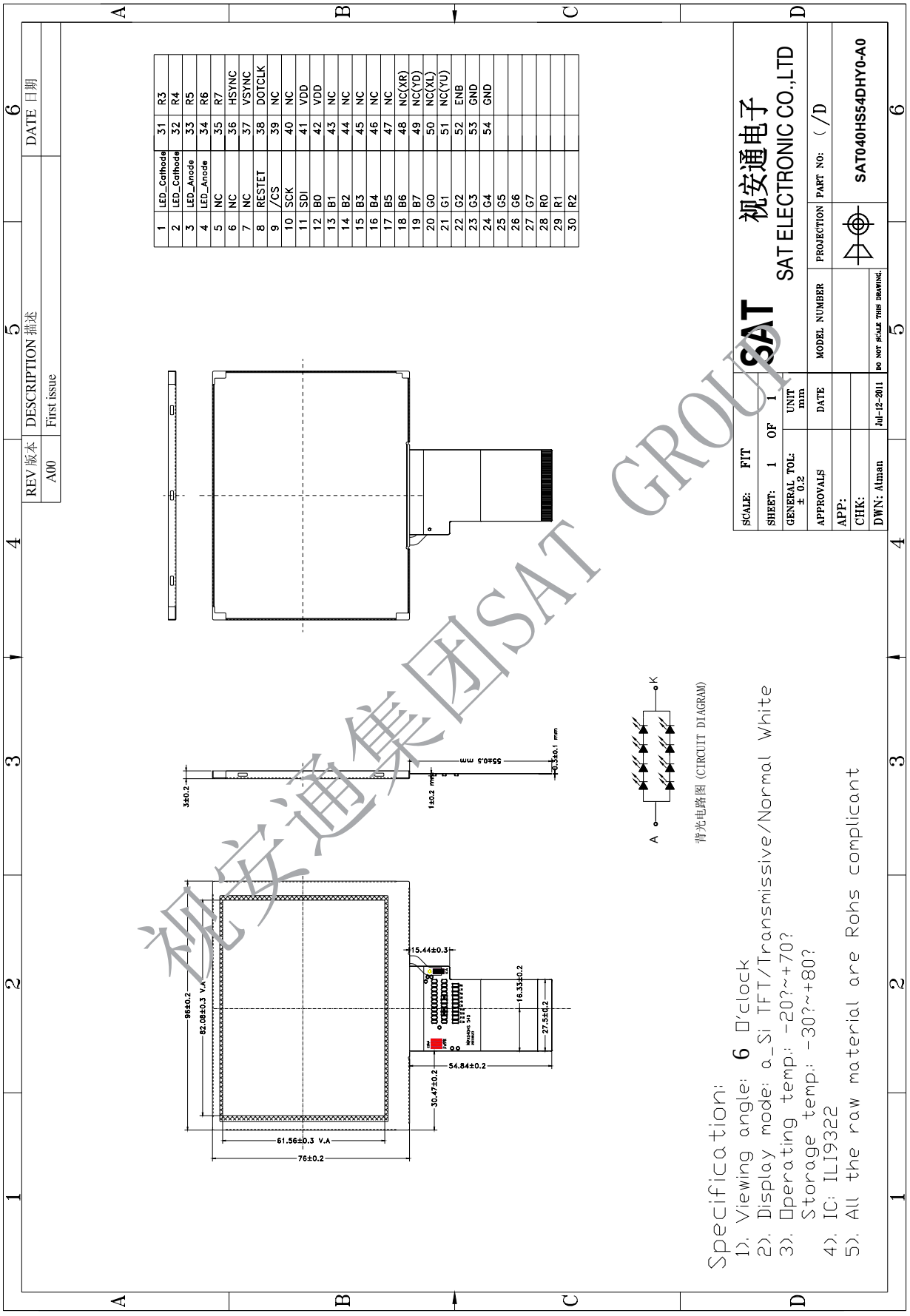
6.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

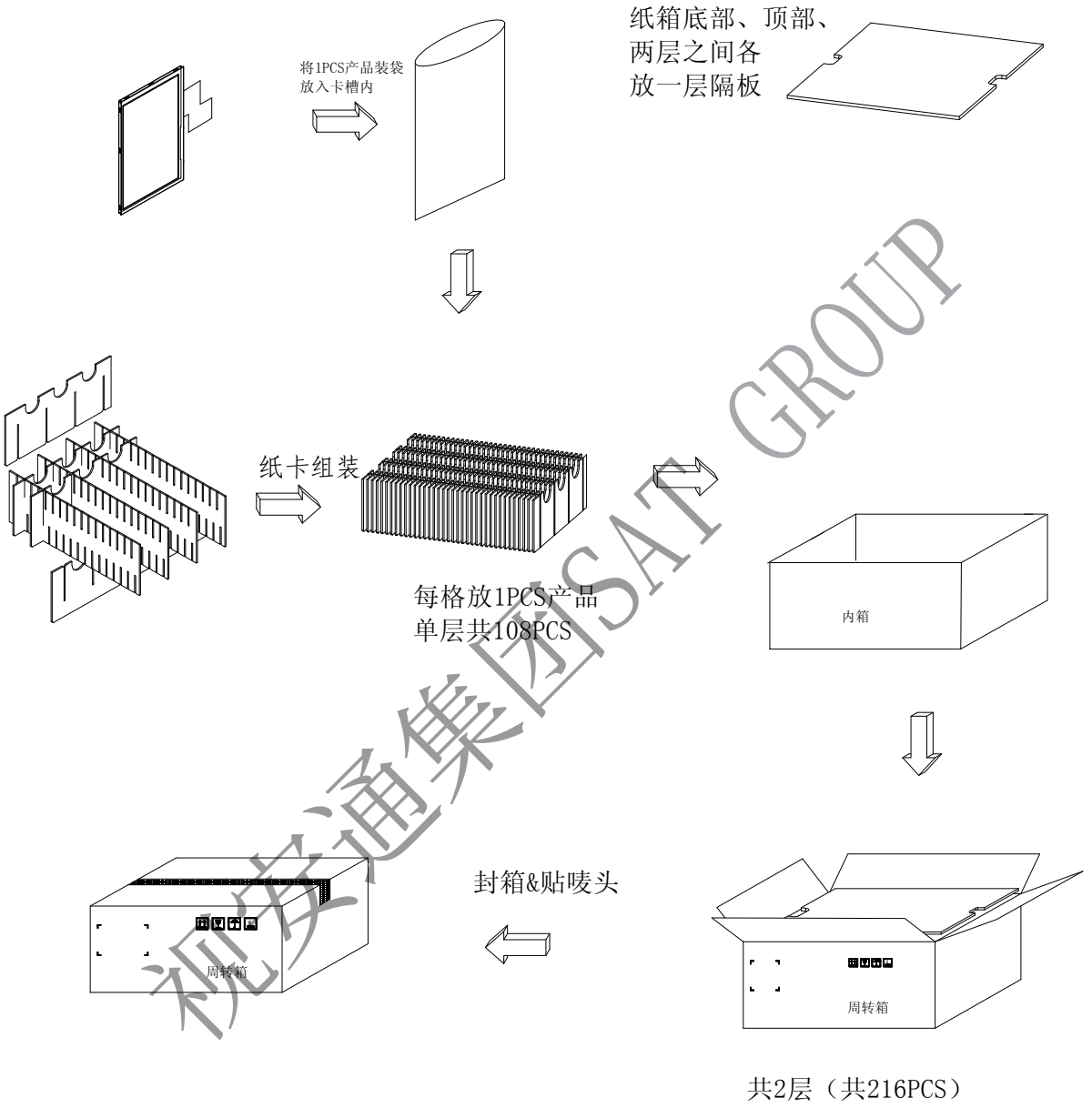
6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing



8. Package Drawing



9 . Product ID Rule

Product Name

No	Definition	Specifications
(1)	TFT LCM Productor No.	**SAT**---- **SAT ELECTRONIC CO.LTD**
(2)	Display monitor opposite angle line size	Unit :inch or mmm (size <10 inch: takes two integers ; size >=10 inch: takes three integers)
(3)	LCD Type	AU----AUO ; CP----CPT ; PV----PVI ; TM----TIANMA ; HS----HSD ; LG----LG ; Wi----Wintek ; CM----CMO ; HY----Hydis ; HI----Hitach; Sh----Sharp ; BO---BOE 。。。
(4)	Interface PIN Number	By two figures characters expression from 01 to 99
(5)	Type	A---- Alternated Video Signal; D---- Data Video Signal;
(6)	LED Back Light Type	H----high light ; M---- Commonly light; L---- low light
(7)	LED Back Light colored warp	Rx----red ; Gx----green ; Bx---- blueness; Yx----white; P----PVI; x---- warp distinction,1 minimal,9 maximal
(8)	BK Productor number	By The English litters : A 0~ Z9 A0---MeX

No	Definition	Specifications
(9)	FPC Type	S---short L---Long
(10)	IC Type	By two figures characters expression from 01 to 99