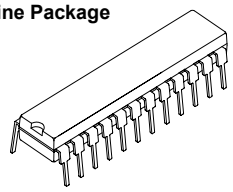
16-bit Constant Current LED Sink Driver with Gain Control

Features

- 16 constant-current output channels
- Output current adjustable through an external resistor
- Programmable output current gain for White Balance
- Constant output current range: 5-90 mA
- Excellent output current accuracy:
  between channels: ±3% (max.), and
  between ICs: ±6% (max.)
- Constant output current invariant to load voltage change
- Fast response of output current, $\overline{OE}$ (min.): 200 ns
- 25MHz clock frequency
- Schmitt trigger input
- 5V supply voltage
- Optional for “Pb-free & Green” Package

Current Accuracy		Conditions
Between Channels	Between ICs	
< ±3%	< ±6%	I_{OUT} = 10 ~ 60 mA

Dual In-Line Package



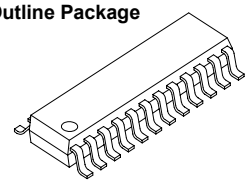
CN: P-DIP24-300-2.54

GN: P-DIP24-300-2.54

CNS: SP-DIP24-300-1.78

GNS: SP-DIP24-300-1.78

Small Outline Package



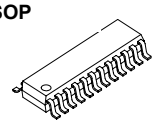
CD: SOP24-300-1.27

GD: SOP24-300-1.27

CF: SOP24-300-1.00

GF: SOP24-300-1.00

Shrink SOP



CP\CPA: SSOP24-150-0.64

GP\GPA: SSOP24-150-0.64

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Product Description

MBI5028 succeeds MBI5026 and is designed for LED displays with Gain Control extension. MBI5028 exploits PrecisionDrive™ technology to enhance its output characteristics. MBI5028 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At MBI5028 output stage, sixteen regulated current ports are designed to provide constant current sinks for driving LEDs within a wide range of Vf variations.

MBI5028 provides users with great flexibility and device performance while using MBI5028 in their LED panel system design. Users may adjust the output current from 5 mA to 90 mA through an external resistor R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. MBI5028 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

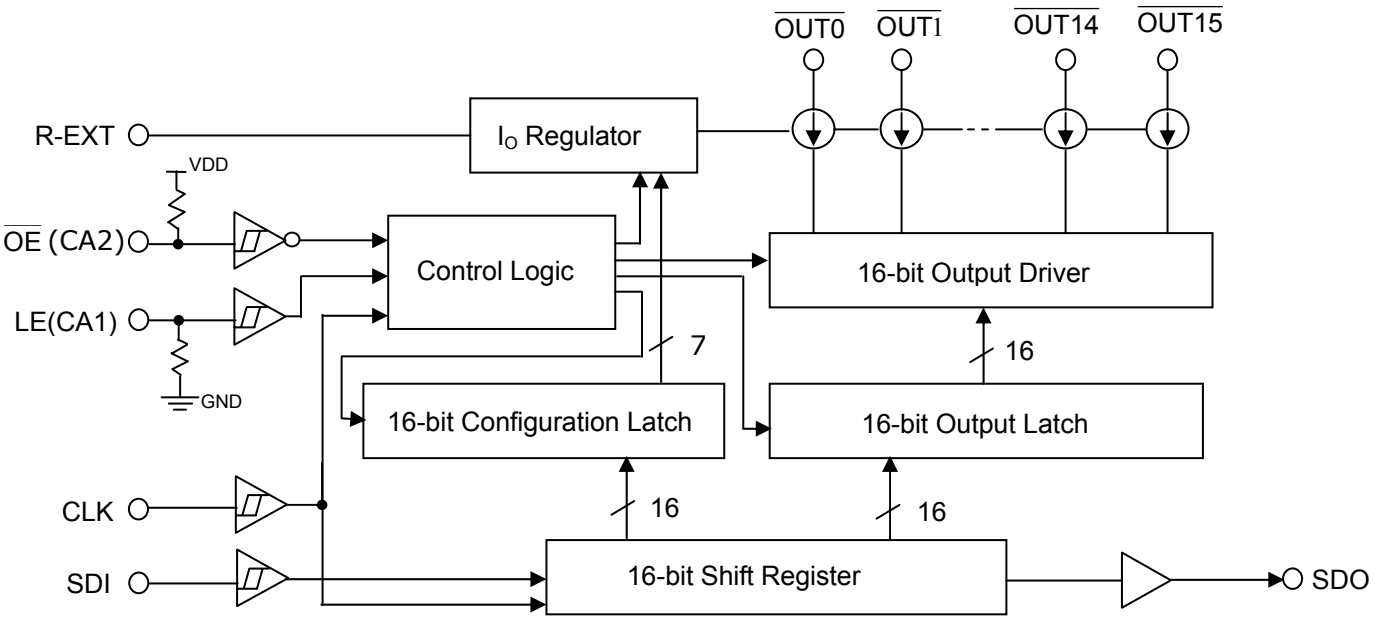
MBI5028 also exploits Share-I-O™ technology and is backward compatible with MBI5026 in both electrical characteristics and package aspect. To utilize the Current Adjust feature, users may not have to change the printed circuit board originally for MBI5026. To enter a special function mode--Current Adjust mode, users just need to set a specific sequence of signals on LE(CA1), $\overline{OE}$ (CA2) and CLK input pins. Normally, the output current can be regulated only through an external resistor. In addition, in the Current Adjust mode, the output current can be software-programmable by a system controller. The system controller adjusts the output current by sending a 7-bit Current Adjust code to 16-bit Configuration Latch through MBI5028 SDI pin. The code will be latched and effective to control the output current regulator. A fine adjustment of the output current could be achieved by a gain ranging from 1/9 to 0.9896 with 128 fine steps. By setting another sequence of signals on LE(CA1), $\overline{OE}$ (CA2) and CLK input pins, MBI5028 may resume to a Normal mode and perform as MBI5026. The Shift Register, with SDI, SDO, and CLK, carries the image data as usual.

By means of the Share-I-O™ technique, an additionally effective function, Current Gain, can be added to LED drivers, MBI5028, without any extra pins. Thus, MBI5028 could be a drop-in replacement of MBI5026. The printed circuit board originally designed for MBI5026 may be also applicable for MBI5028.

For MBI5028, Pin LE and $\overline{OE}$ can respectively offer two functions:

Device Type	Pin Name	Function description
CN\CNS\CD\CF\CP GN\GNS\GD\GF\GP	Pin4	LE+Current Adjust
CPA GPA	Pin10	LE+Current Adjust
CN\CNS\CD\CF\CP GN\GNS\GD\GF\GP	Pin21	$\overline{OE}$ +Current Adjust
CPA GPA	Pin3	$\overline{OE}$ +Current Adjust

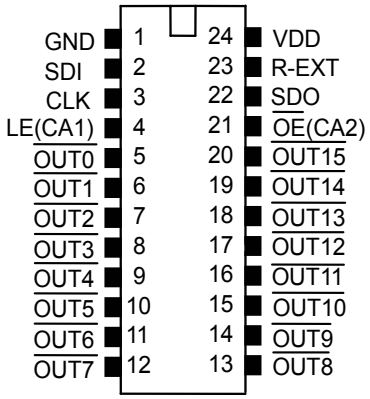
Block Diagram



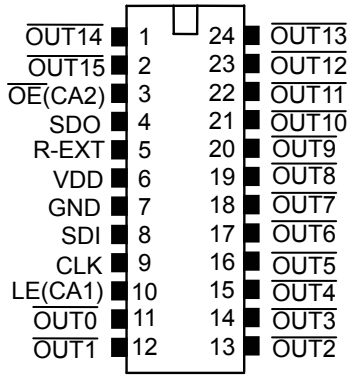
Terminal Description

Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the Shift Register
CLK	Clock input terminal for data shift on rising edge
LE(CA1)	Data strobe input terminal Serial data is transferred to the respective latch when LE(CA1) is high. The data is latched when LE(CA1) goes low. Also, a control signal input for Current Adjust mode (See **Timing Diagram**)
OUT0 ~ OUT15	Constant current output terminals
OE (CA2)	Output enable terminal When OE (CA2)(active) low, the output drivers are enabled; when OE (CA2) high, all output drivers are turned OFF (blanked). Also, a second control signal input for Current Adjust mode (See **Timing Diagram**)
SDO	Serial-data output to the following SDI of next driver IC
R-EXT	Input terminal used to connect an external resister for setting up all output current
VDD	5V supply voltage terminal

Pin Configuration



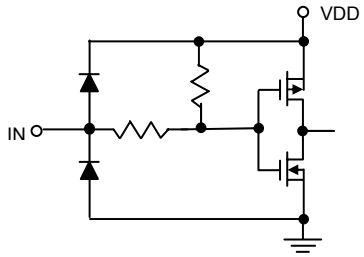
MBI5028 CN\CNS\CD\CF\CP\ GN\GNS\GD\GF\GP



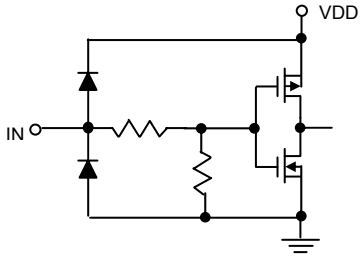
MBI5028 CPA\GPA

Equivalent Circuits of Inputs and Outputs

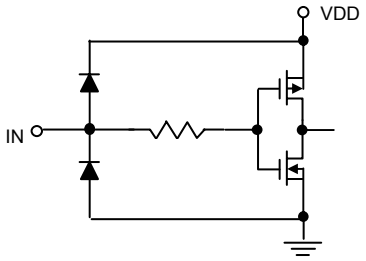
$\overline{OE}$ (CA2) terminal



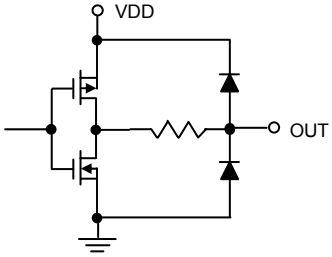
LE(CA1) terminal



CLK, SDI terminal

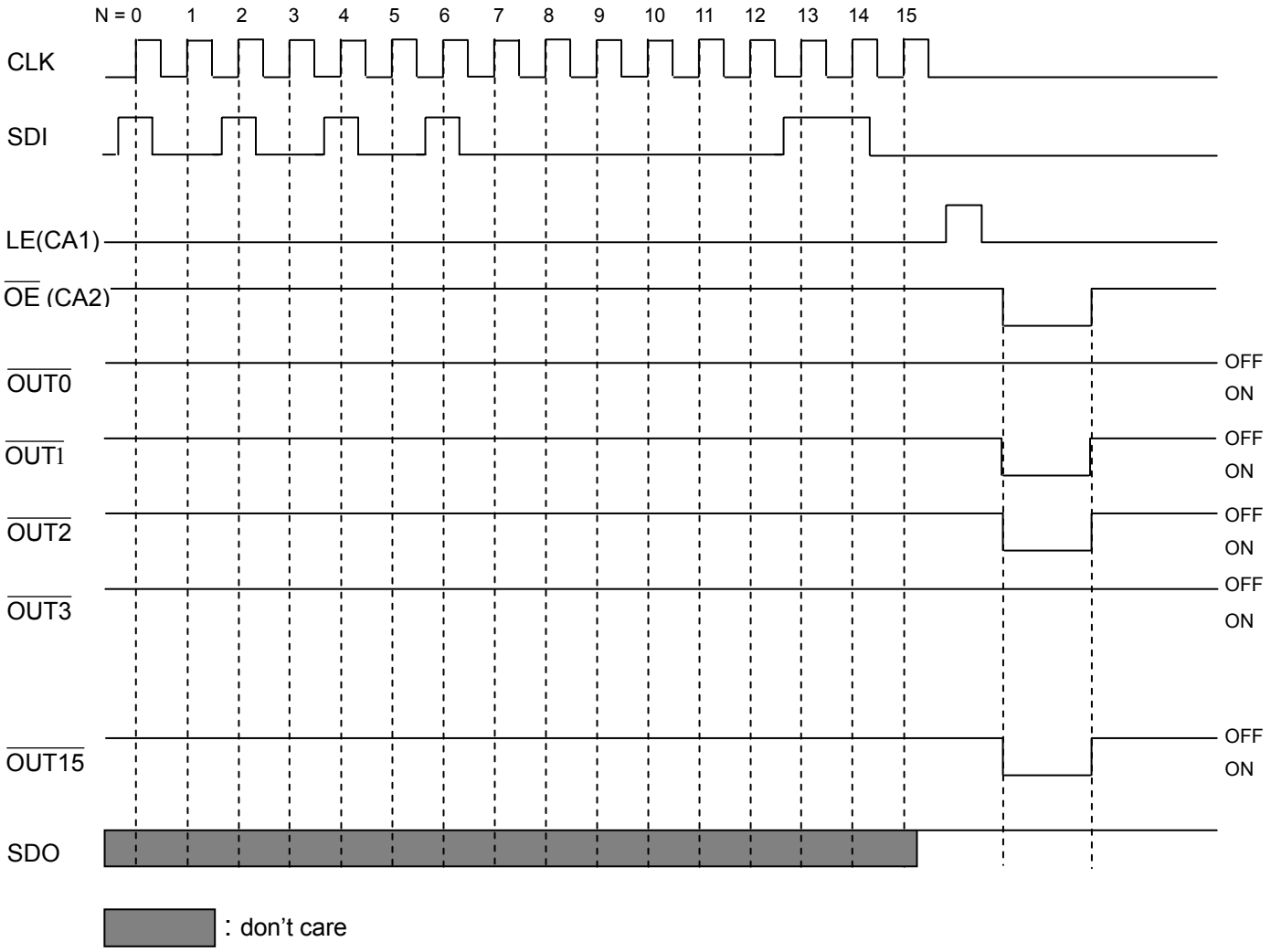


SDO terminal



Timing Diagram

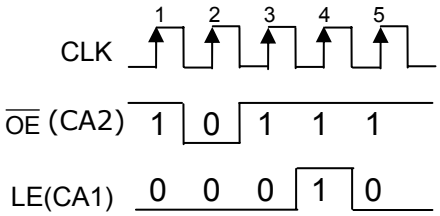
Normal Mode



Truth Table (In Normal Mode)

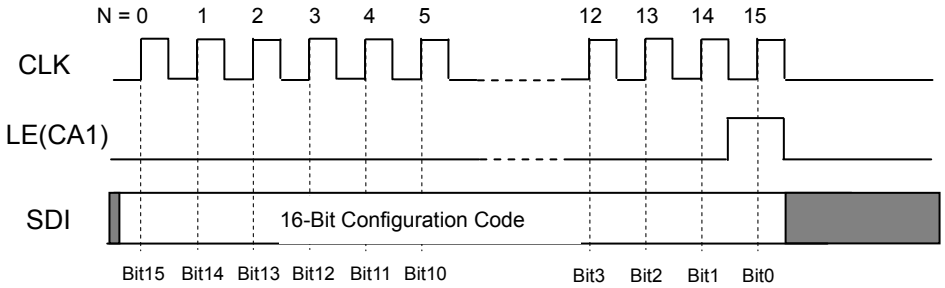
CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ….. $\overline{D_{n-7}}$ …. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Switching to Current Adjust Mode



The signal sequence makes MBI5028 enter a **Current Adjust** mode. Here, the LE active pulse would not latch any data.

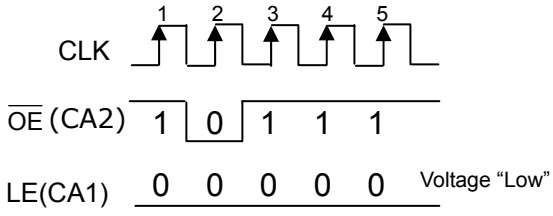
Writing Configuration Code



Note:

In the Current Adjust mode, by sending the positive pulse of LE(CA1), the content of the Shift Register, a Current Adjust code, will be written to the 16-Bit Configuration Latch.

Switching to Normal Mode



The signal sequence makes MBI5028 resume to a Normal mode.

Note:

Pin $\overline{OE}$ (CA2) could always enable the output port no matter MBI5028 enters a Current Adjust mode or not. If users want to know the whole process, that is how to enter a Current Adjust mode, write Current Adjust codes and resume to a Normal mode, please refer to the contents in **Application Information**.

Maximum Ratings

Characteristic			Symbol	Rating		Unit
Supply Voltage			V_{DD}	0 ~ 7.0		V
Input Voltage			V_{IN}	-0.4 ~ V_{DD}+0.4		V
Output Current			I_{OUT}	+90		mA
Output Voltage			V_{DS}	-0.5 ~ +17.0		V
Clock Frequency			F_{CLK}	25		MHz
GND Terminal Current			I_{GND}	1440		mA
Power Dissipation (On PCB, Ta=25°C)	CN	GN	P_D	1.80	2.00	W
	CNS	GNS		1.50	1.61	
	CD	GD		2.01	2.19	
	CF	GF		1.69	1.91	
	CP	GP		1.38	1.46	
	CPA	GPA		1.38	1.46	
Thermal Resistance (On PCB, Ta=25°C)	CN	GN	$R_{th(j-a)}$	53.82	49.91	°C/W
	CNS	GNS		66.74	62.28	
	CD	GD		49.81	45.69	
	CF	GF		59.01	52.38	
	CP	GP		72.43	68.48	
	CPA	GPA		72.43	68.48	
Operating Temperature			T_{opr}	-40~+85		°C
Storage Temperature			T_{stg}	-55~+150		°C

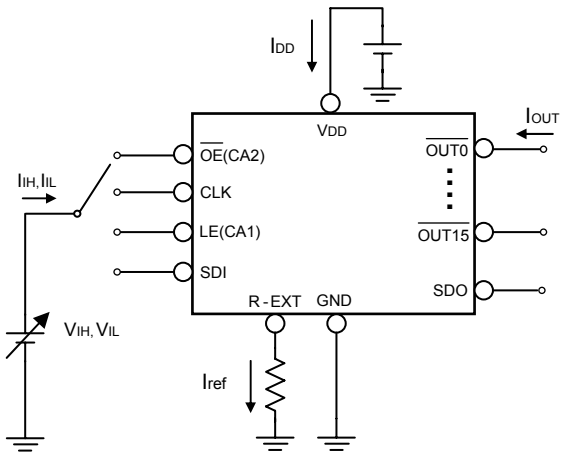
Recommended Operating Conditions

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
Output Voltage	V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	17.0	V
Output Current	I_{OUT}	DC Test Circuit	5	-	90	mA
	I_{OH}	SDO	-	-	-1.0	mA
	I_{OL}	SDO	-	-	1.0	mA
Input Voltage	V_{IH}	CLK, $\overline{OE}$ (CA2), LE(CA1) and SDI	0.8*V_{DD}	-	V_{DD}	V
	V_{IL}	CLK, $\overline{OE}$ (CA2), LE(CA1) and SDI	GND	-	0.3*V_{DD}	V
LE(CA1) Pulse Width	$t_{w(L)}$	Normal Mode V_{DD}=4.5~5.5V	20	-	-	ns
$\overline{OE}$ (CA2) Pulse Width	$t_{w(OE)}$		200	-	-	ns
CLK Pulse Width	$t_{w(CLK)}$		20	-	-	ns
Setup Time for SDI	$t_{su(D)}$		5	-	-	ns
Hold Time for SDI	$t_{h(D)}$		10	-	-	ns
Setup Time for LE(CA1)	$t_{su(L)}$		15	-	-	ns
Hold Time for LE(CA1)	$t_{h(L)}$		15	-	-	ns
CLK Pulse Width	$t_{w(CLK)}$	Current Adjust Mode V_{DD}=4.5~5.5V	20	-	-	ns
Setup Time for LE(CA1)	$t_{su(CA1)}$		5	-	-	ns
Hold Time for LE(CA1)	$t_{h(CA1)}$		10	-	-	ns
Setup Time for $\overline{OE}$ (CA2)	$t_{su(CA2)}$		5	-	-	ns
Hold Time for $\overline{OE}$ (CA2)	$t_{h(CA2)}$		10	-	-	ns
Clock Frequency	F_{CLK}	Cascade Operation	-	-	25.0	MHz

Electrical Characteristics

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	DC Test Circuit		5	-	90	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC		0.8*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC		GND	-	0.3*V_{DD}	V
Output Leakage Current		I_{OH}	V_{OH}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS}=0.6V	R_{ext}=809 Ω	-	26.0	-	mA
Current Skew		dI_{OUT1}	I_{OL}=26mA V_{DS}=0.6V	R_{ext}=809 Ω	-	±1	±3	%
Output Current 2		I_{OUT2}	V_{DS}=0.8V	R_{ext}=404 Ω	-	52.1	-	mA
Current Skew		dI_{OUT2}	I_{OL}=52.1mA V_{DS}=0.8V	R_{ext}=404 Ω	-	±1	±3	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1	-	% / V
Pull-up Resister		R_{IN}(up)	$\overline{OE}$ (CA2)		250	500	800	KΩ
Pull-down Resister		R_{IN}(down)	LE(CA1)		250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6	6.8	mA
		I_{DD}(off) 2	R_{ext}=809 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	8.8	9.6	
		I_{DD}(off) 3	R_{ext}=404 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	12.4	13.2	
	"ON"	I_{DD}(on) 1	R_{ext}=809 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	8.8	10.8	
		I_{DD}(on) 2	R_{ext}=404 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	12.3	15.3	

Test Circuit for Electrical Characteristics

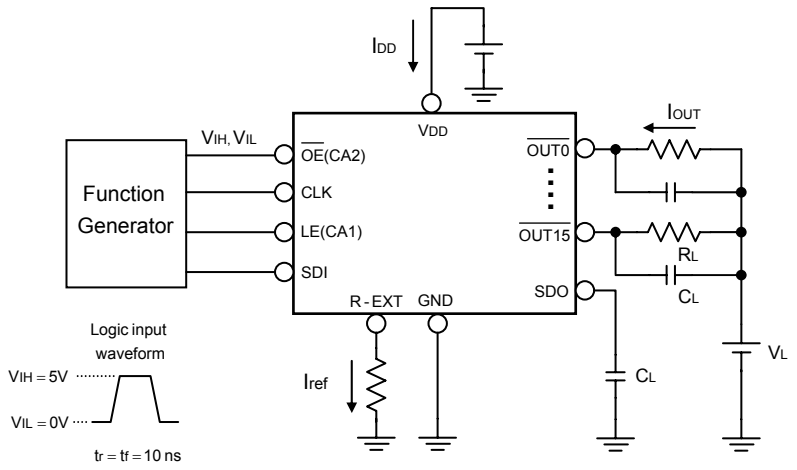


Switching Characteristics

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{OUTn}$	t_{pLH1}	V_{DD}=5.0 V V_{DS}=0.8 V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=300 Ω V_L=4.0 V R_L=52 Ω C_L=10 pF	-	100	150	ns
	LE(CA1) - $\overline{OUTn}$	t_{pLH2}		-	100	150	ns
	$\overline{OE}$ (CA2)- $\overline{OUTn}$	t_{pLH3}		-	50	150	ns
	CLK - SDO	t_{pLH}		15	20	-	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{OUTn}$	t_{pHL1}		-	50	100	ns
	LE(CA1) - $\overline{OUTn}$	t_{pHL2}		-	50	100	ns
	$\overline{OE}$ (CA2)- $\overline{OUTn}$	t_{pHL3}		-	20	100	ns
	CLK - SDO	t_{pHL}		15	20	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE(CA1)	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ (CA2)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE(CA1)		$t_{h(L)}$		5	-	-	ns
Setup Time for LE(CA1)		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r**		-	-	500	ns
Maximum CLK Fall Time		t_f**		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	70	200	ns
Output Fall Time of Vout (turn on)		t_{of}		-	40	120	ns

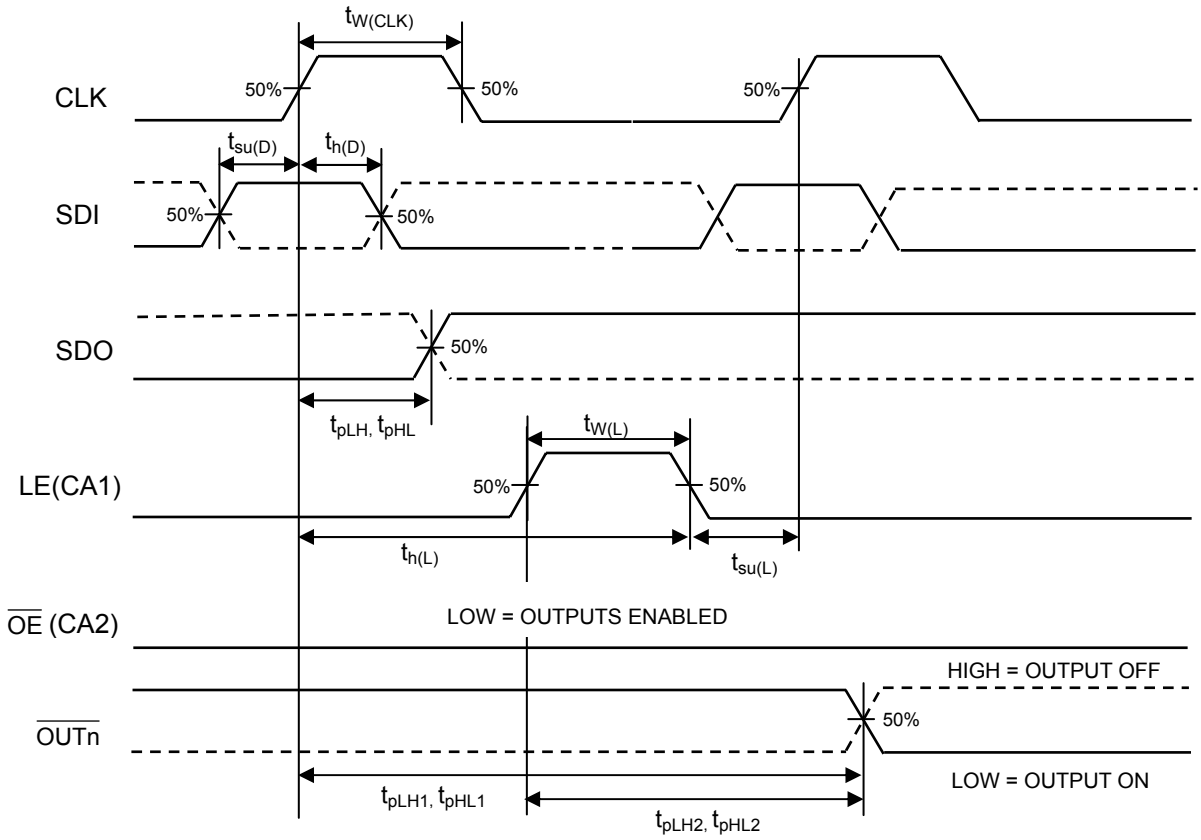
**If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

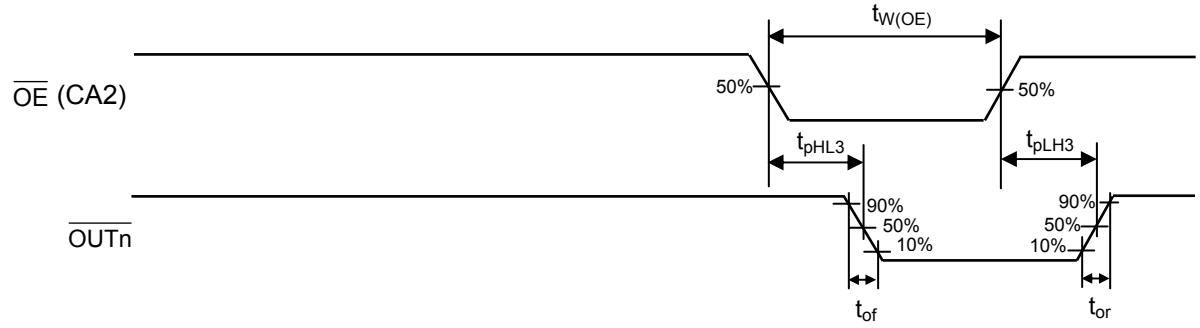
Test Circuit for Switching Characteristics



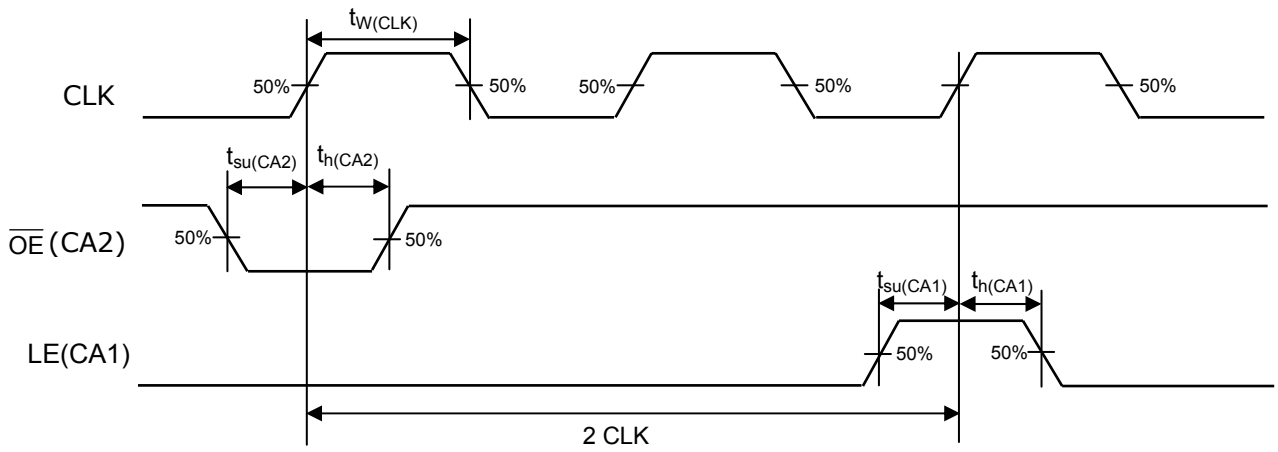
Timing Waveform

Normal Mode





Switching to Current Adjust Mode



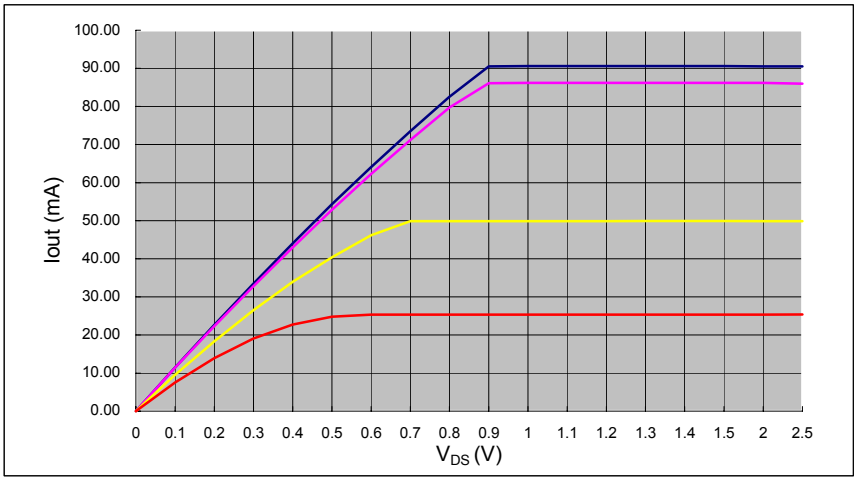
Application Information

Constant Current

In LED display applications, MBI5028 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

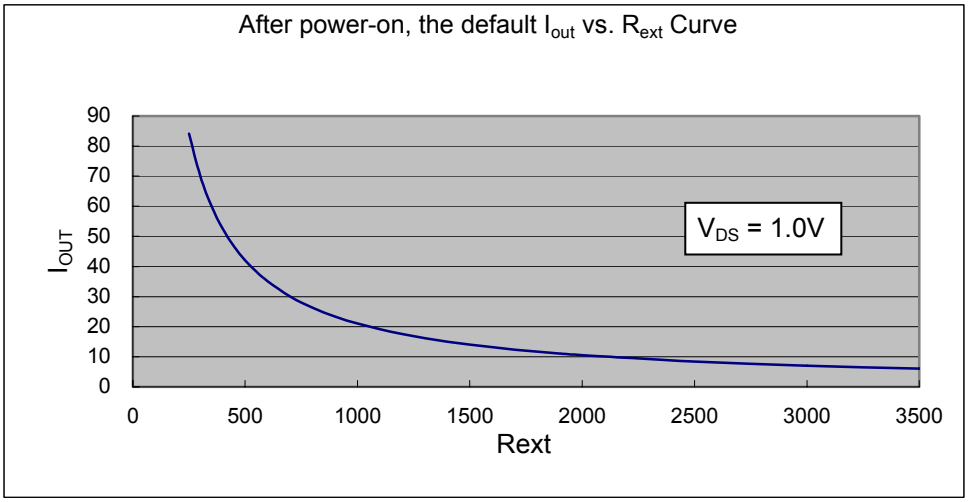
1) The maximum current variation between channels is less than ±3%, and that between ICs is less than ±10%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (Vf). This performs as a perfection of load regulation.



Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. After power-on, the default relationship between I_{out} and R_{ext} is shown in the following figure.



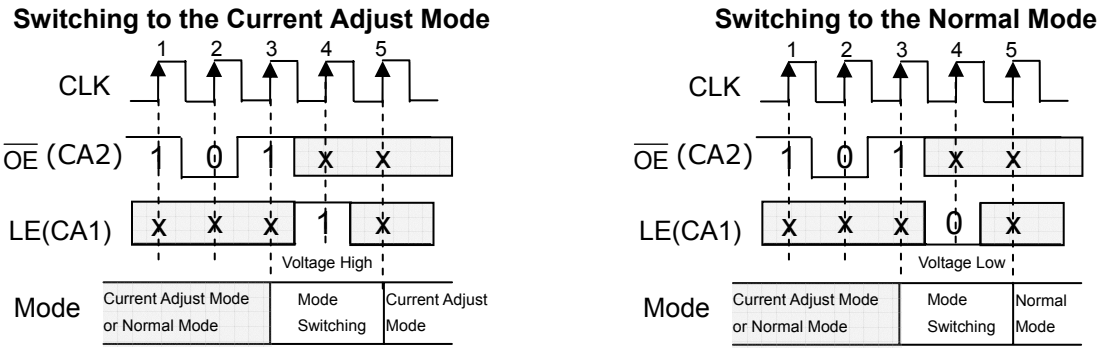
Resistance of the external resistor, R_{ext}, in Ω

Also, the output current can be calculated from the equations:

$V_{R\text{-}EXT}$ = 1.4175Volt x G ; I_{OUT} = ($V_{R\text{-}EXT}$ / R_{ext}) x 15

where R_{ext}, is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. Conceptually, G is the digital current gain, defined by the Current Adjust Code. After power-on, the default value of G is 0.9896. Based on the default gain, I_{OUT} = (1.4175Volt x 0.9896 / R_{ext}) x 15 = (1.4027Volt/ R_{ext}) x 15, if another end of the resistor R_{ext} is connected to the ground. The magnitude of current is around 52.1mA at 404Ω and 26.0mA at 809Ω. The section “16-bit Configuration Code” would describe how to set up the gain, G.

Operation Mode Switching

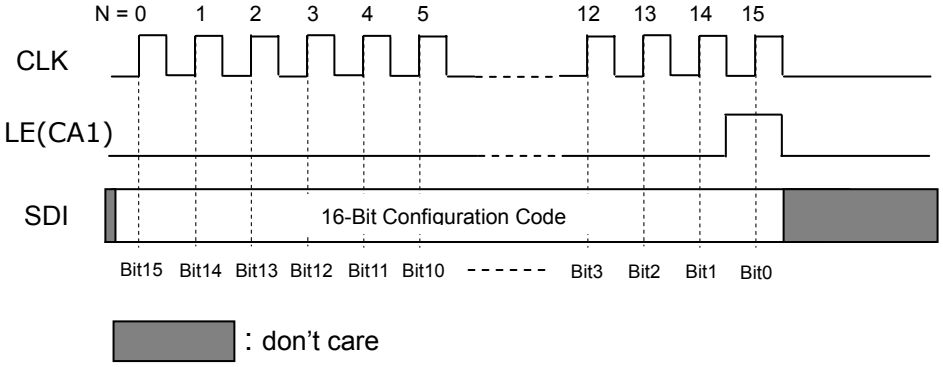


As shown in the above figures, once a short pulse "101" of $\overline{OE}$ (CA2) appears, MBI5028 would go through the mode switching. At the fourth rising edge of CLK, if LE(CA1) is sampled as " Voltage High", MBI5028 would switch to the Current Adjust mode; otherwise, it would switch to the Normal Mode. Worthwhile noticing, the signal LE(CA1) between the third and the fifth rising edges of CLK can not latch any data. Its level is just used for determining which mode to switch. However, the short pulse of $\overline{OE}$ (CA2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI pin and shifted out from SDO pin.

Note:

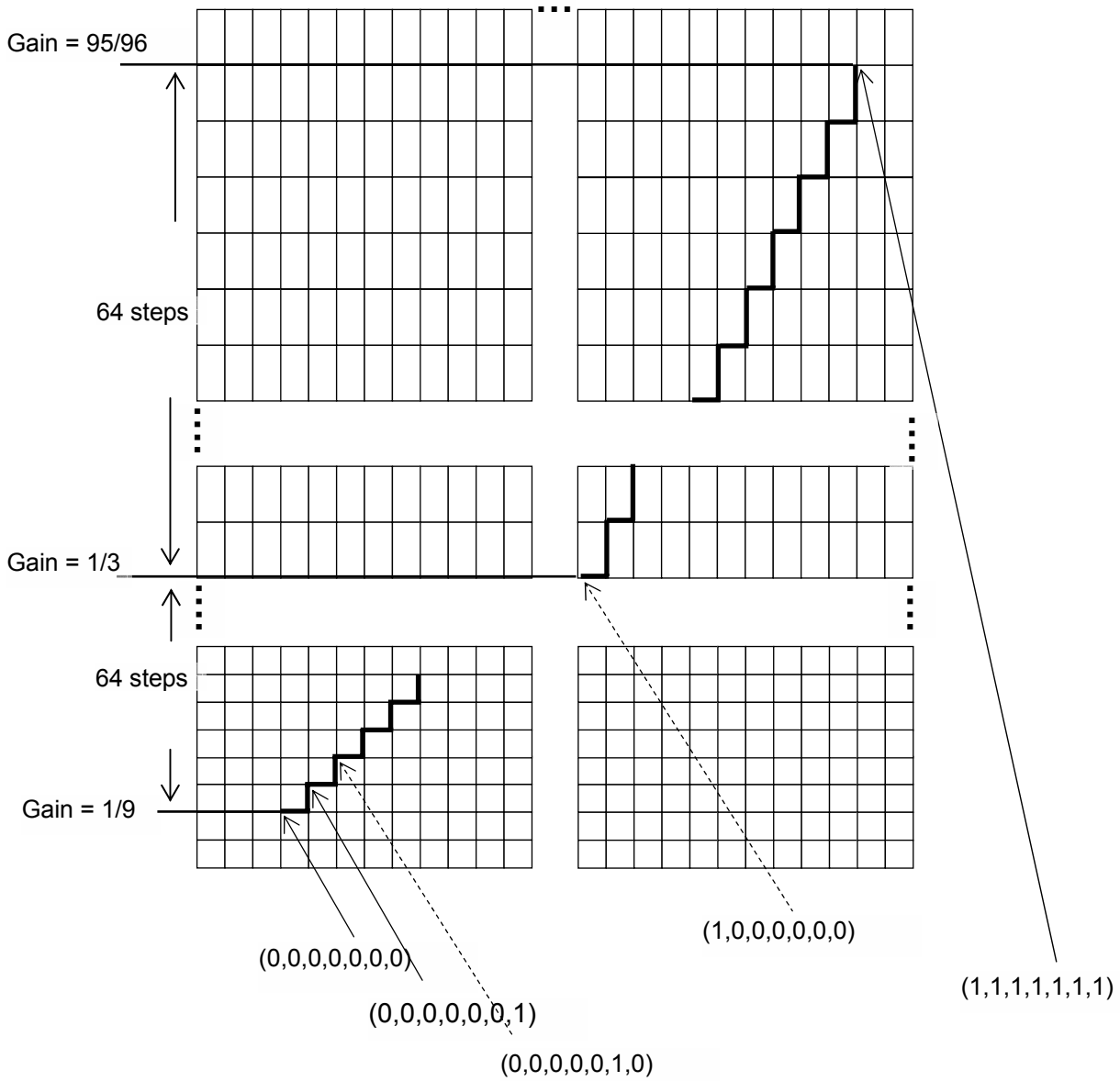
1. The signals for mode switching could be used for making sure under which mode MBI5028 is working.
2. The aforementioned "1" and "0" are sampled at the rising edge of CLK. The "X" means its level would not affect the result of mode switching.
3. After power-on, the default operation mode is Normal mode.

Writing Configuration Code



After entering the Current Adjust mode, the system controller sends a 7-bit Current Adjust code to 16-bit Shift Register through MBI5028 SDI pin. Then sending LE(CA1) active pulse will transfer the contents in the Shift Register to a 16-bit Configuration Latch rather than the 16-bit Output Latch in a Normal mode. The 7-bit Current Adjust code in the Configuration Latch will directly affect the voltage at R-EXT terminal and output current I_{out} by the gain, G. The output current resulted by the gain values will be then defined as: (1.4175Volt x G / R_{ext}) x 15. The gain will always be effective until power off or the Configuration Latch is re-written.

Current Gain



16-Bit Configuration Code

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
Meaning	-	HC	CC0	CC1	CC2	CC3	CC4	CC5	-	-	-	-	-	-	-	-
Default Value	-	1	1	1	1	1	1	1	-	-	-	-	-	-	-	-

← 7-bit Current Adjust Code →

Note: "-" means "reserved and not used now"

The relationship between the Current Adjust Code HC, CC〔0:5〕} and current gain G is shown below:

$G = [(1 + 2 \times HC)/3] \times [(1 + D/32)/3]$

where HC is 1 or 0 (HC=0 : Low current band; HC=1 : High current band) and

$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$;

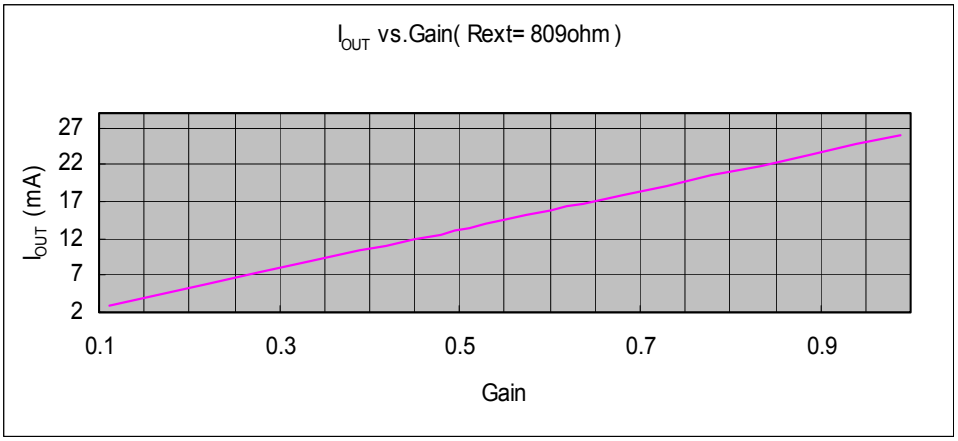
So, the Current Adjust Code is a floating number with one bit exponent HC and 6-bit mantissa.

For example,
when the Current Adjust Code is (1,1,1,1,1,1,1)
Gain, G = [(1 + 2 x 1)/3] x [(1 + 63/32)/3]= 0.9896

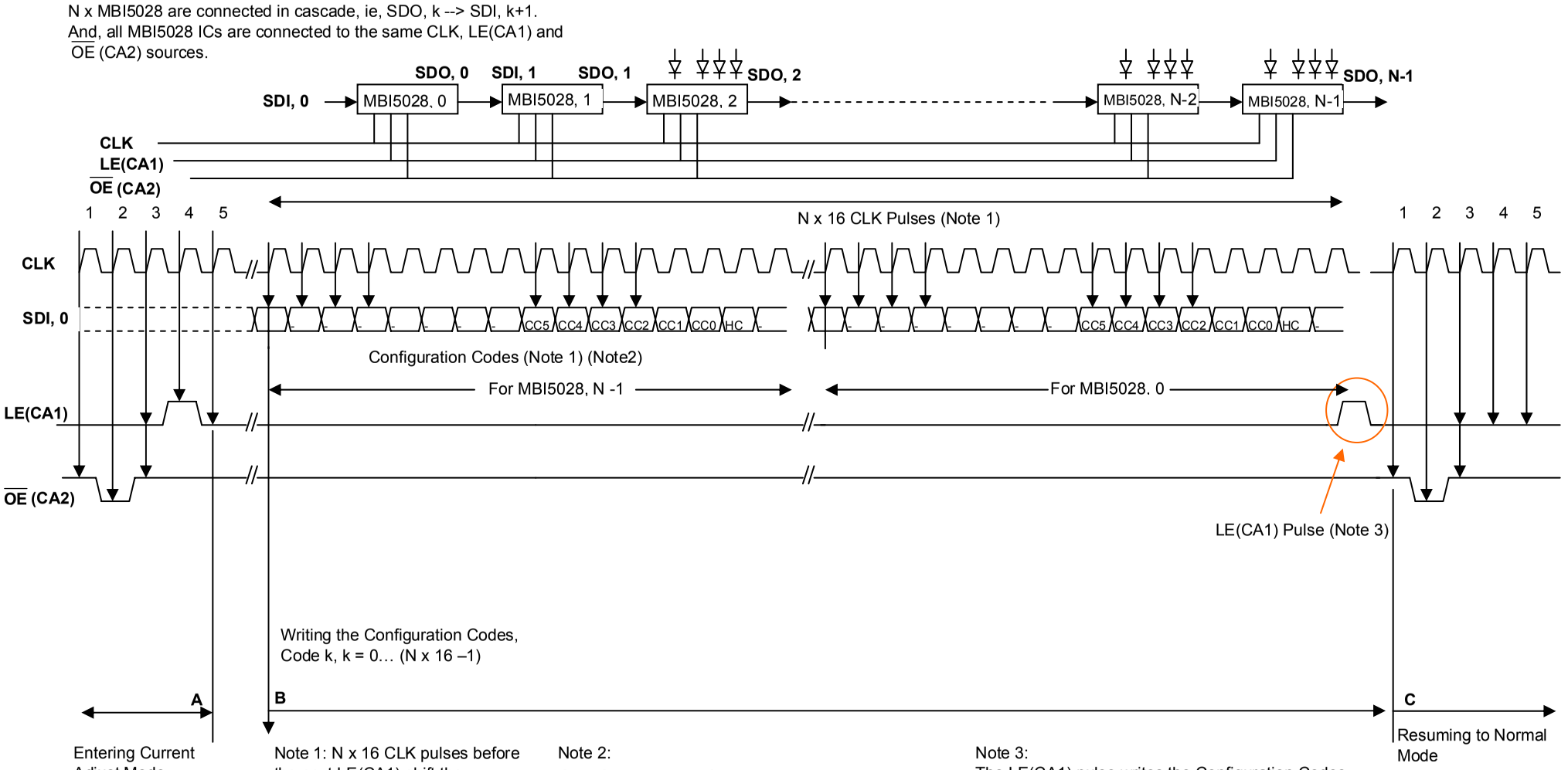
when the Current Adjust Code is (1,0,0,0,0,0,0)
Gain, G = [(1 + 2 x 1)/3] x [(1 + 0/32)/3]= 1/3

when the Current Adjust Code is (0,0,0,0,0,0,0)
Gain, G = [(1 + 2 x 0)/3] x [(1 + 0/32)/3]= 1/9

After power on, the default value of Current Adjust Code is (1,1,1,1,1,1,1). Thus, G is 0.9896.
Typically, the output current resulted by the digital current gain, G, is shown as the figure below.

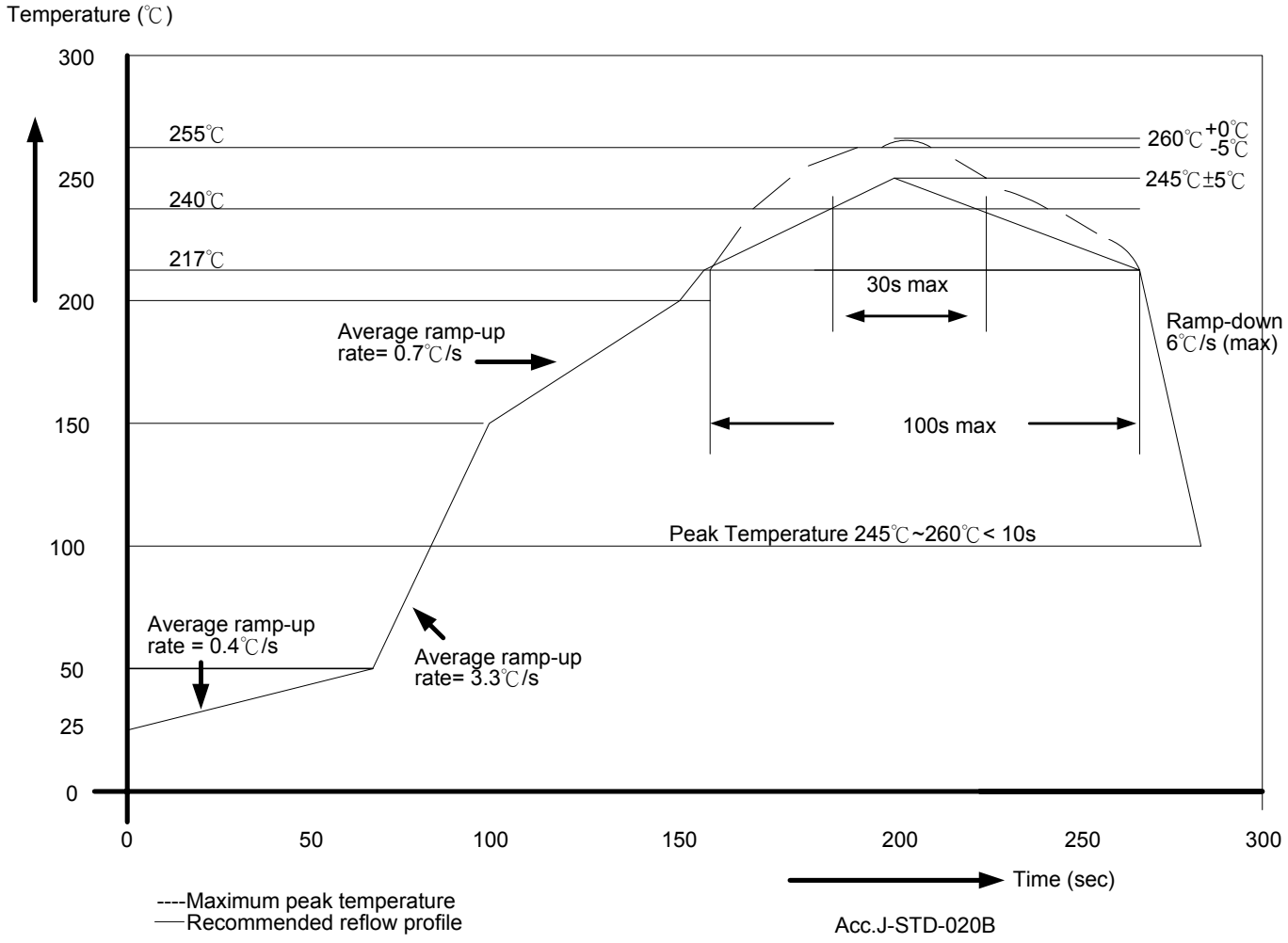


Timing Chart for Current Adjust Mode (An Example)



Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defines "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin** (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020B as shown below.



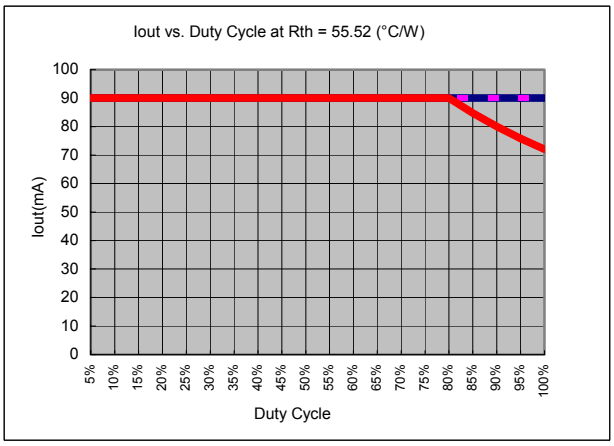
*Note1: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (P_D)

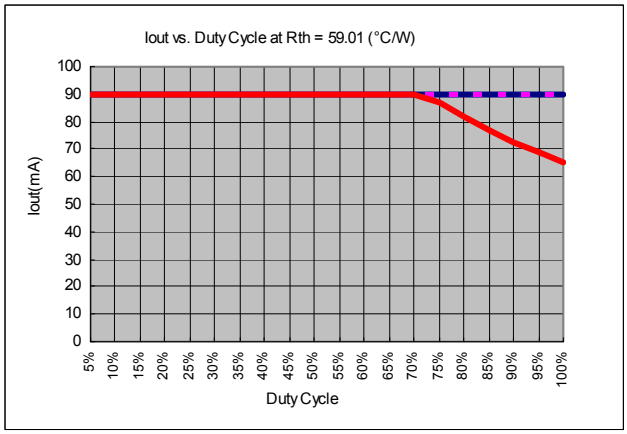
The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$. Therefore, to keep $P_D(act) \leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT} = \{ [(Tj – Ta) / R_{th(j-a)}] – (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 16,$

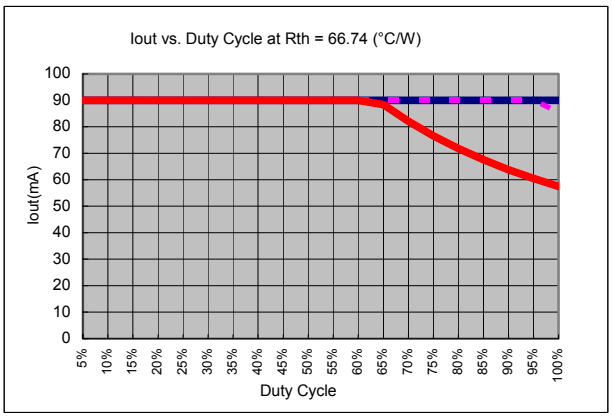
where Tj = 150°C.



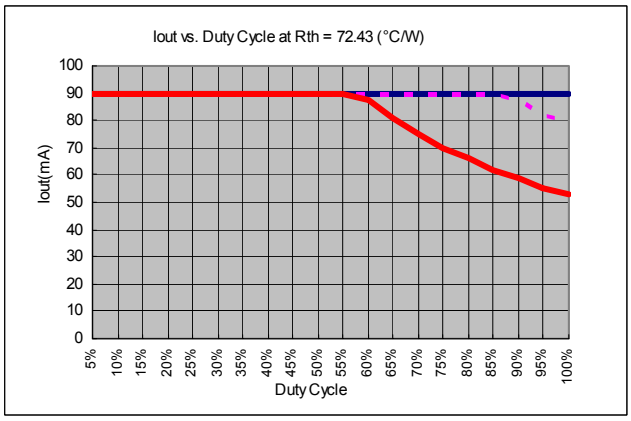
CN\GN type package



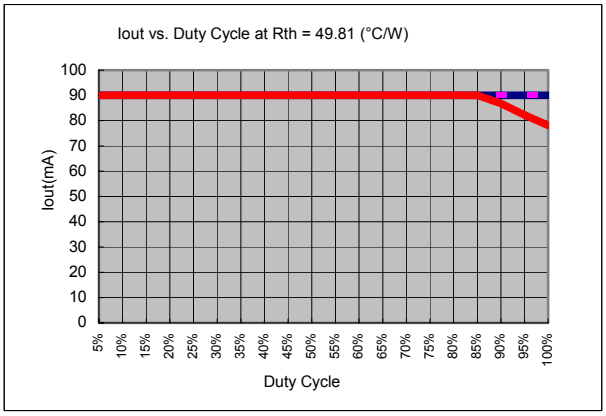
CF\GF type package



CNS\GNS type package



CP\CPA\GP\GPA type package

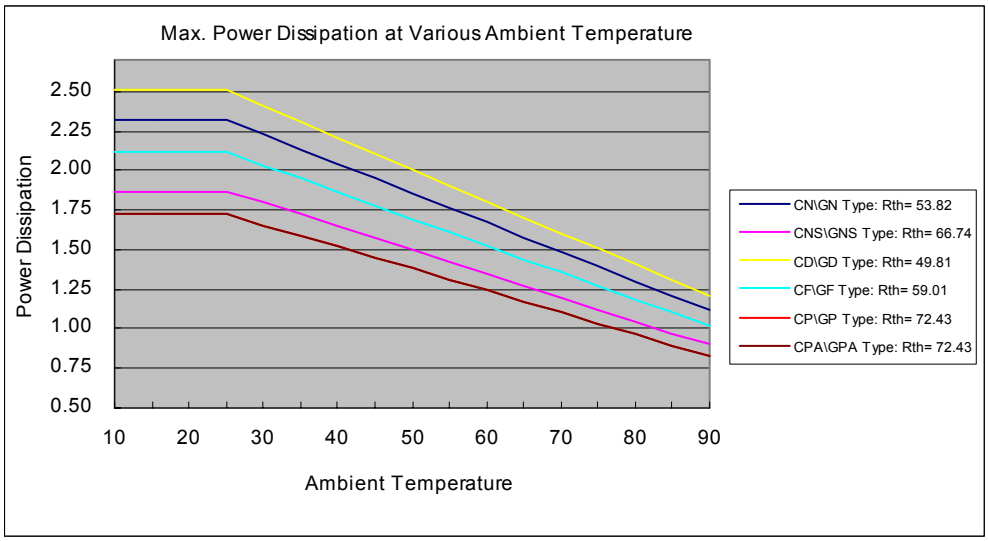


CD type package

Condition : I_{out} = 90mA , V_{DS} = 1.0V , 16 output channels active

Device Type		$R_{th(j-a)}$(°C/W)		Note
CN	GN	55.52	49.90	Ta = 25℃ Ta = 55℃ Ta = 85℃
CNS	GNS	66.74	62.28	
CD	GD	49.81	45.69	
CF	GF	59.01	52.38	
CP\CPA	GP\GPA	72.43	68.48	

The maximum power dissipation, $P_D(max) = (Tj – Ta) / R_{th(j-a)}$, decreases as the ambient temperature increases.

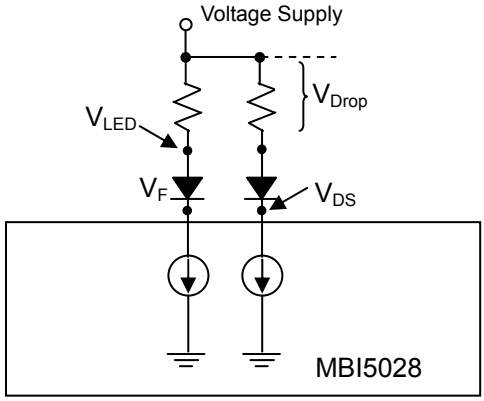


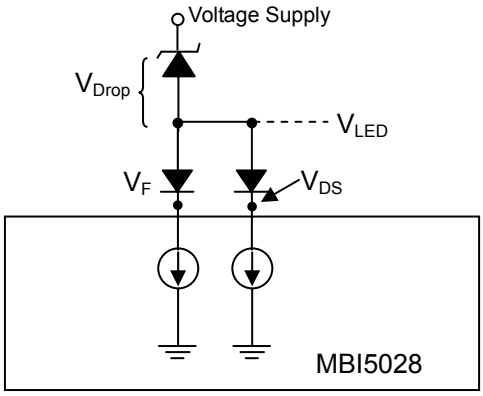
Load Supply Voltage (V_{LED})

MBI5028 are designed to operate with V_{DS} ranging from 0.4V to 1.0V considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED} = 5V and $V_{DS} = V_{LED} – V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer (V_{DROP}).

A voltage reducer lets $V_{DS} = (V_{LED} – V_F) – V_{DROP}$.

Resisters, or Zener diode can be used in the applications as the following figures.

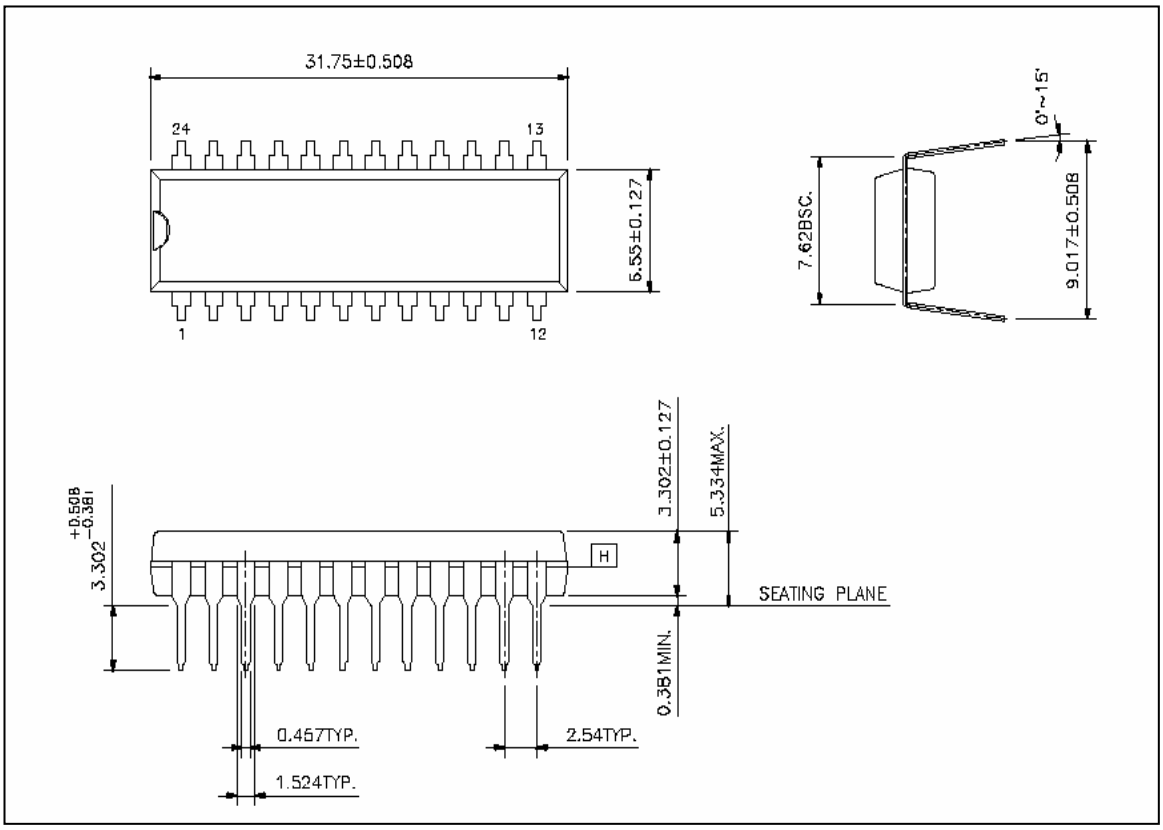




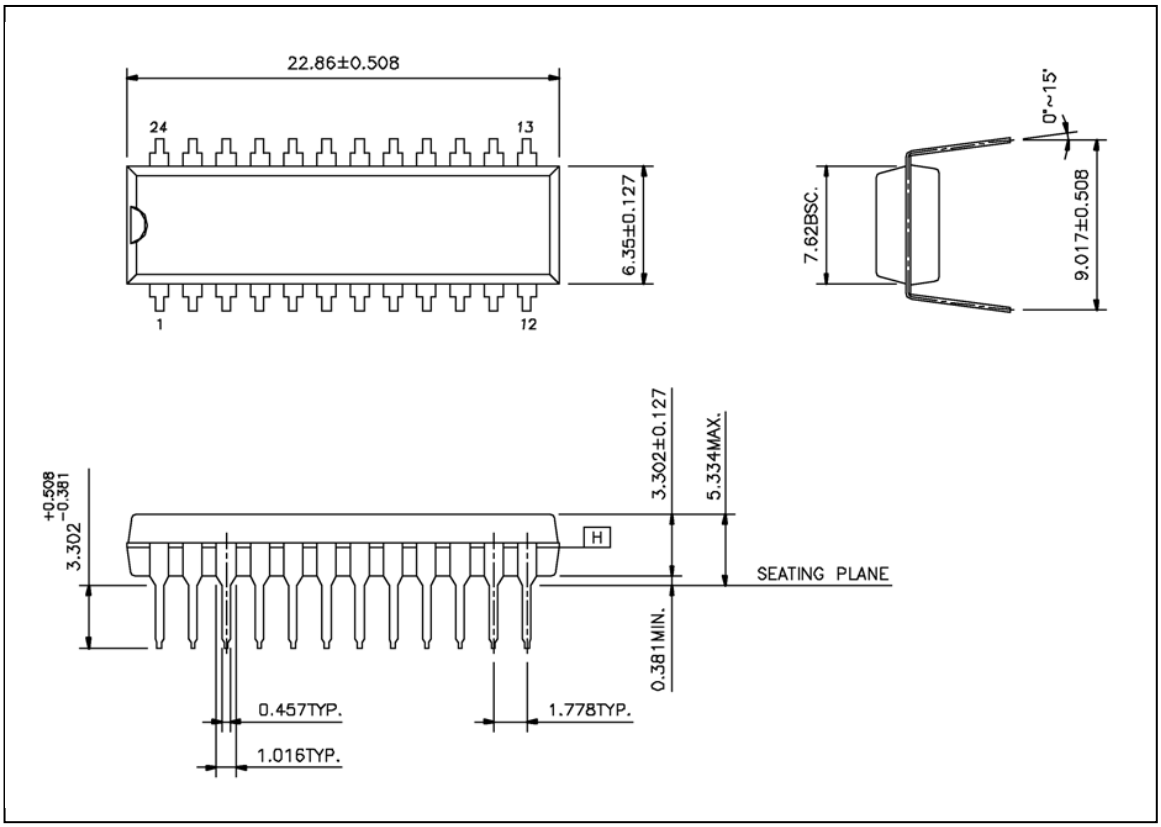
Switching Noise Reduction

LED driver ICs are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

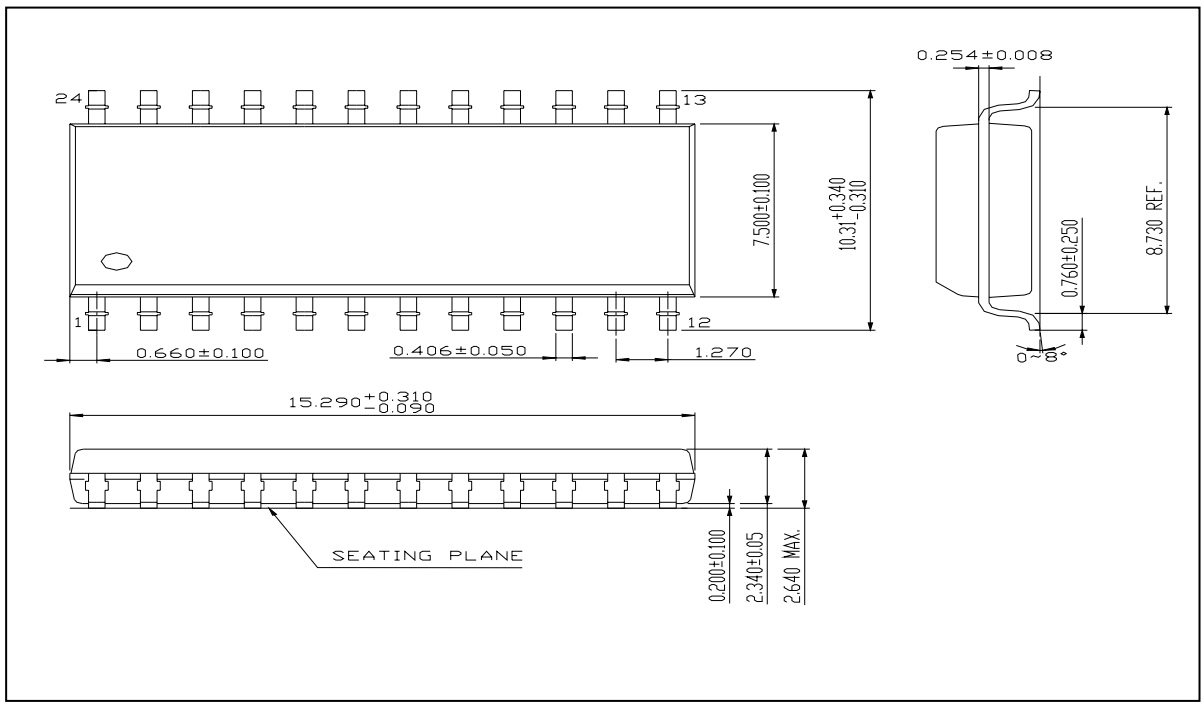
Package Outline



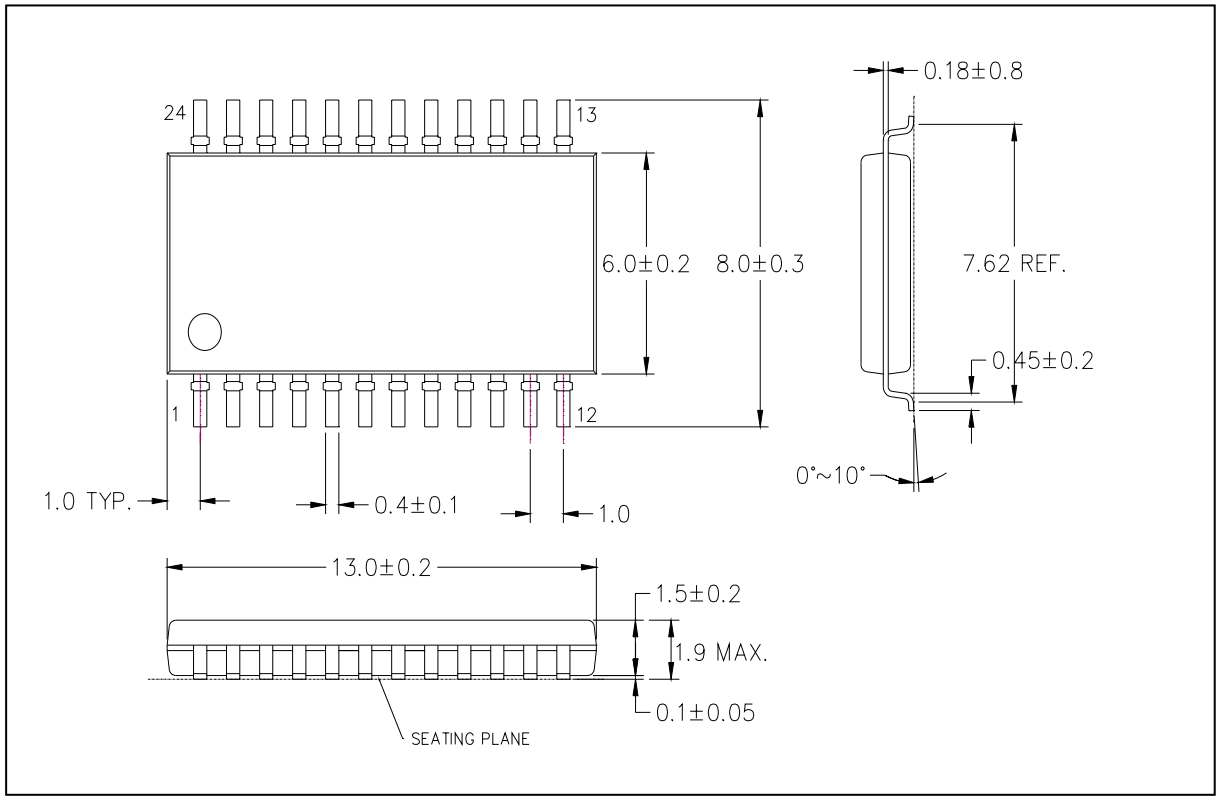
MBI5028CN\GN Outline Drawing



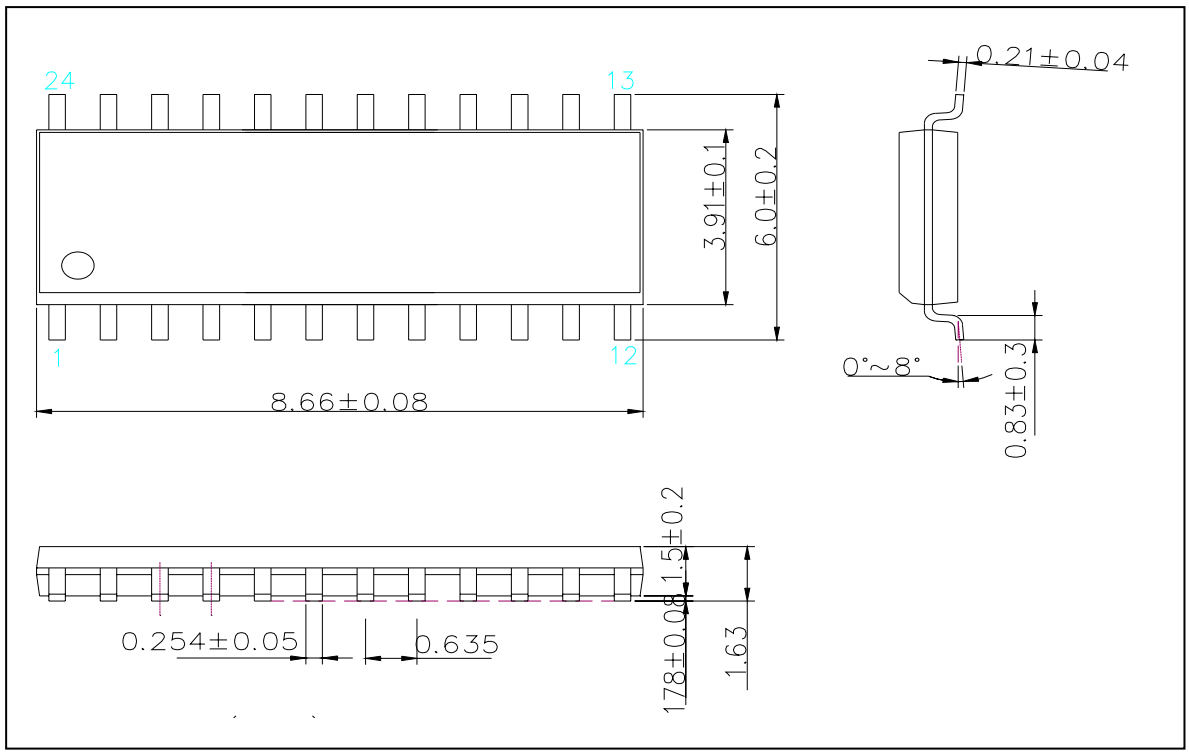
MBI5028CNS\GNS Outline Drawing



MBI5028CD\GD Outline Drawing



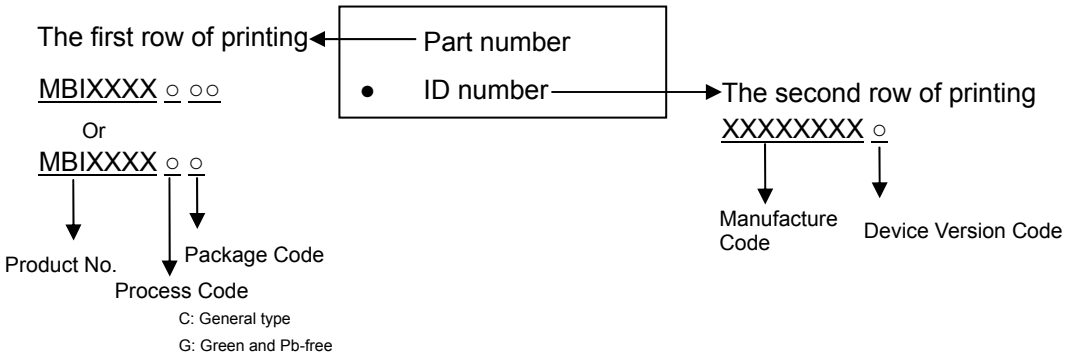
MBI5028CF\GF Outline Drawing



MBI5028CP\CPA\GP\GPA Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
VA.00	*Not defined*
VA.01	A
VA.02	A

Product Ordering Information

Part Number	Package Type	Weight (g)
MBI5028CN	P-DIP24-300-2.54	1.628
MBI5028CNS	SP-DIP24-300-1.78	1.11
MBI5028CD	SOP24-300-1.27	0.617
MBI5028CF	SOP24-300-1.00	0.28
MBI5028CP	SSOP24-150-0.64	0.11
MBI5028CPA	SSOP24-150-0.64	0.11

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5028GN	P-DIP24-300-2.54	1.628
MBI5028GNS	SP-DIP24-300-1.78	1.11
MBI5028GD	SOP24-300-1.27	0.617
MBI5028GF	SOP24-300-1.00	0.28
MBI5028GP	SSOP24-150-0.64	0.11
MBI5028GPA	SSOP24-150-0.64	0.11

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