

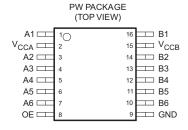
# 6-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO-DIRECTION SENSING AND ±15-kV ESD PROTECTION

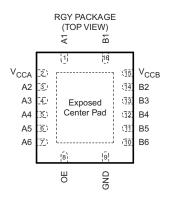
Check for Samples: TXB0106

#### **FEATURES**

- 1.2 V to 3.6 V on A Port and 1.65 to 5.5 V on B Port (V<sub>CCA</sub>≤ V<sub>CCB</sub>)
- V<sub>CC</sub> Isolation Feature If Either V<sub>CC</sub> Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V<sub>CCA</sub>
- Low Power Consumption, 4-μA Max I<sub>CC</sub>
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 150-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - ±15-kV Human-Body Model (A114-B)
    - 150-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)





- A. The exposed center pad, if used, must be connected as a secondary ground or left electrically open.
- B. Pull up resistors are not required on both sides for Logic I/O.
- C. If pull up or pull down resistors are needed, the resistor value must be over 50 k $\Omega$ .
- D. 50 k $\Omega$  is a safe recommended value, if the customer can accept higher Vol or lower Voh, smaller pull up or pull down resistor is allowed, the draft estimation is Vol = Vccout × 4.5k/(4.5k + Rpu) and Voh = Vccout × Rdw/(4.5k + Rdw).
- E. If pull up resistors are needed, please refer to the TXS0108 (different package with TXB0106) or contact TI.
- F. For detailed information, please refer to application note SCEA043.

#### DESCRIPTION/ORDERING INFORMATION

This 6-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.  $V_{CCA}$  should not exceed  $V_{CCB}$ .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0106 is designed so that the OE input circuit is supplied by V<sub>CCA</sub>.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **Table 1. ORDERING INFORMATION**

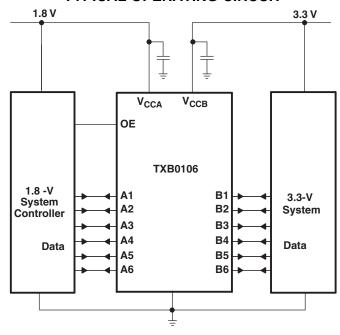
T <sub>A</sub>	PACKAGE	(1) (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	TXB0106RGYR	YE06
-40 C to 65 C	TSSOP - PW	Reel of 2000	TXB0106PWR	YE06

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

#### **PIN DESCRIPTION**

NO.	NAME	FUNCTION
1	A1	Input/output 1. Referenced to V <sub>CCA</sub> .
2	V <sub>CCA</sub>	A-port supply voltage. 1.2 V $\leq$ V <sub>CCA</sub> $\leq$ 3.6 V, V <sub>CCA</sub> $\leq$ V <sub>CCB</sub> .
3	A2	Input/output 2. Referenced to V <sub>CCA</sub> .
4	А3	Input/output 3. Referenced to V <sub>CCA</sub> .
5	A4	Input/output 4. Referenced to V <sub>CCA</sub> .
6	A5	Input/output 5. Referenced to V <sub>CCA</sub> .
7	A6	Input/output 6. Referenced to V <sub>CCA</sub> .
8	OE	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to $V_{\text{CCA}}$ .
9	GND	Ground
10	В6	Input/output 6. Referenced to V <sub>CCB</sub> .
11	B5	Input/output 5. Referenced to V <sub>CCB</sub> .
12	B4	Input/output 4. Referenced to V <sub>CCB</sub> .
13	В3	Input/output 3. Referenced to V <sub>CCB</sub> .
14	B2	Input/output 2. Referenced to V <sub>CCB</sub> .
15	V <sub>CCB</sub>	B-port supply voltage. 1.65 V ≤ V <sub>CCB</sub> ≤ 5.5 V.
16	B1	Input/output 1. Referenced to V <sub>CCB</sub> .

#### **TYPICAL OPERATING CIRCUIT**





# ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$	Supply voltage range		-0.5	4.6	V
$V_{CCB}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)	ange <sup>(2)</sup> -		6.5	V
Vo	Voltage range applied to any output in the high-impedance or power	r-off state <sup>(2)</sup>	-0.5	6.5	V
\/	Valence represented to a construct in the bight and acceptable (2) (3)	A inputs	-0.5	V <sub>CCA</sub> + 0.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)	B inputs	-0.5	V <sub>CCB</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		<b>-</b> 50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
	Darland the condition of the condition	PW package <sup>(4)</sup>		83	00044
JA	Package thermal impedance	RGY package <sup>(5)</sup>		37	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup> (2)

			V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
$V_{CCA}$	Cupply voltage				1.2	3.6	V
$V_{CCB}$	Supply voltage				1.65	5.5	V
\/	High lovel input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V <sub>CCI</sub> × 0.65 <sup>(3)</sup>	V <sub>CCI</sub>	V
V <sub>IH</sub>	High-level input voltage	OE	1.2 V tO 3.6 V	1.65 V to 5.5 V	V <sub>CCA</sub> × 0.65	5.5	V
V	Low lovel input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	$V_{CCI} \times 0.35^{(3)}$	V
V <sub>IL</sub>	Low-level input voltage	OE	1.2 V to 3.6 V	1.65 V 10 5.5 V	0	V <sub>CCA</sub> × 0.35	V
		A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	
$\Delta t/\Delta v$	Input transition rise or fall rate	D port inpute	1.2.\/ to 2.6.\/	1.65 V to 3.6 V		40	ns/V
	noo or rain rato	B-port inputs	1.2 V to 3.6 V	4.5 V to 5.5 V		30	
$T_A$	Operating free-air temperate	ure	_		-40	85	°C

The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V<sub>CCI</sub> or both at GND.

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The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

The value of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.

The package thermal impedance is calculated in accordance with JESD 51-7.
The package thermal impedance is calculated in accordance with JESD 51-5.

 $V_{CCA}$  must be less than or equal to  $V_{CCB}$  and must not exceed 3.6 V.  $V_{CCI}$  is the supply voltage associated with the input port.



# ELECTRICAL CHARACTERISTICS(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

<b>D</b>	ARAMETER	TEST	V	V	T,	<sub>λ</sub> = 25°C	:	–40°C to 8	35°C	UNIT
P	ARAMETER	CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNI
V		J 20A	1.2 V			1.1				V
$V_{OHA}$		$I_{OH} = -20 \mu A$	1.4 V to 3.6 V					V <sub>CCA</sub> - 0.4		V
.,		1 00 1	1.2 V			0.9				
$V_{OLA}$		$I_{OL} = 20 \mu A$	1.4 V to 3.6 V						0.4	V
V <sub>OHB</sub>		I <sub>OH</sub> = -20 μA		1.65 V to 5.5 V				V <sub>CCB</sub> - 0.4		V
V <sub>OLB</sub>		I <sub>OL</sub> = 20 μA		1.65 V to 5.5 V					0.4	V
l <sub>l</sub>	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	μΑ
	A port		0 V	0 V to 5.5 V			±1		±2	
l <sub>off</sub>	B port		0 V to 3.6 V	0 V			±1		±2	μΑ
loz	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	μΑ
			1.2 V	4.05.77 5.5.77		0.06				
		$V_I = V_{CCI}$ or GND,	1.4 V to 3.6 V	1.65 V to 5.5 V					5	
I <sub>CCA</sub>		$I_{O} = 0$	3.6 V	0 V					2	μΑ
			0 V	5.5 V				2		
			1.2 V	4.05.1/1- 5.5.1/		3.4				
		$V_I = V_{CCI}$ or GND,	1.4 V to 3.6 V	1.65 V to 5.5 V					5	
I <sub>CCB</sub>		$I_0 = 0$	3.6 V	0 V					-2	μΑ
			0 V	5.5 V					2	
		$V_I = V_{CCI}$ or GND,	1.2 V	4.05.77 5.5.77		3.5				
I <sub>CCA</sub> +	ICCB	$I_{O} = 0$	1.4 V to 3.6 V	1.65 V to 5.5 V					10	μΑ
		$V_I = V_{CCI}$ or GND,	1.2 V			0.05				
I <sub>CCZA</sub>		I <sub>O</sub> = 0, OE = GND	1.4 V to 3.6 V	1.65 V to 5.5 V	V to 5.5 V		5	μA		
		$V_I = V_{CCI}$ or GND,	1.2 V			3.3				
I <sub>CCZB</sub>		I <sub>O</sub> = 0, OE = GND	1.4 V to 3.6 V	1.65 V to 5.5 V					5	μΑ
Cı	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	5			5.5	pF	
<u> </u>	A port		4.2.V.to 2.6.V	1 CE \/ to E E \/		5			6.5	"F
$C_{io}$	B port		1.2 V to 3.6 V	1.65 V to 5.5 V		8			10	pF

## **TIMING REQUIREMENTS**

 $T_A = 25^{\circ}C, V_{CCA} = 1.2 \text{ V}$ 

			V <sub>CCB</sub> = 1.8 V	V <sub>CCB</sub> = 2.5 V	V <sub>CCB</sub> = 3.3 V	V <sub>CCB</sub> = 5 V	UNIT
			TYP	TYP	TYP	TYP	UNII
	Data rate		20	20	20	20	Mbps
t <sub>w</sub>	Pulse duration	Data inputs	50	50	50	50	ns

#### **TIMING REQUIREMENTS**

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (unless otherwise noted)

				V <sub>CCB</sub> = 1.8 V ± 0.15 V			V <sub>CCB</sub> = 3.3 V V <sub>CCB</sub> = 5 V ± 0.3 V ± 0.5 V			UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t <sub>w</sub>	Pulse duration	Data inputs	20		20		20		20		ns

Product Folder Link(s): TXB0106

 $<sup>\</sup>begin{array}{ll} \hbox{(1)} & V_{CCI} \ \hbox{is the supply voltage associated with the input port.} \\ \hbox{(2)} & V_{CCO} \ \hbox{is the supply voltage associated with the output port.} \end{array}$ 



#### **TIMING REQUIREMENTS**

over recommended operating free-air temperature range,  $V_{CCA}$  = 1.8 V ± 0.15 V (unless otherwise noted)

				V <sub>CCB</sub> = 1.8 V ± 0.15 V			c <sub>CB</sub> = 3.3 V V <sub>CCB</sub> = 5 V ± 0.3 V ± 0.5 V			UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t <sub>w</sub>	Pulse duration	Data inputs	19		17		17		17		ns

#### **TIMING REQUIREMENTS**

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

			V <sub>CCB</sub> = 2 ± 0.2		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t <sub>w</sub>	Pulse duration	Data inputs	14		10		10		ns

#### TIMING REQUIREMENTS

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

			V <sub>CCB</sub> = 3 ± 0.3	.3 V V	V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t <sub>w</sub>	Pulse duration	Data inputs	10		10		ns

#### **SWITCHING CHARACTERISTICS**

 $T_A = 25^{\circ}C, V_{CCA} = 1.2 \text{ V}$ 

PARAMETER	FROM	то	V <sub>CCB</sub> = 1.8 V	V <sub>CCB</sub> = 2.5 V	V <sub>CCB</sub> = 3.3 V	V <sub>CCB</sub> = 5 V	UNIT
FARAWIETER	(INPUT)	(OUTPUT)	TYP	TYP	TYP	TYP	ONII
	Α	В	9.5	7.9	7.6	8.5	
t <sub>pd</sub>	В	А	9.2	8.8	8.4	8	ns
	OF	А	1	1	1	1	
t <sub>en</sub>	OE	В	1	1	1	1	μs
	OF.	А	20	17	17	18	
t <sub>dis</sub>	OE	В	20	16	15	15	ns
t <sub>rA</sub> , t <sub>fA</sub>	A-port rise a	nd fall times	4.1	4.4	4.1	3.9	ns
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise a	nd fall times	5	5	5.1	5.1	ns
t <sub>SK(O)</sub>	Channel-to-c	hannel skew	2.4	1.7	1.9	7	ns
Max data rate			20	20	20	20	Mbps

Product Folder Link(s): TXB0106



#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)			1.8 V 5 V	V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	В	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	
t <sub>pd</sub>	В	Α	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	ns
	OE	Α		1		1		1		1	
t <sub>en</sub>	OE	В		1		1		1		1	μs
	٥٢	Α	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	
t <sub>dis</sub>	OE	В	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	ns
t <sub>rA</sub> , t <sub>fA</sub>	A-port rise a	and fall times	8.0	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise a	and fall times	1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
t <sub>SK(O)</sub>	Channel-to-c	channel skew		2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (unless otherwise noted)

PARAMETER	PARAMETER FROM (INPUT)		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
	Α	В	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5		
t <sub>pd</sub>	В	Α	1.5	12	1.2	8.4	0.8	7.6	0.5	7.1	ns	
	OE	Α		1		1		1		1		
t <sub>en</sub>	OE	В		1		1		1		1	μs	
	0.5	Α	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7		
$t_{dis}$	OE	В	6.1	33.9	5.2	23.7	5	19.9	5	17.6	ns	
t <sub>rA</sub> , t <sub>fA</sub>	A-port rise a	nd fall times	0.7	5.1	0.7	5	1	5	0.7	5	ns	
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns	
t <sub>SK(O)</sub>	Channel-to-c	hannel skew		0.8		0.7		0.6		0.6	ns	
Max data rate			52		60		60		60		Mbps	



#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = ± 0.3		V <sub>CCB</sub> = ± 0.5	UNIT		
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX		
	Α	В	1.1	6.4	1	5.3	0.9	4.7	20	
t <sub>pd</sub>	В	A	1	7	0.6	5.6	0.3	4.4	ns	
	0.5	A		1		1		1		
t <sub>en</sub>	OE	В		1		1		1	μs	
	0.5	A	5	16.9	4.9	15	4.5	13.8		
t <sub>dis</sub>	OE	В	4.8	21.8	4.5	17.9	4.4	15.2	ns	
$t_{rA}, t_{fA}$	A-port rise a	and fall times	0.8	3.6	0.6	3.6	0.5	3.5	ns	
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise a	and fall times	0.6	4.9	0.7	3.9	0.6	3.2	ns	
t <sub>SK(O)</sub>	Channel-to-c	channel skew		0.4		0.3		0.3	ns	
Max data rate			70		100		100		Mbps	

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CCB</sub> = 3 ± 0.3		V <sub>CCB</sub> = ± 0.5	UNIT		
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX		
	A	В	0.9	4.9	0.8	4		
t <sub>pd</sub>	В	A	0.5	5.4	0.2	4	ns	
	0.5	A		1		1		
t <sub>en</sub>	OE	В		1	1		μs	
	0.5	A	4.5	13.9	4.1	12.4		
t <sub>dis</sub>	OE	В	4.1	17.3	4	14.4	ns	
$t_{rA}, t_{fA}$	A-port rise a	and fall times	0.5	3	0.5	3	ns	
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise a	and fall times	0.7	3.9	0.6	3.2	ns	
t <sub>SK(O)</sub>	Channel-to-c	channel skew		0.4		0.3	ns	
Max data rate			100		100		Mbps	

Product Folder Link(s): TXB0106



# **OPERATING CHARACTERISTICS**

 $T_A = 25^{\circ}C$ 

						V <sub>CCA</sub>					
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V		
			V <sub>CCB</sub>								
	PARAMETER	TEST CONDITIONS	5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	UNIT	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP		
C	A-port input, B-port output	C = 0 f = 10 MHz	9	8	7	7	7	7	8	pF	
C <sub>pdA</sub>	B-port input, A-port output	$C_L = 0$ , $f = 10 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$ ,	12	11	11	11	11	11	11		
C	A-port input, B-port output	OE = V <sub>CCA</sub>	35	26	27	27	27	27	28		
C <sub>pdB</sub>	B-port input, A-port output	(outputs enabled)	26	19	18	18	18	20	21		
C	A-port input, B-port output	C 0 f _ 10 MHz	0.01	0.01	0.01	0.01	0.01	0.01	0.01		
C <sub>pdA</sub>	B-port input, A-port output	$C_L = 0, f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns},$ OE = GND	0.01	0.01	0.01	0.01	0.01	0.01	0.01	+	
C	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03		
C <sub>pdB</sub>	B-port input, A-port output	(outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.03		



#### PRINCIPLES OF OPERATION

## **Applications**

The TXB0106 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

#### **Architecture**

The TXB0106 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0106 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70  $\Omega$  at  $V_{CCO}$  = 1.2 V to 1.8 V, 50  $\Omega$  at  $V_{CCO}$  = 1.8 V to 3.3 V and 40  $\Omega$  at  $V_{CCO}$  = 3.3 V to 5 V.

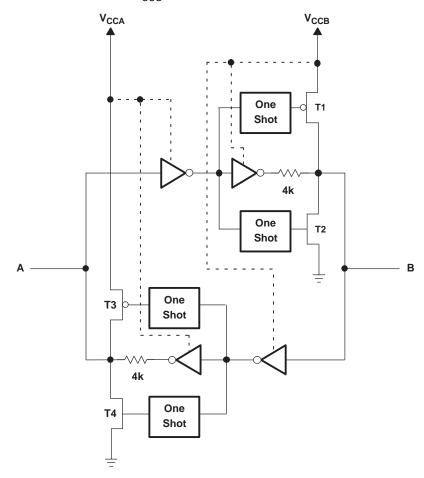


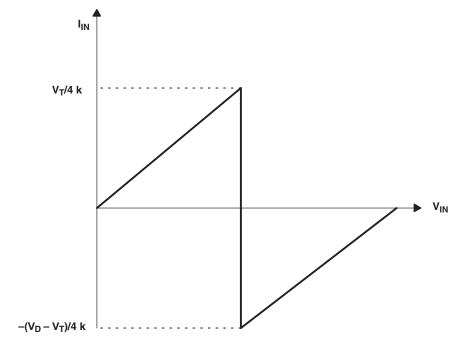
Figure 1. Architecture of TXB0106 I/O Cell

#### **Input Driver Requirements**

Typical  $I_{IN}$  vs  $V_{IN}$  characteristics of the TXB0106 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0106 must have drive strength of at least  $\pm 2$  mA.

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- A.  $V_T$  is the input threshold voltage of the TXB0106 (typically  $V_{CCI}/2$ ).
- B. V<sub>D</sub> is the supply voltage of the external driver.

Figure 2. Typical I<sub>IN</sub> vs V<sub>IN</sub> Curve

#### **Power Up**

During operation, ensure that  $V_{CCA} \le V_{CCB}$  at all times. During power-up sequencing,  $V_{CCA} \ge V_{CCB}$  does not damage the device, so any power supply can be ramped up first. The TXB0106 has circuitry that disables all output ports when either  $V_{CC}$  is switched off ( $V_{CCA/B} = 0 \text{ V}$ ).

#### **Enable and Disable**

The TXB0106 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time ( $t_{dis}$ ) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

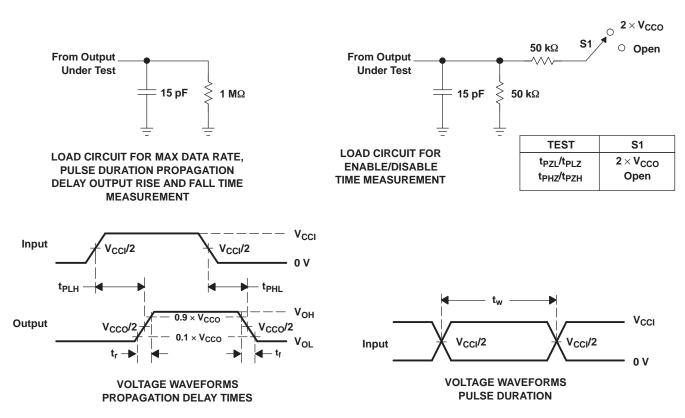
## Pullup or Pulldown Resistors on I/O Lines

The TXB0106 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0106 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k $\Omega$  to ensure that they do not contend with the output drivers of the TXB0106.

For the same reason, the TXB0106 should not be used in applications such as  $I^2C$  or 1-Wire where an opendrain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.



#### PARAMETER MEASUREMENT INFORMATION



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $dv/dt \geq 1 V/ns$ .
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- F.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

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# **REVISION HISTORY**

Ch	Added notes to pin out graphics.	
•	Added notes to pin out graphics.	



# **PACKAGE OPTION ADDENDUM**

7-Nov-2014

#### **PACKAGING INFORMATION**

www.ti.com

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0106PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06	Samples
TXB0106PWRG4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		Samples
TXB0106RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE06	Samples
TXB0106RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE06	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



# **PACKAGE OPTION ADDENDUM**

7-Nov-2014

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#### OTHER QUALIFIED VERSIONS OF TXB0106:

Automotive: TXB0106-Q1

NOTE: Qualified Version Definitions:

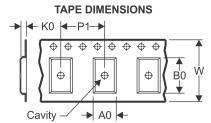
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE MATERIALS INFORMATION

www.ti.com 26-Jan-2013

# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

7 til dilliononono aro momina												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0106PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0106RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

www.ti.com 26-Jan-2013



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0106PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TXB0106RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



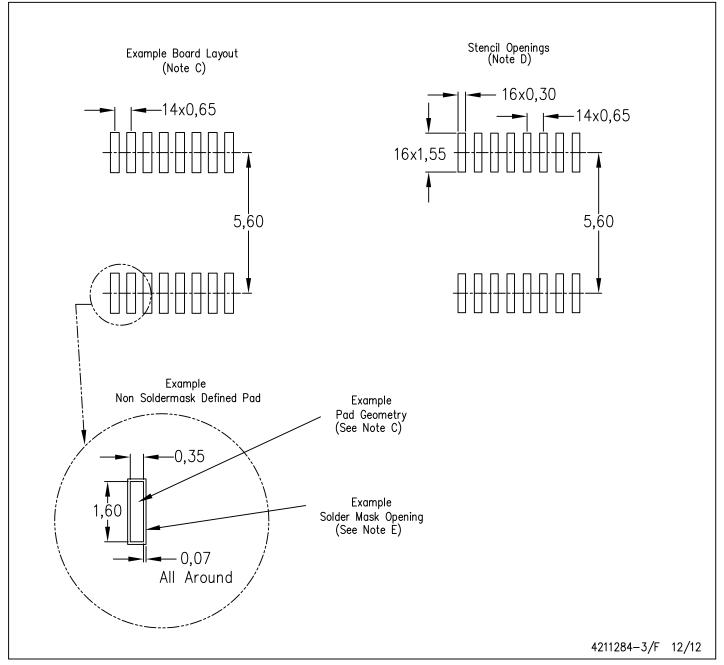
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

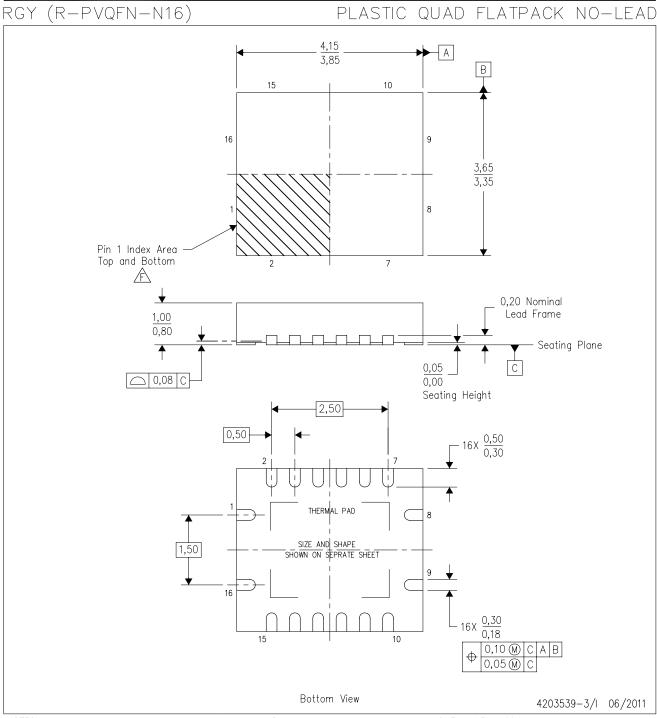
# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



# RGY (R-PVQFN-N16)

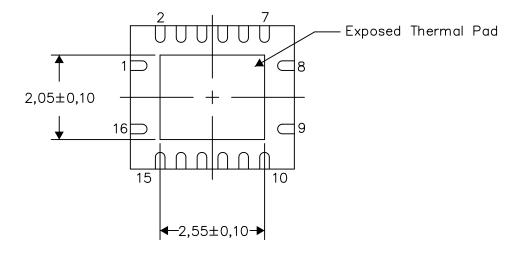
#### PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

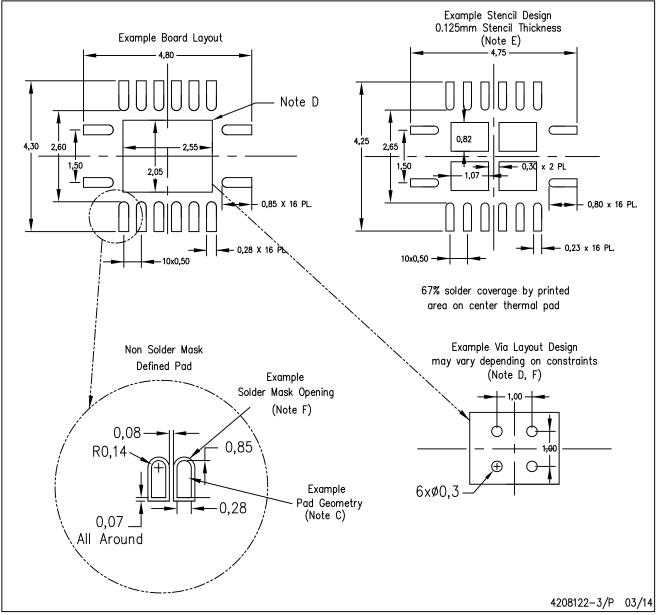
4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



# RGY (R-PVQFN-N16)

# PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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