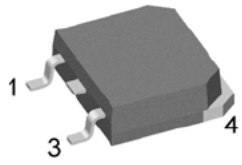
# High Efficiency Thyristor

$V_{RRM}$ = 1200 V
$I_{TAV}$ = 50 A
$V_T$ = 1.27 V

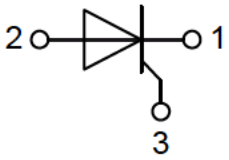
Single Thyristor

**Part number**

CLA50E1200TC




Backside: anode




**Features / Advantages:**

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

**Applications:**

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

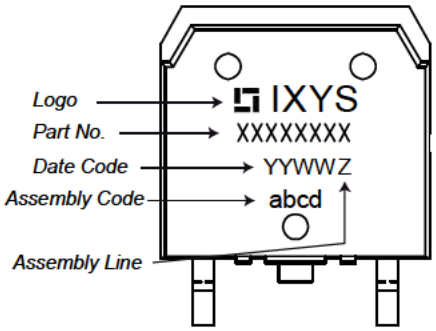
**Package:** TO-268AA (D3Pak)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

| Thyristor | | | | Ratings | | | |
|---|---|---|---|---|---|---|---|
| Symbol | Definition | Conditions | | min. | typ. | max. | Unit |
| $V_{RSM/DSM}$ | *max. non-repetitive reverse/forward blocking voltage* | | $T_{VJ}$ = 25°C | | | 1300 | V |
| $V_{RRM/DRM}$ | *max. repetitive reverse/forward blocking voltage* | | $T_{VJ}$ = 25°C | | | 1200 | V |
| $I_{R/D}$ | *reverse current, drain current* | $V_{R/D}$ = 1200 V | $T_{VJ}$ = 25°C | | | 50 | µA |
| | | $V_{R/D}$ = 1200 V | $T_{VJ}$ = 125°C | | | 4 | mA |
| $V_T$ | *forward voltage drop* | $I_T$ = 50 A | $T_{VJ}$ = 25°C | | | 1.32 | V |
| | | $I_T$ = 100 A | | | | 1.60 | V |
| | | $I_T$ = 50 A | $T_{VJ}$ = 125°C | | | 1.27 | V |
| | | $I_T$ = 100 A | | | | 1.65 | V |
| $I_{TAV}$ | *average forward current* | $T_C$ = 125°C | $T_{VJ}$ = 150°C | | | 50 | A |
| $I_{T(RMS)}$ | *RMS forward current* | 180° sine | | | | 79 | A |
| $V_{T0}$ | *threshold voltage* } *for power loss calculation only* | | $T_{VJ}$ = 150°C | | | 0.88 | V |
| $r_T$ | *slope resistance* } | | | | | 7.7 | mΩ |
| $R_{thJC}$ | *thermal resistance junction to case* | | | | | 0.25 | K/W |
| $R_{thCH}$ | *thermal resistance case to heatsink* | | | | 0.15 | | K/W |
| $P_{tot}$ | *total power dissipation* | | $T_C$ = 25°C | | | 500 | W |
| $I_{TSM}$ | *max. forward surge current* | t = 10 ms; (50 Hz), sine | $T_{VJ}$ = 45°C | | | 650 | A |
| | | t = 8,3 ms; (60 Hz), sine | $V_R$ = 0 V | | | 700 | A |
| | | t = 10 ms; (50 Hz), sine | $T_{VJ}$ = 150°C | | | 555 | A |
| | | t = 8,3 ms; (60 Hz), sine | $V_R$ = 0 V | | | 595 | A |
| $I^2t$ | *value for fusing* | t = 10 ms; (50 Hz), sine | $T_{VJ}$ = 45°C | | | 2.12 | kA²s |
| | | t = 8,3 ms; (60 Hz), sine | $V_R$ = 0 V | | | 2.04 | kA²s |
| | | t = 10 ms; (50 Hz), sine | $T_{VJ}$ = 150°C | | | 1.54 | kA²s |
| | | t = 8,3 ms; (60 Hz), sine | $V_R$ = 0 V | | | 1.48 | kA²s |
| $C_J$ | *junction capacitance* | $V_R$ = 400 V f = 1 MHz | $T_{VJ}$ = 25°C | | 25 | | pF |
| $P_{GM}$ | *max. gate power dissipation* | $t_P$ = 30 µs | $T_C$ = 150°C | | | 10 | W |
| | | $t_P$ = 300 µs | | | | 5 | W |
| $P_{GAV}$ | *average gate power dissipation* | | | | | 0.5 | W |
| $(di/dt)_{cr}$ | *critical rate of rise of current* | $T_{VJ}$ = 150°C; f = 50 Hz | repetitive, $I_T$ = 150 A | | | 150 | A/µs |
| | | $t_P$ = 200 µs; $di_G/dt$ = 0.3 A/µs; | | | | | |
| | | $I_G$ = 0.3A; $V_D$ = ⅔ $V_{DRM}$ | non-repet., $I_T$ = 50 A | | | 500 | A/µs |
| $(dv/dt)_{cr}$ | *critical rate of rise of voltage* | $V_D$ = ⅔ $V_{DRM}$ | $T_{VJ}$ = 150°C | | | 1000 | V/µs |
| | | $R_{GK}$ = ∞; method 1 (linear voltage rise) | | | | | |
| $V_{GT}$ | *gate trigger voltage* | $V_D$ = 6 V | $T_{VJ}$ = 25°C | | | 1.5 | V |
| | | | $T_{VJ}$ = -40°C | | | 1.6 | V |
| $I_{GT}$ | *gate trigger current* | $V_D$ = 6 V | $T_{VJ}$ = 25°C | | | 50 | mA |
| | | | $T_{VJ}$ = -40°C | | | 80 | mA |
| $V_{GD}$ | *gate non-trigger voltage* | $V_D$ = ⅔ $V_{DRM}$ | $T_{VJ}$ = 150°C | | | 0.2 | V |
| $I_{GD}$ | *gate non-trigger current* | | | | | 3 | mA |
| $I_L$ | *latching current* | $t_p$ = 10 µs | $T_{VJ}$ = 25°C | | | 125 | mA |
| | | $I_G$ = 0.3A; $di_G/dt$ = 0.3 A/µs | | | | | |
| $I_H$ | *holding current* | $V_D$ = 6 V $R_{GK}$ = ∞ | $T_{VJ}$ = 25°C | | | 100 | mA |
| $t_{gd}$ | *gate controlled delay time* | $V_D$ = ½ $V_{DRM}$ | $T_{VJ}$ = 25°C | | | 2 | µs |
| | | $I_G$ = 0.3A; $di_G/dt$ = 0.3 A/µs | | | | | |
| $t_q$ | *turn-off time* | $V_R$ = 100 V; $I_T$ = 50 A; $V_D$ = ⅔ $V_{DRM}$ | $T_{VJ}$ = 150°C | | 200 | | µs |
| | | di/dt = 10 A/µs; dv/dt = 20 V/µs; $t_p$ = 200 µs | | | | | |

| Package TO-268AA (D3Pak) | | | Ratings | | | |
|---|---|---|---|---|---|---|
| Symbol | Definition | Conditions | min. | typ. | max. | Unit |
| $I_{RMS}$ | *RMS current* | per terminal | | | 70 | A |
| $T_{stg}$ | *storage temperature* | | -55 | | 150 | °C |
| $T_{VJ}$ | *virtual junction temperature* | | -40 | | 150 | °C |
| **Weight** | | | | 5 | | g |
| $F_C$ | *mounting force with clip* | | 20 | | 120 | N |

## Product Marking




## Part number

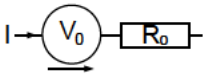
C = Thyristor (SCR)
L = High Efficiency Thyristor
A = (up to 1200V)
50 = Current Rating [A]
E = Single Thyristor
1200 = Reverse Voltage [V]
TC = TO-268AA (D3Pak) (2)

| Ordering | Part Number | Marking on Product | Delivery Mode | Quantity | Code No. |
|---|---|---|---|---|---|
| Standard | CLA50E1200TC | CLA50E1200TC | Tube | 30 | 502708 |

| Similar Part | Package | Voltage class |
|---|---|---|
| CLA50E1200HB | TO-247AD (3) | 1200 |

## Equivalent Circuits for Simulation

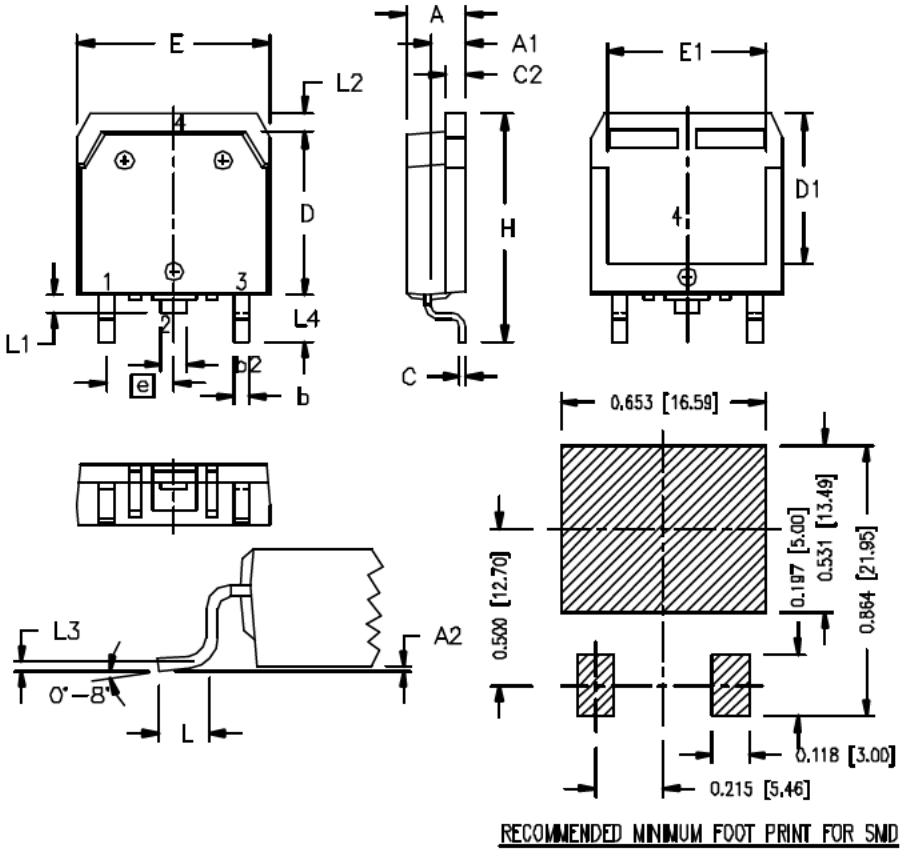
** on die level* $T_{VJ}$ = 150°C



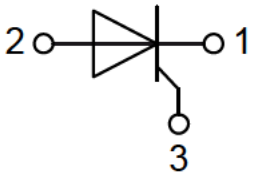

Thyristor

| | | | |
|---|---|---|---|
| $V_{0\,max}$ | *threshold voltage* | 0.88 | V |
| $R_{0\,max}$ | *slope resistance ** | 5.2 | mΩ |

## Outlines TO-268AA (D3Pak)




| Dim. | Millimeter | | Inches | |
|---|---|---|---|---|
| | min | max | min | max |
| A | 4.90 | 5.10 | 0.193 | 0.201 |
| A1 | 2.70 | 2.90 | 0.106 | 0.114 |
| A2 | 0.02 | 0.25 | 0.001 | 0.100 |
| b | 1.15 | 1.45 | 0.045 | 0.057 |
| b2 | 1.90 | 2.10 | 0.075 | 0.083 |
| C | 0.40 | 0.65 | 0.016 | 0.026 |
| C2 | 1.45 | 1.60 | 0.057 | 0.063 |
| D | 13.80 | 14.00 | 0.543 | 0.551 |
| D1 | 12.40 | 12.70 | 0.488 | 0.500 |
| E | 15.85 | 16.05 | 0.624 | 0.632 |
| E1 | 13.30 | 13.60 | 0.524 | 0.535 |
| e | 5.45 BSC | | 0.215 BSC | |
| H | 18.70 | 19.10 | 0.736 | 0.752 |
| L | 2.40 | 2.70 | 0.094 | 0.106 |
| L1 | 1.20 | 1.40 | 0.047 | 0.055 |
| L2 | 1.00 | 1.15 | 0.039 | 0.045 |
| L3 | 0.25 BSC | | 0.100 BSC | |
| L4 | 3.80 | 4.10 | 0.150 | 0.161 |



## Thyristor

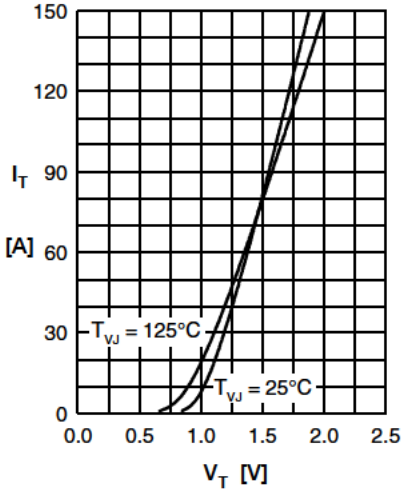



Fig. 1 Forward characteristics

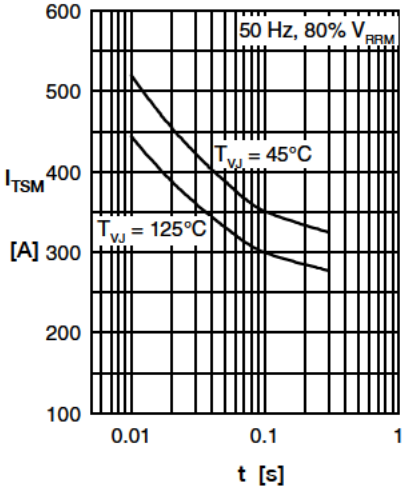



Fig. 2 Surge overload current
$I_{TSM}$: crest value, t: duration

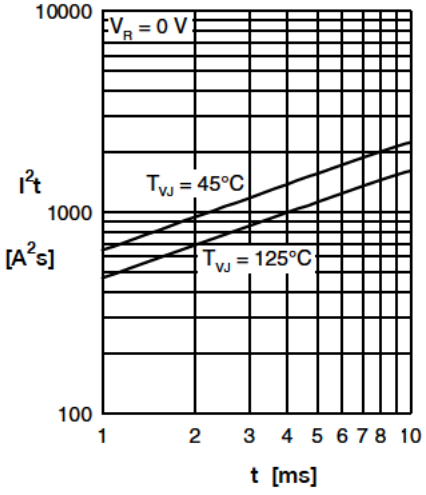



Fig. 3 $I^2t$ versus time (1-10 s)

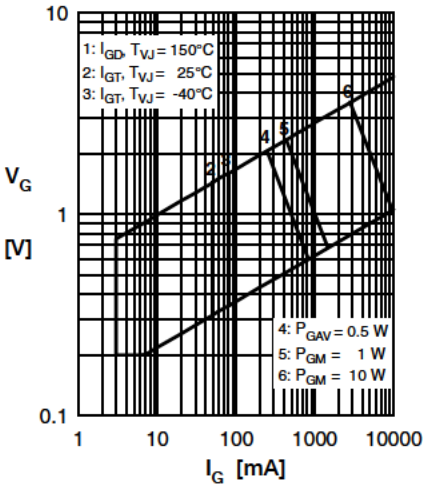



Fig. 4 Gate voltage & gate current

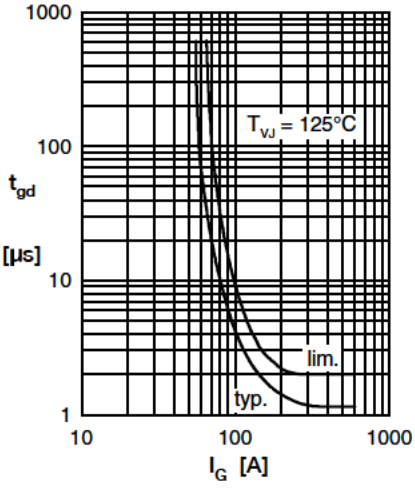



Fig. 5 Gate controlled delay time $t_{gd}$

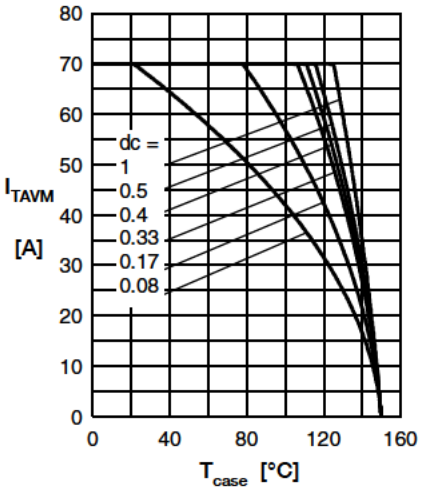



Fig. 6 Max. forward current at case temperature

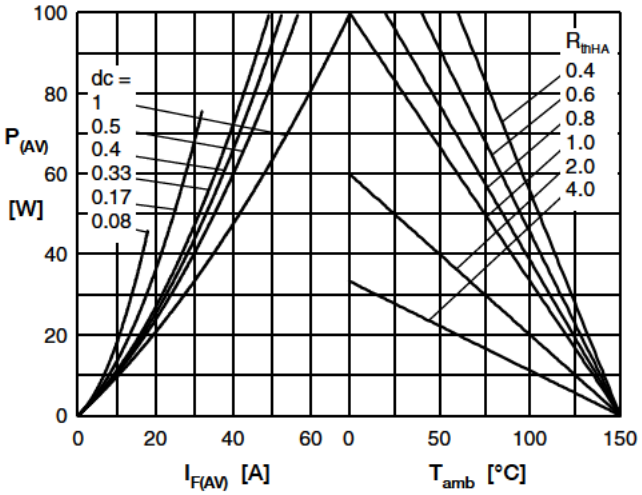
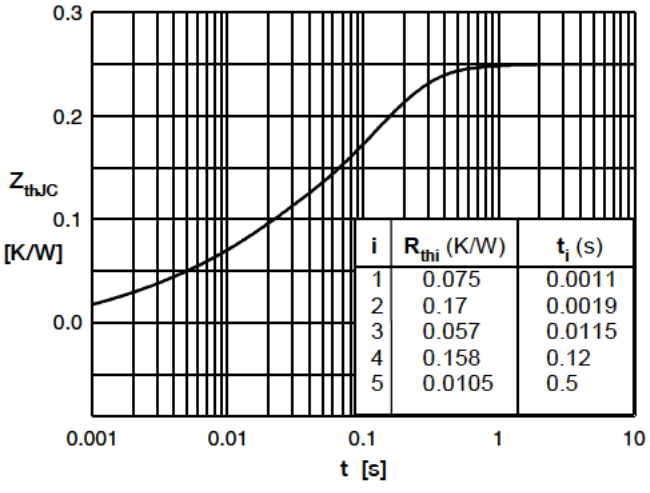



Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature




| i | $R_{thi}$ (K/W) | $t_i$ (s) |
|---|---|---|
| 1 | 0.075 | 0.0011 |
| 2 | 0.17 | 0.0019 |
| 3 | 0.057 | 0.0115 |
| 4 | 0.158 | 0.12 |
| 5 | 0.0105 | 0.5 |

Fig. 7 Transient thermal impedance junction to case