A96F902N

8-Bit Microcontroller

Product Specification

DOC. VERSION 2.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2009/05/27
2.0	1. Deleted ICE652N information and PAGE instruction. 2. Added CPU operation with Green/Idle mode, LCALL/LJMP/TBRD instructions. 3. Proclaimed use ICE660N to simulates A96F902N.	2009/08/25
2.1	Deleted R3 bit5 PS0.	2009/10/09
2.2	Modified ICC1 and ICC2 current	2010/08/13
2.3	ModifiedTable6-8,C1 and C2 value.	2012/03/13
2.4	Added device characteristics	2012/11/22

1 General Description

The A96F902N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology, and high noise immunity. It has an on-chip 2K×13-bit Electrical Flash Memory and 128×8-bit in system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet your requirements.

With its enhanced Flash-ROM feature, the A96F902N can provide a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates with development and programming tools. You can avail yourself of the ELAN Writer to easily program your development code.

2 Features

- **CPU Configuration:**
  - 2K×13 bits Flash memory
  - 144×8 bits on-chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM
    *Endurance: 100,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 2 mA at 5V/4MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during Sleep mode
- **I/O Port Configuration:**
  - 3 bidirectional I/O ports
  - Wake-up port: P6
  - High sink port: P6
  - 12 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 4 programmable open-drain I/O pins
  - External interrupt: P60
- **Operating Voltage Range:**
  - Operating voltage: 2.4V~5.5V at -40°C ~85°C (Industrial)
  - Operating voltage: 2.2V~5.5V ay 0°C ~70°C (Commercial)
- **Operating Frequency Range (base on two clocks):**
  - Crystal mode:
    DC ~ 20 MHz @ 5V
    DC ~ 8 MHz @ 3V
    DC ~ 4 MHz @ 2.2V
  - ERC mode:
    DC ~ 20 MHz @ 5V
    DC ~ 8 MHz @ 3V
    DC ~ 4 MHz @ 2.2V
  - IRC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.2V~5.5V)	Process	Total
1 MHz	±3%	±4%	±2.5%	±9.5%
4 MHz	±3%	±4%	±2.5%	±9.5%
8 MHz	±3%	±5%	±2.5%	±10.5%
16 MHz	±3%	±5%	±2.5%	±10.5%

  - TC2: Timer/Counter/Window
- **One 8-bit Timer/Counter**
  - TC3: Timer/Counter/PDO (programmable divider output) /PWM (pulse width modulation)
- **Two Pairs of OP Amplifier or Comparator (CMP1,2)**
- **One Pair of Comparator (CMP3)**
- **Nine Available Interrupts:**
  - Internal interrupts: 4
  - External interrupts: 5
- 8 **Channels Analog-to-Digital Converter with 10-Bit Resolution**
- **Peripheral Configuration:**
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
  - 4 programmable Level Voltage Reset (LVR): 4.0V, 3.5V, 2.7V, and POR
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - 2/4/8/16 clocks per instruction cycle selected by code option
  - High EFT immunity
  - There are two sub-frequencies; 28kHz and 16kHz. The 16kHz is provided by dividing 128kHz
- **Single Instruction Cycle Commands**
- **Four Crystal Range in Oscillator Mode**

Crystal Range	Oscillator Mode
20 MHz ~ 6 MHz	HXT
6 MHz ~ 1 MHz	XT
1MHz ~ 100kHz	LXT1
32.768kHz	LXT2

- **Programmable Free Running Watchdog Timer**
- **Package Type:**
  - 16-pin DIP 300mil: A96F902ND16
  - 16-pin SOP 300mil: A96F902NSO16
  - 18-pin DIP 300mil: A96F902ND18
  - 18-pin SOP 300mil: A96F902NSO18
  - 20-pin DIP 300 mil: A96F902ND20
  - 20-pin SOP 300mil: A96F902NSO20

NOTE
These are Green Products which do not contain hazardous substances

3 Pin Assignment

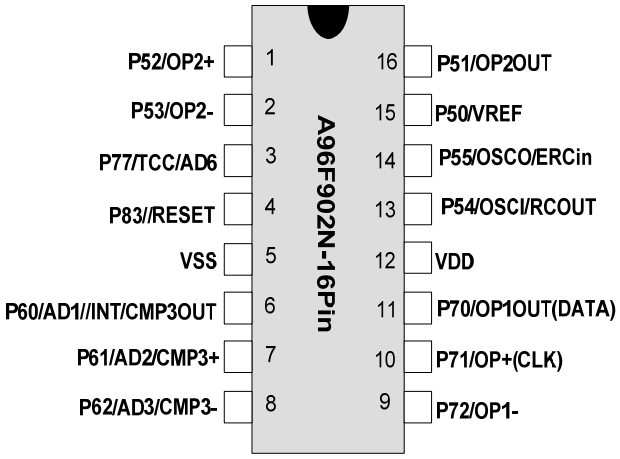


Figure 3-1 A96F902ND16/SO16

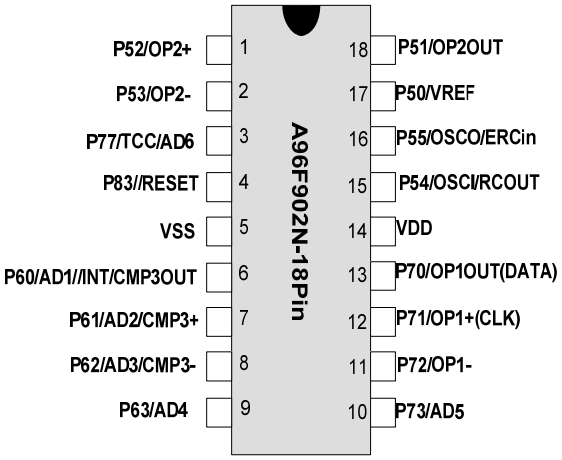


Figure 3-2 A96F902ND18/SO18

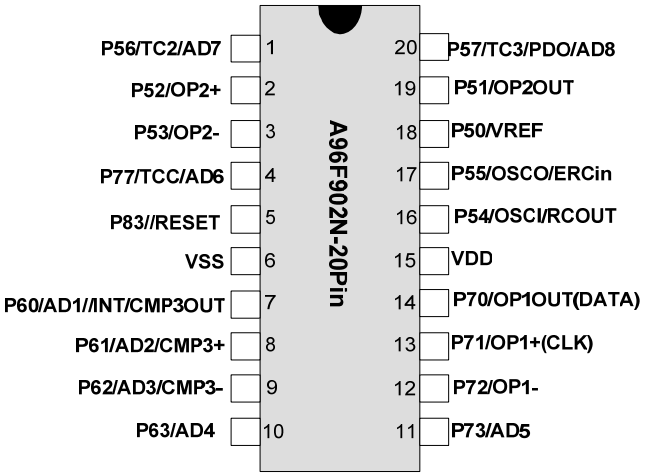


Figure 3-3 A96F902ND20/SO20

4 Pin Description

4.1 A96F902ND16/SO16

Symbol	Pin No.	Type	Function
OSCI/RCOUT	13	I/O	External clock crystal resonator oscillator input pin Clock output from internal RC oscillator
OSCO/ERCin	14	I/O	Clock output from crystal oscillator External RC oscillator clock input pin
TCC	3	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	4	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * */RESET is /RESET pin for Writer programming (Required).* * *For ISP (In System Programming) design rules. Please refer to "EM78F6xxN/5xxN MCU Programming" application notes.*
P50~P51 P52~P53 P54~P55	15, 16 1, 2 13, 14	I/O	Bidirectional 8-bit input/output pins P50~P53 can be used as pull-down pins. P50 can be used as external reference voltage for ADC. P51 can be used as OP2 Amplifier Output. P52 can be used as OP2 Amplifier non-inverting input. P53 can be used as OP Amplifier inverting input.
P60~P62	6~8	I/O	Bidirectional 3-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 4-channel 10-bit resolution A/D converter. P60 can be used as external interrupt.
P70~P72 P77	11~9 3	I/O	P70 ~P72, P77 are bidirectional I/O ports. P70 can be used as OP1 Amplifier Output. P71 can be used as OP1 Amplifier non-inverting input. P72 can be used as OP1 Amplifier inverting input. P77 can be used as 4-channel 10-bit resolution A/D converter P70~P72 can be used as pull-high or pull-down pins. * *P70 is DATA pin for Programming.* * *P71 is CLK pin for Programming.*
P83	4	I/O	P83 is a bidirectional I/O port.
VDD	12	–	Power supply
VSS	5	–	Ground

4.2 A96F902ND18/SO18

Symbol	Pin No.	Type	Function
OSCI/RCOUT	15	I/O	External clock crystal resonator oscillator input pin Clock output from internal RC oscillator
OSCO/ERCin	16	I/O	Clock output from crystal oscillator External RC oscillator clock input pin
TCC	3	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	4	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * */RESET is /RESET pin for Writer programming (Required).* * *For ISP (In System Programming) design rules. Please refer to "EM78F6xxN/5xxN MCU Programming" application notes.*
P50~P51 P52~P53 P54~P55	17, 18 1, 2 15, 16	I/O	Bidirectional 8-bit input/output pins P50~P53 can be used as pull-down pins. P50 can be used as external reference voltage for ADC P51 can be used as OP2 Amplifier Output P52 can be used as OP2 Amplifier non-inverting input P53 can be used as OP Amplifier inverting input
P60~P63	6~9	I/O	Bidirectional 4-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 6-channel 10-bit resolution A/D converter. P60 can be used as external interrupt
P70~P73 P77	13~10 3	I/O	P70 ~P73, P77 are bidirectional I/O ports. P70 can be used as OP1 Amplifier Output. P71 can be used as OP1 Amplifier non-inverting input. P72 can be used as OP1 Amplifier inverting input. P73 and P77 can be used as 6-channel 10-bit resolution A/D converter. P70~P73 can be used as pull-high or pull-down pins. * *P70 is DATA pin for Programming.* * *P71 is CLK pin for Programming.*
P83	4	I/O	P83 is a bidirectional I/O port.
VDD	14	-	Power supply
VSS	5	-	Ground

4.3 A96F902ND20/SO20

Symbol	Pin No.	Type	Function
OSCI/RCOUT	16	I/O	External clock crystal resonator oscillator input pi Clock output from internal RC oscillator.
OSCO/ERCin	17	I/O	Clock output from crystal oscillator External RC oscillator clock input pin
TCC	4	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	5	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * */RESET is /RESET pin for Writer programming (Required).* * *For ISP (In System Programming) design rules. Please refer to "EM78F6xxN/5xxN MCU Programming" application notes.*
P50~P51 P52~P53 P54~P55 P56~P57	18, 19 2, 3 16, 17 1, 20	I/O	Bidirectional 8-bit input/output pins. P50~P53 can be used as pull-down pins. P56~P57 can be used as 8-channel 10-bit resolution A/D converter. P50 can be used as external reference voltage for ADC P51 can be used as OP2 Amplifier Output. P52 can be used as OP2 Amplifier non-inverting input. P53 can be used as OP Amplifier inverting input. P56 can be used as 16-bit timer/counter. P57 can be used as 8-bit timer/counter or programmable divider output (PDO).
P60~P63	7~10	I/O	Bidirectional 5-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 8-channel 10-bit resolution A/D converter. P60 can be used as external interrupt.
P70~P73 P77	14~11 4	I/O	P70 ~P73, P77 are bidirectional I/O ports. P70 can be used as OP1 Amplifier Output. P71 can be used as OP1 Amplifier non-inverting input. P72 can be used as OP1 Amplifier inverting input. P73 and P77 can be used as 8-channel 10-bit resolution A/D converter. P70~P73 can be used as pull-high or pull-down pins. * *P70 is DATA pin for Programming.* * *P71 is CLK pin for Programming.*
P83	5	I/O	P83 is a bidirectional I/O port.
VDD	15	-	Power supply
VSS	6	-	Ground

5 Block Diagram

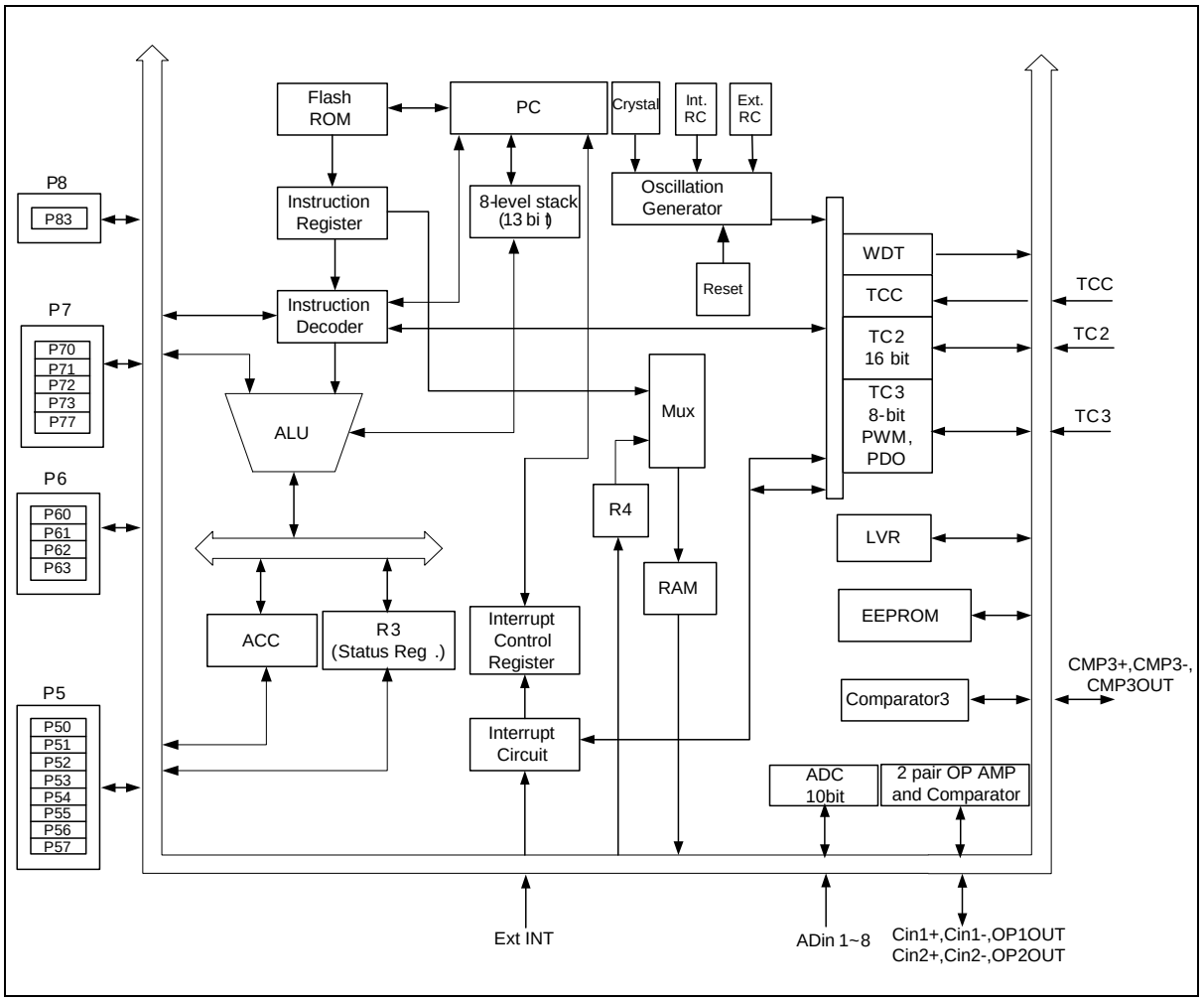


Figure 5-1 A96F902N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC if the PSTE bit (CONT-3) is reset. The contents of the prescaler counter are cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) & Stack

Depending on the device type, R2 and hardware stack are 11-bit wide. The structure is depicted in Figure 6-1 below.

The configuration structure generates 2K×13 bits of on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "**0**"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page (1K).

"CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

"LJMP" instruction allows direct loading of the lower 11 program counter bits. Thus, "LJMP" allows PC to go to any location within 2K.

"LCALL" instruction loads the lower 11 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 2K.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC won't be changed.

Any instruction, except “ADD R2,A;” that is written to R2 (e.g., “MOV R2, A”, “BC R2, 6”) will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8 or fclk/16) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

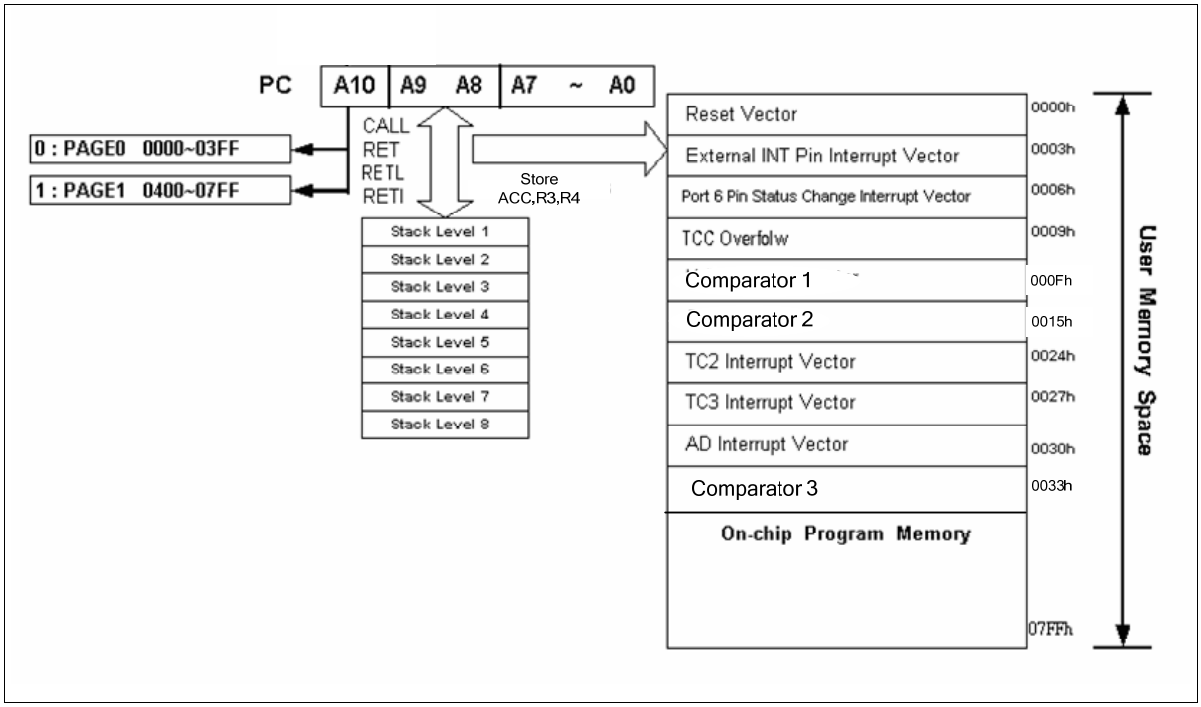


Figure 6-1 Program Counter Organization

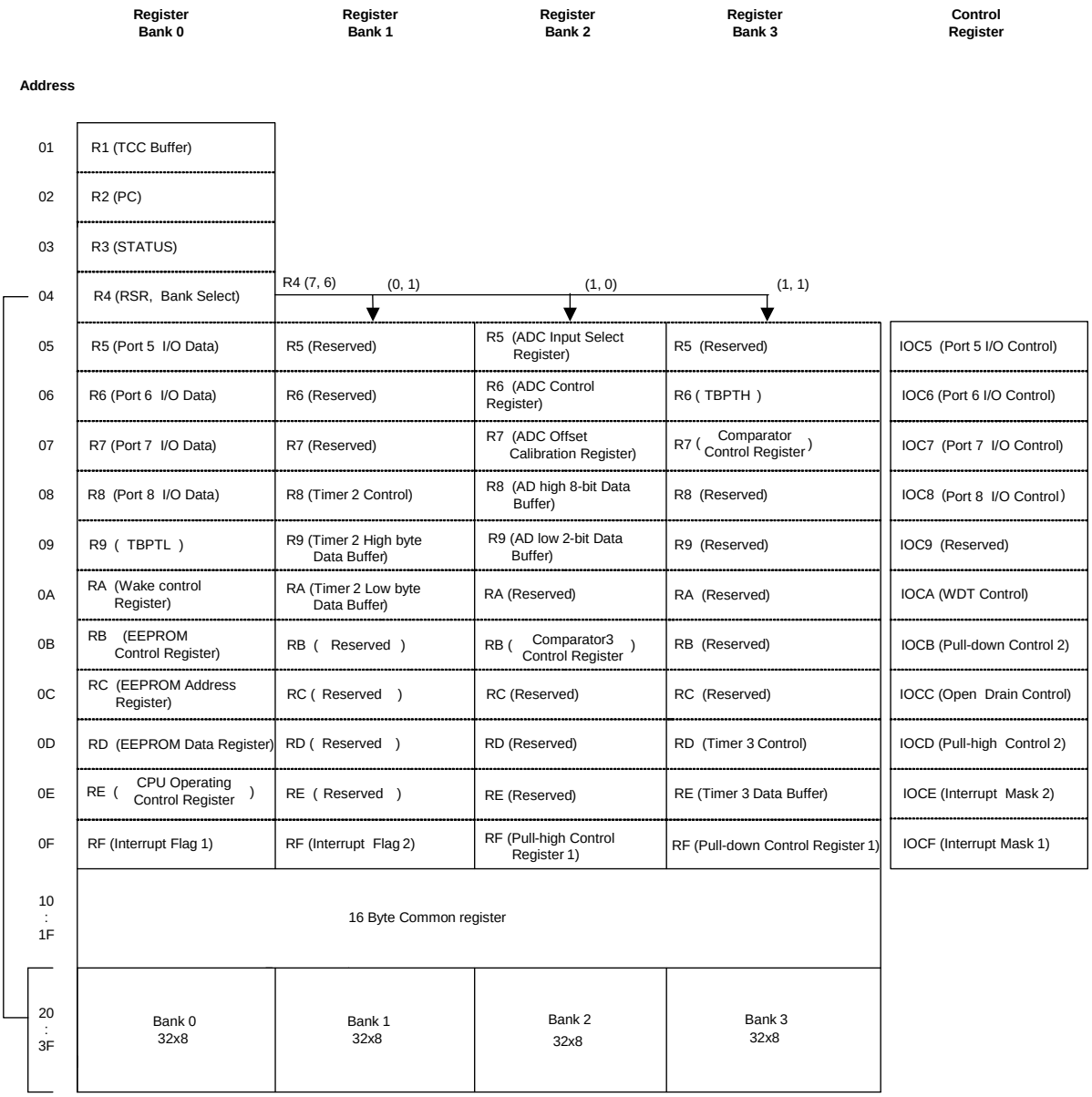


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bit 7 ~ Bit 5: Not used, set to "**0**" at all time

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5~0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2 above.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R7 are I/O registers.

6.1.7 Bank 0 R9 TBPTL (Low Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0

6.1.8 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WE	ICWE	ADWE	EXWE	-	CMP1WE	CMP3WE	-

Bit 7 (CMP2WE): Comparator 2 wake-up enable bit

0: Disable Comparator 2 wake-up

1: Enable Comparator 2 wake-up

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up

1: Enable ADC wake-up

When ADC completed status is used to enter the interrupt vector or to wake up the A96F902N from Sleep, with A/D conversion running, the ADWE bit must be set to "Enable".

Bit 4 (EXWE): External wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

Bit 2 (CMP1WE): Comparator 1 wake-up enable bit

0: Disable Comparator 1 wake-up

1: Enable Comparator 1 wake-up

Bit 1 (CMP3WE): Comparator 3 wake-up enable bit

0: Disable Comparator 3 wake-up

1: Enable Comparator 3 wake-up

Bits 3, 0: Not used, set to "**0**" at all time

6.1.9 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM content (RD can be set by software, RD is cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software. WR is cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit

0: Write to EEPROM is prohibited.

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM detect flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating.

Bits 2 ~ 0: Not used, set to "**0**" at all time

6.1.10 Bank 0 RC (EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 6 ~ 0: EEPROM address

6.1.11 Bank 0 RD (EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: EEPROM data

6.1.12 Bank 0 RE (CPU Operating Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE-	-			

Bit 7: Not used, set to "**0**" at all time

Bit 6 (TIMERSC): TCC, TC2, TC3 clock source select

0: Fs. Fs**:** sub frequency for WDT internal RC time base

1: Fm. Fm**:** main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0: S ub-oscillator (fs)

1: M ain oscillator (fosc)

When CPUS=0, the CPU oscillator will select the sub-oscillator and the **main oscillator is stopped.**

Bit 4 (IDLE): Idle Mode Enable Bit. This bit decides the Idle mode status under SLEP instruction.

0: IDLE="**0**"+SLEP instruction → Sleep mode

1: IDLE="**1**"+SLEP instruction → Idle mode

■ **CPU Operation Mode**

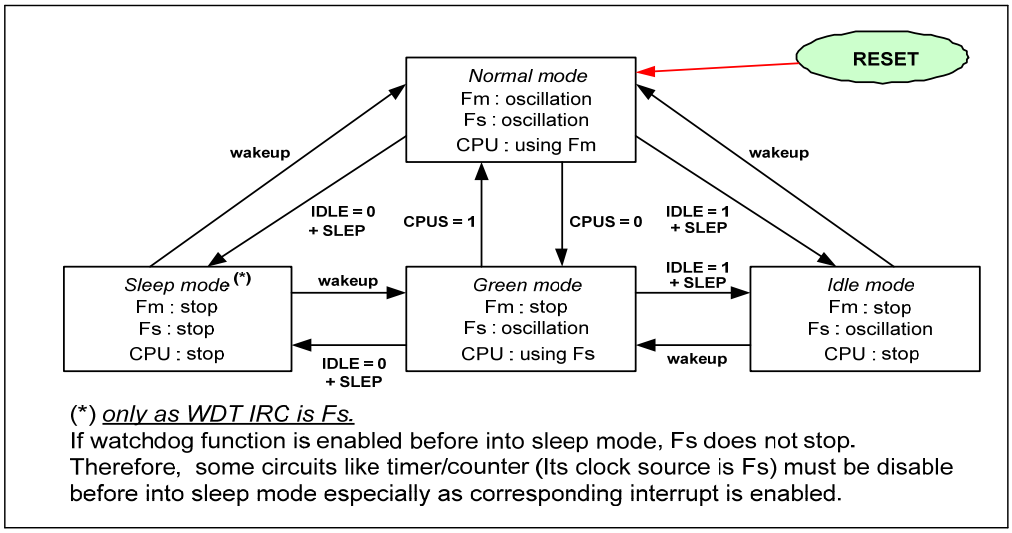


Figure 6-3 CPU Operation Mode

Bits 3 ~ 0: Not used, set to "**0**" at all time

6.1.13 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF3	ADIF	-	-	-	EXIF	ICIF	TCIF

***NOTE:** "**1**" means with interrupt request "**0**" means no interrupt occurs*

Bit 7 (CMPIF3): Comparator 3 Interrupt Flag. Set when a change occurs in the Comparator 3 output. Reset by software.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5~3: Not used, set to "**0**" at all time

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

Bank 0 RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE
The result of reading Bank 0 RF is the "logic AND" of Bank 0 RF and IOCF.

6.1.14 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.1.15 Bank 1 R5 ~R7

Reserved registers

6.1.16 Bank 1 R8 TC2CR (Timer 2 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bit 7 and Bit 6 (RCM1, RCM0): IRC mode select bits

Writer Trim IRC	Bank1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4MHz	**0**	**0**	4MHz±2.5%	2.2V~5.5V	<5µs
	0	**1**	16MHz±10%	4.5V~5.5V	<1.5µs
	1	**0**	8MHz±10%	3.0V~5.5V	<3µs
	1	**1**	1MHz±10%	2.2V~5.5V	<22µs
16MHz	**0**	**0**	4MHz±10%	2.2V~5.5V	<6µs
	0	**1**	16MHz±2.5%	4.5V~5.5V	<1.25µs
	1	**0**	8MHz±10%	3.0V~5.5V	<3µs
	1	**1**	1MHz±10%	2.2V~5.5V	<22µs
8MHz	**0**	**0**	4MHz±10%	2.2V~5.5V	<6µs
	0	**1**	16MHz±10%	4.5V~5.5V	<1.5µs
	1	**0**	8MHz±2.5%	3.0V~5.5V	<2.5µs
	1	**1**	1MHz±10%	2.2V~5.5V	<22µs
1MHz	**0**	**0**	4MHz±10%	2.2V~5.5V	<6µs
	0	**1**	16MHz±10%	4.5V~5.5V	<1.5µs
	1	**0**	8MHz±10%	3.0V~5.5V	<3µs
	1	**1**	1MHz±2.5%	2.2V~5.5V	<20µs

NOTE

- *BANK1 R8<7,6> of the initialized values are kept the same as WORD 1<3,2>.*
- *After A Frequency switches to B Frequency, F902N needs to hold some stable time on B frequency.*

  ***Ex:** Writer trim IRC 4MHz → BANK1 R8<7,6> set to "10" → holds 3 µs → F902N works on 8MHz ± 10%.*

Code option Word 1 COBS=0**:**

The R8<7,6> of the initialized values will remain the same as Word 1<3,2>.

The R8<7,6> cannot change frequency.

Code option Word 1 COBS=1**:**

The R8<7,6> of the initialized values will remain the same Word as 1<3,2>.

The R8<7,6> can change when user wants to work on other IRC frequency.

Bit 5 (TC2ES): TC2 signal edge

0: Incremented if a transition from low to high (rising edge) takes place on the TC2 pin

1: Incremented if a transition from high to low (falling edge) takes place on the TC2 pin

Bit 4 (TC2M): Timer/Counter 2 mode select

0: Timer/counter mode

1: Window mode

Bit 3 (TC2S): Timer/Counter 2 start control

0: Stop and counter cleared

1: Start

Bit 2~Bit 0 (TC2CK2~TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{23}$	1.05 sec	19.1 hr
0	0	1	$Fc/2^{13}$	1.02 ms	1.1 min
0	1	0	$Fc/2^{8}$	32µs	2.1 sec
0	1	1	$Fc/2^{3}$	1µs	65.5 ms
1	0	0	Fc	125ns	7.9 ms
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	External clock (TC2 pin)	–	–

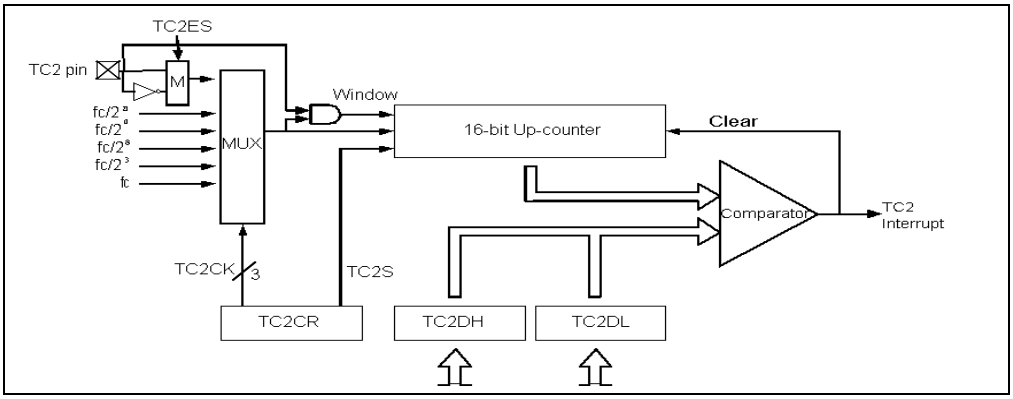


Figure 6-4 Timer / Counter 2 Configuration

In Timer mode, counting up is performed using internal clock. When the contents of the up-counter are matched by TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

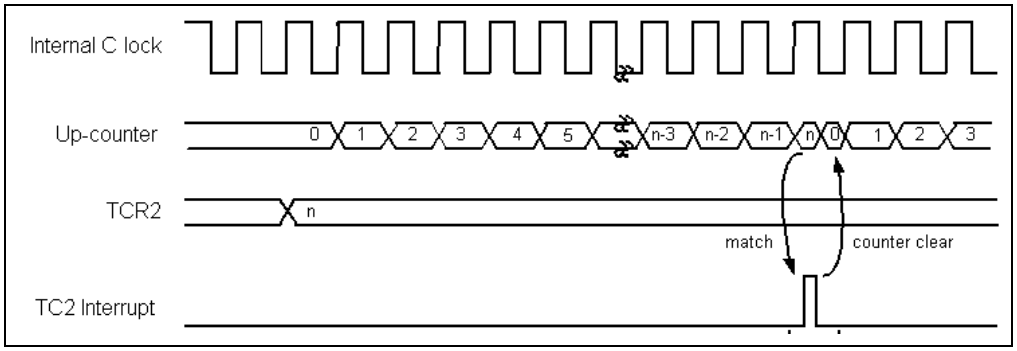


Figure 6-5 Timer Mode Timing Diagram

In Counter mode, counting up is performed using the external clock input pin (TC2 pin) and either rising or falling can be selected by setting TC2ES. When the contents of up-counter are matched by TCR2 (TCR2H+TCR2L), then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

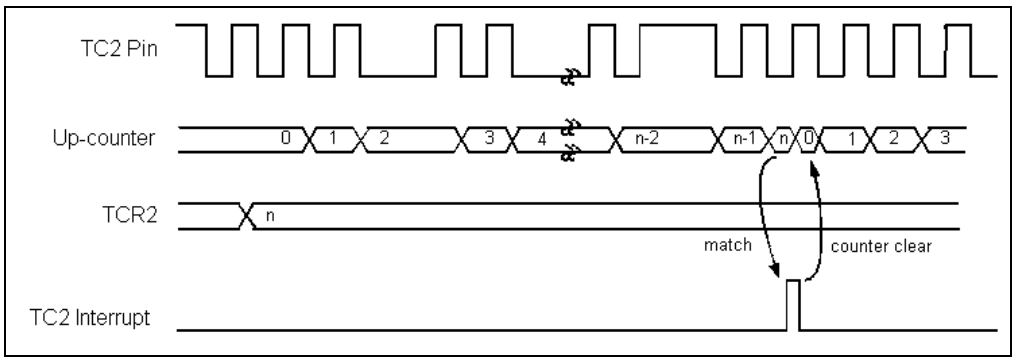


Figure 6-6 Counter Mode Timing Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter are matched by TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

NOTE
When writing to the TCR2L, the comparison is inhibited until TCR2H is written.

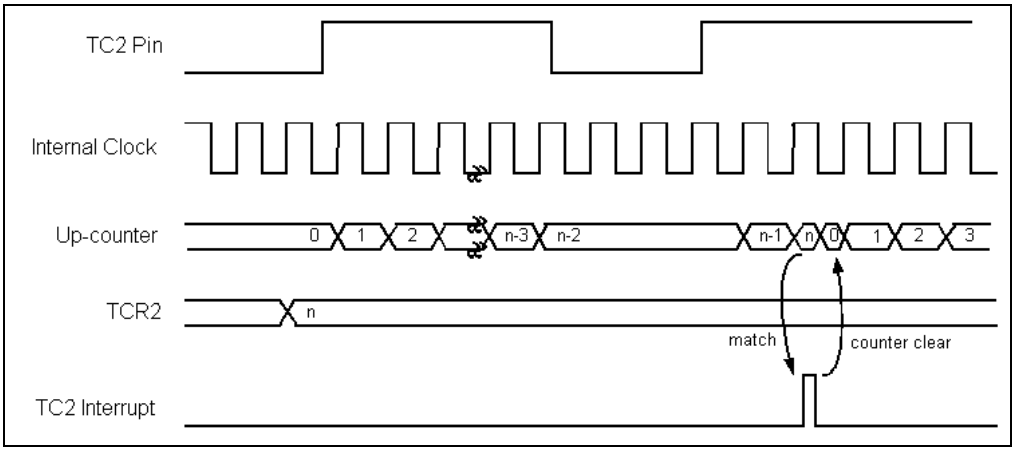


Figure 6-7 Window Mode Timing Diagram

6.1.17 Bank 1 R9 TC2DH (Timer 2 High Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TC2D8 ~ TC2D15): High byte data buffer of 16-bit Timer/Counter 2.

6.1.18 Bank 1 RA TC2DL (Timer 2 Low Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0): Low byte data buffer of 16-bit Timer/Counter 2.

6.1.19 Bank 1 RB ~RE

These are reserved registers.

6.1.20 Bank 1 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF2	CMPIF1	TCIF3	TCIF2	-	-	-	-

***NOTE:** "**1**" means with interrupt request "**0**" means no interrupt occurs*

Bits 7~6 (CMPIFx): Comparator interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 5 (TCIF3): 8-bit Timer/Counter 3 interrupt flag. Interrupt flag is cleared by software.

Bit 4 (TCIF2): 16-bit Timer/Counter 2 interrupt flag. Interrupt flag is cleared by software.

Bits 3~0: Not used, set to "**0**" at all time

Bank 1RF can be cleared by instruction but cannot be set.
IOCE is the interrupt mask register.

NOTE
The result of reading Bank 1 RF is the "logic AND" of Bank 1 RF and IOCE.

6.1.21 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register for ADC pins functions as analog input or digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE8	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1

Bit 7 (ADE8): AD converter enable bit of P57 pin

0: Disable ADC8, P57 functions as I/O pin

1: Enable ADC8 to function as analog input pin

Bit 6 (ADE7): AD converter enable bit of P56 pin.

0: Disable ADC7, P56 functions as I/O pin

1: Enable ADC7 to function as analog input pin

Bit 5 (ADE6): AD converter enable bit of P77 pin

0: Disable ADC6, P77 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 4 (ADE5): AD converter enable bit of P73 pin

0: Disable ADC5, P73 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 3 (ADE4): AD converter enable bit of P63 pin

0: Disable ADC4, P63 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 2 (ADE3): AD converter enable bit of P62 pin

0: Disable ADC3, P62 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 1 (ADE2): AD converter enable bit of P61 pin

0: Disable ADC2, P61 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 0 (ADE1): AD converter enable bit of P60 pin

0: Disable ADC1, P60 functions as I/O pin

1: Enable ADC1 to function as analog input pin

The following table shows the priority of P60/AD1//INT/CMP3OUT.

P60/AD1//INT/CMP3OUT Pin Priority			
Hight	Medium	Medium	Low
/INT	CMP3OUT	AD1	P60

6.1.22 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC.

0: Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The oscillator clock rate of ADC

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
01	F_{OSC}	1 MHz
10	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0: Reset upon completion of AD conversion. This bit cannot be reset by software.

1: A/D conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating

1: ADC is operating

Bits 2~0 (ADIS2~ADIS0): AD Input Select Bits

ADIS2	ADIS1	ADIS0	AD Input Pin
0	**0**	**0**	AD1
0	**0**	**1**	AD2
0	**1**	**0**	AD3
0	**1**	**1**	AD4
1	**0**	**0**	AD5
1	**0**	**1**	AD6
1	**1**	**0**	AD7
1	**1**	**1**	AD8

6.1.23 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	OPADEN	OPADS

Bit 7 (CALI): Calibration enable bit for A/D offset

0: Calibration disable

1: Calibration enable

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	Offset
0	**0**	**0**	0LSB
0	**0**	**1**	1LSB
0	**1**	**0**	2LSB
0	**1**	**1**	3LSB
1	**0**	**0**	4LSB
1	**0**	**1**	5LSB
1	**1**	**0**	6LSB
1	**1**	**1**	7LSB

Bit 2: Not used, set to "**0**" at all time

Bit 1 (OPADEN): OPOUT connects to ADC Enable bit

0: ADC is not dedicated to OP output.

1: ADC is dedicated to OP output.

OPADEN	ADIS2	ADIS1	ADIS0	AD Input Select
1	×	×	×	OPx output
0	×	×	×	ADx

Bit 0 (OPADS): OPOUT connects to ADC select

0: OP1 output connects to AD.

1: OP2 output connects to AD.

6.1.24 Bank 2 R8 ADDH (AD High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2

When the A/D conversion is completed, the result of high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.25 Bank 2 R9 ADDL (AD Low 2-Bit Data Buffer)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	ADD1	ADD0

Bits 7 ~ 2: Not used, set to "**0**" at all time

6.1.26 Bank 2 RA, RC ~RE

Reserved registers

6.1.27 Bank 2 RB CMP3CON (Comparator 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CP3OUT	CP3S1	CP3S0

Bits 7 ~ 3: Not used. Set to "**0**" at all time.

Bit 2 (CP3OUT): The result of the Comparator 3 output

NOTE

The P60/AD1/INT/CMP3OUT pin priority is as follows:

Priority			
High	Medium	Medium	Low
INT	CMP3OUT	AD1	P60

Bit 1 ~ Bit 0 (CP3S1 ~ CP3S0): Comparator 3 Select bits

CO3S1	CO3S0	Function Description
0	0	Comparator 3 is not used. P60 functions as normal I/O pin.
0	1	Used as Comparator 3 and P60 functions as normal I/O pin
1	0	Used as Comparator 3 and P60 funcions as Comparator 3 output pin (CMP3OUT)
1	1	Reserved

NOTE

The P61/AD2/CMP3+ pin priority is as follows:

Priority		
High	Medium	Low
CMP3+	AD2	P61

NOTE

The P62/AD3/CMP3- pin priority is as follows:

Priority		
High	Medium	Low
CMP3-	AD3	P62

6.1.28 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PH73	/PH72	/PH71	/PH70

Bits 7 ~ 4: Not used, set to "**0**" at all time.

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin.

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin.

Bit 0 (/PH70): Control bit used to enable pull-high the P70 pin.

The RF Register is both readable and writable.

6.1.29 Bank 3 R5

Reserved Register

6.1.30 Bank 3 R6 TBPTH (High Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	RBit 10	RBit 9	RBit 8

Bit 7 (MLB): Take MSB or LSB at machine code

Bits 6 ~ 3: Not used. Set "**0**" at all time.

Bits 2 ~ 0: Table pointer address Bits 10~8

6.1.31 Bank 3 R7 CMPCON (Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP1OUT	CO1S1	CO1S0	CP2OUT	CO2S1	CO2S0	-	-

Bit 7 (CP1OUT): The result of the comparator1 output

Bit 6 ~ Bit 5 (CO1S1 ~ CO1S0): Comparator 1 / OP1 Select bits

CO1S1	CO1S0	Function Description
0	**0**	Comparator 1 and OP1 are not used. P70 functions as normal I/O pin.
0	**1**	Used as Comparator 1. P70 functions as normal I/O pin
1	**0**	Used as Comparator 1. P70 funcions as Comparator 1 output pin (OP1OUT)
1	**1**	Used as OP1. P70 functions as OP1 output pin (OP1OUT)

Bit 4 (CP2OUT): The result of the Comparator 2 output

Bit 3 ~ Bit 2 (CO2S1 ~ CO2S0): Comparator 2 / OP2 Select bits

CO2S1	CO2S0	Function Description
0	0	Comparator 2 and OP2 are not used. P51 functions as normal I/O pin.
0	1	Used as Comparator 2 and P51 functions as normal I/O pin.
1	0	Used as Comparator 2 and P51 funcions as Comparator 2 output pin (OP2OUT)
1	1	Used as OP2 and P51 functions as OP2 output pin (OP2OUT)

Bits 1 ~ 0: No used. Set "**0**" at all time.

6.1.32 Bank 3 R8~RC

Reserved Registers

6.1.33 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bit 7 ~ Bit 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear the counter

1: Start

Bit 4 ~ Bit 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{11}$	250 µs	64 ms
0	0	1	$Fc/2^{7}$	16 µs	4 ms
0	1	0	$Fc/2^{5}$	4 µs	1 ms
0	1	1	$Fc/2^{3}$	1 µs	255 µs
1	0	0	$Fc/2^{2}$	500 ns	127.5 µs
1	0	1	$Fc/2^{1}$	250 ns	63.8 µs
1	1	0	Fc	125 ns	31.9 µs
1	1	1	External clock (TC3 pin)	-	-

Bit 1 ~ Bit 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	**0**	Timer/Counter
0	**1**	Reserved
1	**0**	Programmable Divider output
1	**1**	Pulse Width Modulation output

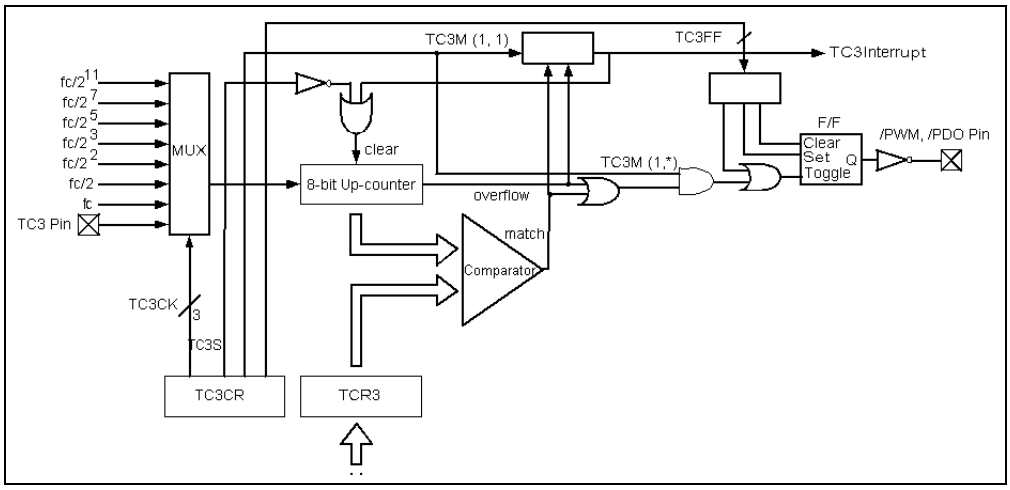


Figure 6-8 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match with TCR3, the interrupt are then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using external clock input pin (TC3 pin). When the contents of the up-counter match with TCR3, the interrupt are then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. The F/F can be initialized by the program and it is initialized to "**0**" during reset. A TC3 interrupt is generated each time the /PDO output is toggled.

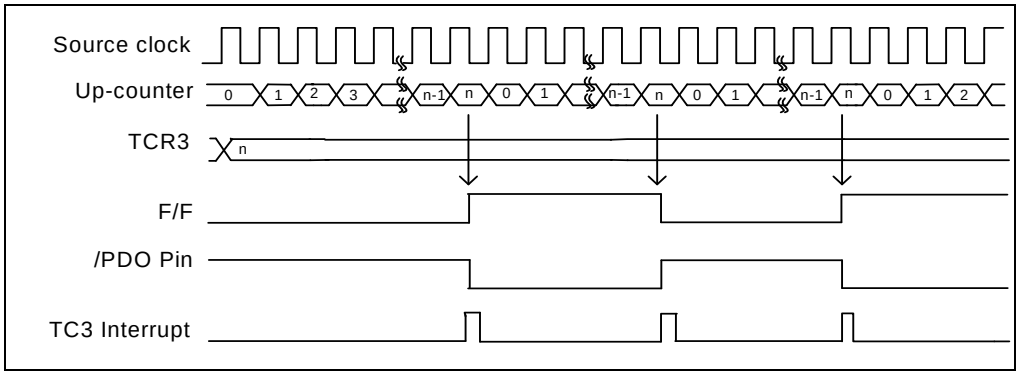


Figure 6-9 PDO Mode Timing Diagram

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. Then the counter continues counting, and the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. TCR3 is configured as a 2-stage shift register and, during output; will not switch until one output cycle is completed even if TCR3 is overwritten. Therefore, the output can be changed continuously. Also, the TRC3 is shifted for the first time by setting TC3S to "**1**" after data is loaded to TCR3.

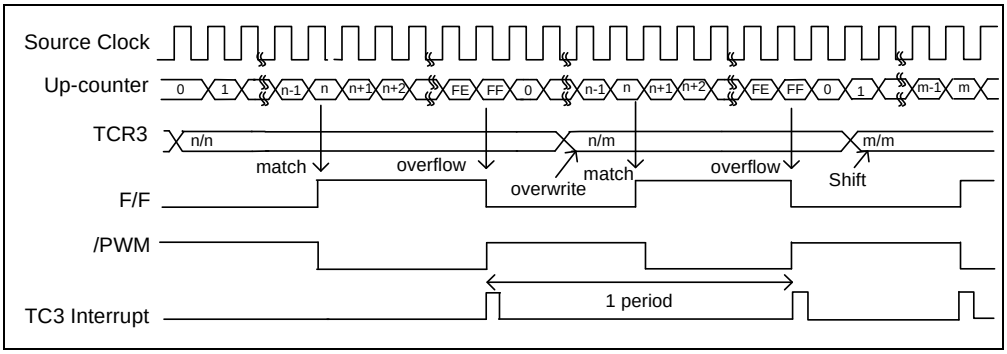


Figure 6-10 PWM Mode Timing Chart

6.1.34 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bit 7 ~ Bit 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.35 Bank 3 RF (Pull-down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PD73	/PD72	/PD71	/PD70

Bit 7~ Bit 4: Not used, set to "**0**" at all time

Bit 3 (/PD73): Control bit used to enable the P73 pull-down pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 2 (/PD72): Control bit used to enable the P72 pull-down pin

Bit 1 (/PD71): Control bit used to enable the P71 pull-down pin

Bit 0 (/PD70): Control bit used to enable the P70 pull-down pin

The RF Register is both readable and writable.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at the rising edge of the INT pin

1: Interrupt occurs at the falling edge of the INT pin

Bit 6 (/INT): Interrupt enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on TCC pin

Bit 4 (TE): TCC signal edge

0: Increment if a transition from low to high takes place on TCC pin

1: Increment if a transition from high to low takes place on TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit, TCC rate is 1**:**1

1: Prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	**0**	**0**	1:2
0	**0**	**1**	1:4
0	**1**	**0**	1:8
0	**1**	**1**	1:16
1	**0**	**0**	1:32
1	**0**	**1**	1:64
1	**1**	**0**	1:128
1	**1**	**1**	1:256

CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC8 (I/O Port Control Register)

A value of "**1**" sets the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output.

IOC5, IOC6, IOC7, and IOC8 registers are both readable and writable.

6.2.4 IOC9

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**".

When EIS is "**0**", the path of /INT is masked. When EIS is "**1**", the status of /INT pin can also be read by reading Port 6 (R6).

EIS is both readable and writable.

Bits 5~4: Not used, set to "**0**" at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit, WDT rate is 1:1.

1: Prescaler enable bit, WDT rate is set as Bit 0~Bit 2.

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	**0**	**0**	1:2
0	**0**	**1**	1:4
0	**1**	**0**	1:8
0	**1**	**1**	1:16
1	**0**	**0**	1:32
1	**0**	**1**	1:64
1	**1**	**0**	1:128
1	**1**	**1**	1:256

6.2.6 IOCB (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 7 (/PD7): Control bit used to enable pull-down of the of P63 pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable pull-down of the P62 pin

Bit 5 (/PD5): Control bit used to enable pull-down of the P61 pin

Bit 4 (/PD4): Control bit used to enable pull-down of the P60 pin

Bit 3 (/PD3): Control bit used to enable pull-down of the P53 pin

Bit 2 (/PD2): Control bit used to enable pull-down of the P52 pin

Bit 1 (/PD1): Control bit used to enable pull-down of the P51 pin

Bit 0 (/PD0): Control bit used to enable pull-down of the P50 pin

The IOCB Register is both readable and writable.

6.2.7 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	OD3	OD2	OD1	OD0

Bits 7 ~ 4: Not used, set to "**0**" at all time

Bit 3 (OD3): Control bit used to enable the open-drain output of P63 pin

0: Disable open-drain output

1: Enable open-drain output

Bit 2 (OD2): Control bit used to enable the open-drain output of P62 pin

Bit 1 (OD1): Control bit used to enable the open-drain output of P61 pin

Bit 0 (OD0): Control bit used to enable the open-drain output of P60 pin

The IOCC Register is both readable and writable.

6.2.8 IOCD (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	/PH3	/PH2	/PH1	/PH0

Bits 7~4: Not used, set to "**0**" at all time

Bit 3 (/PH3): Control bit used to enable pull-high of the P63 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 2 (/PH2): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH1): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH0): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE2	CMPIE1	TCIE3	TCIE2	–	–	–	–

Bits 7~6 (CMPIEx): Interrupt enable bit

0: Disable CMPIFx interrupt

1: Enable CMPIFx interrupt

When the Comparator Output Status Changed is used to enter an interrupt vector or enter the next instruction, the CMPIEx bit must be set to “Enable”.

Bit 5 (TCIE3): Interrupt enable bit

0: Disable TCIF3 interrupt

1: Enable TCIF3 interrupt

Bit 4 (TCIE2): Interrupt enable bit

0: Disable TCIF2 interrupt

1: Enable TCIF2 interrupt

Bits 3 ~ 0: Not used, set to “**0**” at all time

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE3	ADIE	–	–	–	EXIE	ICIE	TCIE

Bit 7 (CMPIE3): Interrupt enable bit

0: Disable CMPIF3 interrupt

1: Enable CMPIF3 interrupt

Bit 6 (ADIE): ADIF interrupt enable bit

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When the ADC Complete is used to enter an interrupt vector or the next instruction, the ADIE bit must be set to “Enable“.

Bits 5 ~ 3: Not used, set to “**0**” at all time

Bit 2 (EXIE): EXIF interrupt enable bit
0: Disable EXIF interrupt
1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit
0: Disable ICIF interrupt
1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit
0: Disable TCIF interrupt
1: Enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler. Likewise, the PSW0~PSW2 bits of the IOCA register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the “WDTC” and “SLEP” instructions. Figure 6-11 below depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). As illustrated in Figure 6-11, selection of Fc depends on the Bank 0 RE.6 <TIMERSC>. If TCC signal source is from external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (kept in High or Low level) must be greater than 1CLK. The TCC will stop running when Sleep mode occurs.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCA register. With no prescaler, the WDT time-out period is approximately 18ms[1] (one oscillator start-up timer period).

[1] *VDD=5V, WDT time-out period = 16.5ms ± 5%*
VDD=3V, WDT time-out period = 18ms ± 5%.

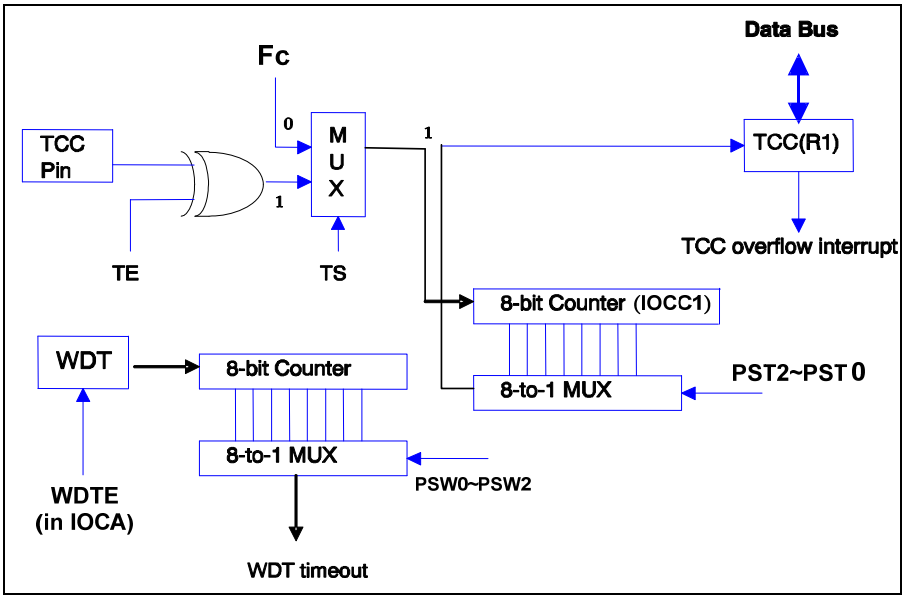
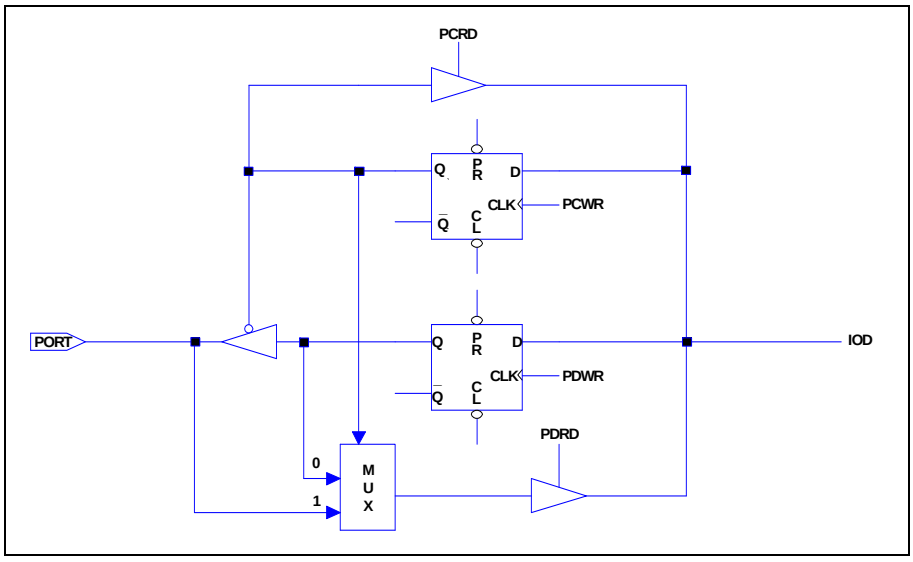


Figure 6-11 TCC and WDT Block Diagram

6.4 I/O Ports

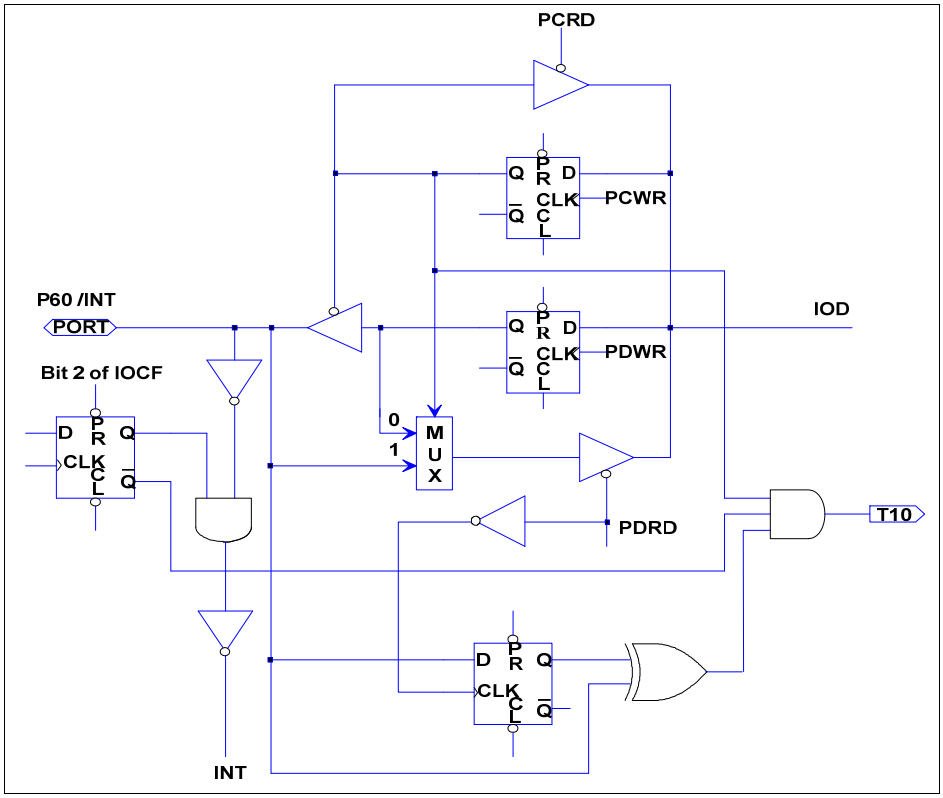
The I/O registers, Ports 5, 6, 7 and 8, are bidirectional tri-state I/O ports. Port 6 / 7 can be pulled high internally by software. In addition, Port 6 can also be set as open-drain output by software. Input status change interrupt (or Wake-up) function on Port 6 P50 ~ P53 and P60 ~ P63 and Port 7 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, Port 7 and Port 8 are shown in the following circuit diagrams (Figures 6-12, 6-13 (a), 6-13 (b), and Figure 6-14) below.



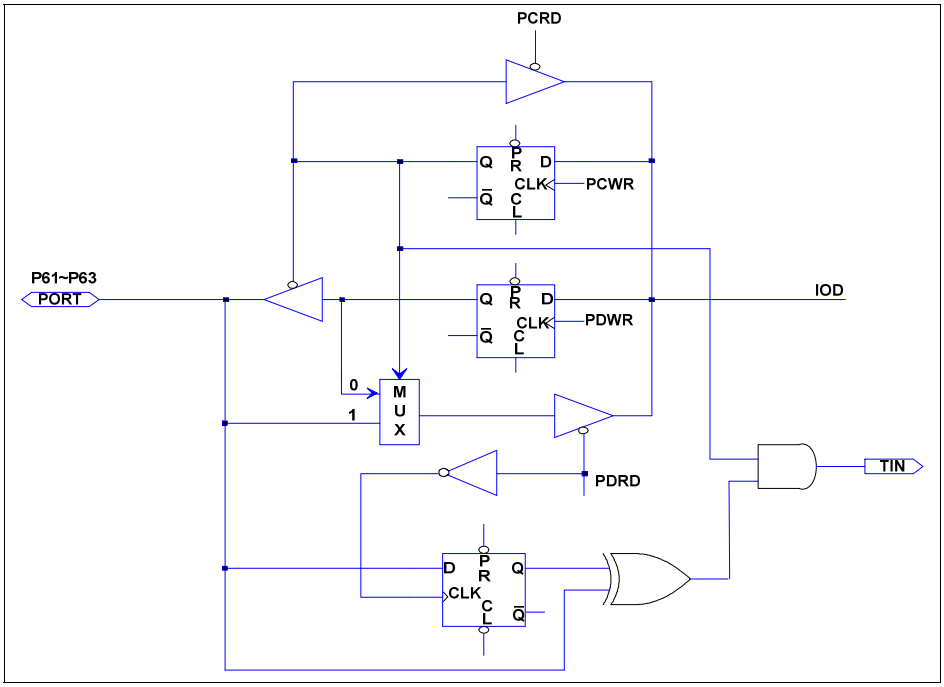
NOTE: *Pull-down not shown in the figure.*

Figure 6-12 I/O Port and I/O Control Register Circuit for Ports 5, 6, 7



NOTE: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-13(a) I/O Port and I/O Control Register Circuit for P60 (/INT)



NOTE: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-13(b) I/O Port and I/O Control Register Circuit for P61~P63,P83

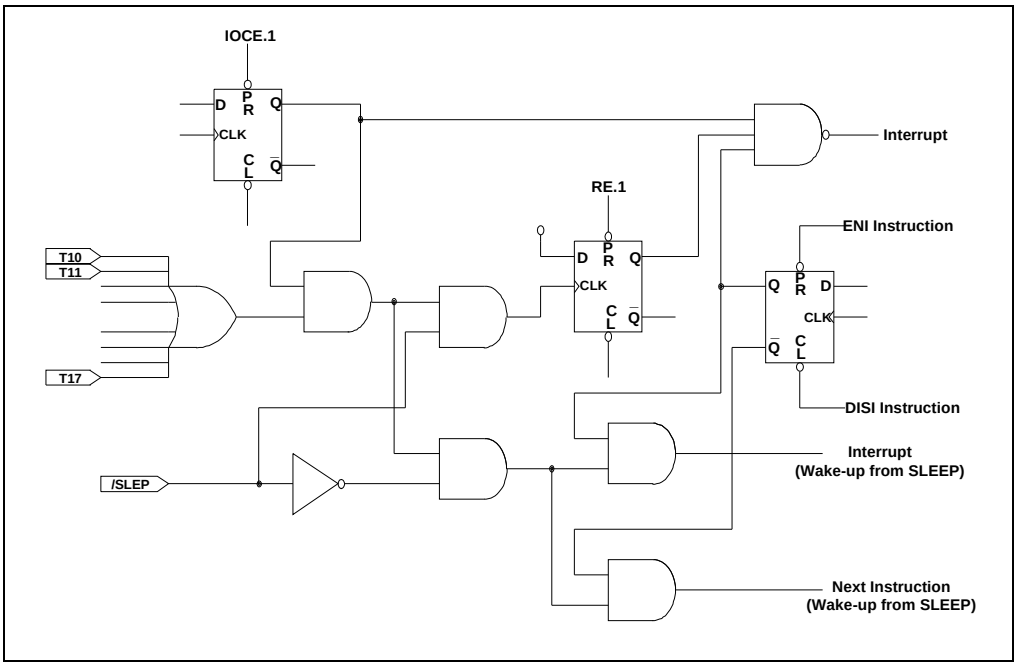


Figure 6-14 I/O Port 6 with Input Change Interrupt/Wake-up Block Diagram

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

1. Wake-up Input Status Change	2. Interrupt Input Status Change
a) Before Sleep: 1) Disable WDT[2] (use this very carefully) 2) Read I/O Port 6 (MOV R6,R6) 3a) Enable interrupt (Set IOCF=1) after wake-up. If "ENI," switched to interrupt vector (006H). If "DISI" excute next instruction. 3b) Disable interrupt (Set IOCF=1). Always execute next instruction 4) Enable wake-up bit (Set RA=6) 5) Execute "SLEP" instruction **b) After Wake-up:** 1) IF "ENI" → Interrupt vector (006H) 2) IF "DISI" → Next instruction	1) Read I/O Port 6 (MOV R6,R6) 2) Execute "ENI" 3) Enable interrupt (Set IOCF=1) 4) IF Port 6 change (interrupt) → Interrupt vector (006H)

[2] *Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-up function (Code Option Register Word 0 Bit 6 (ENWDTB) is set to "1").*

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18ms[3] (one oscillator start-up timer period) after the reset is detected. Once a reset occurs, the following functions are performed. Refer to Figure 6-15 below.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD, RD, RE registers are set to their previous status.
- The bits of the CONT register are set to all "**0**" except for Bit 6 (INT flag).
- Bank 0 RF, IOCF registers are cleared.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, the WDT (if enabled) is cleared but keeps on running. Wake-up is then generated. In RC mode, the wake-up time is 34 clocks, in High Crystal mode wake-up time is 2ms and 32 clocks, and in Low Crystal 2 mode, wake-up time is 500ms.

The controller can be awakened by:

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 6 input status changes (if enabled)
4) External (P60, /INT) pin changes (if EXWE is enabled)
5) A/D conversion completed (if ADWE is enabled)
6) Comparator output status change (if CMPxWE is enabled)

[3] *Vdd = 5V, set up time period = 16.8ms ± 8%*
Vdd = 3V, set up time period = 18ms ± 8%

The first two events (1 & 2) will cause the A96F902N to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). Events 3, 4, and 5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x3, 0x6 0xF, 0x15 or 0X30, after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after Wake-up. All throughout the Sleep mode, the Wake-up time is150µs, no matter what oscillation mode is (except low Crystal mode). In Low Crystal 2 mode, the Wake-up time is 500ms.

One or more of the above Events 3 to 6 may be enabled before entering into Sleep mode but is awakened only by one of the events.

a) If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the A96F902N can be awakened only by Event 1 or 2. Refer to Section 6.6 *Interrupt* for further details.

b) If Port 6 Input Status Change is used to wake up the A96F902N and the ICWE bit of the RA register is enabled before SLEP, WDT must be disabled. Hence, the A96F902N can be awakened only by Event 3. The following instructions must be executed before SLEP**:**

```
MOV           A, @001110xxb  ;Select WDT prescaler and disable WDT
IOW           IOCA
WDTC                         ;Clear WDT and prescaler
MOV           R6, R6         ;Read Port 6
ENI (or DISI)                ;Enable (or disable) global interrupt
MOV           A, @010xxxxxb  ;Enable Port 6 input change Wake-up bit
MOV           RA,A
MOV           A, @00000x1xb  ;Enable Port 6 input change interrupt
IOW           IOCF
SLEP                         ;Sleep
```

c) If External (P60, /INT) pin changes is used to wake-up the A96F902N and EXWE bit of the RA register is enabled before SLEP, WDT must be disabled by software. Hence, the A96F902N wakes up only by Event 4.

d) If A/D conversion completed is used to wake-up A96F902N and ADWE bit of RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the A96F902N wakes up only by Event 5.

e) If Comparator output status change is used to wake-up A96F902N and CMPWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the A96F902N wakes up only by Event 6. The following instructions must be executed before SLEP**:**

```
BS            R4, 7          ;Select Bank 3
BS            R4, 6
MOV           A, @x10xxxxxb  ;Select a comparator and P70 act as CO pin
MOV           R7,A
MOV           A, @001110xxb  ;Select WDT prescaler and Disable WDT
IOW           IOCA
WDTC                         ;Clear WDT and prescaler
ENI (or DISI)                ;Enable (or disable) global interrupt
MOV           A, @100xxxxxb  ;Enable comparator output status change
                             ;wake-up bit
MOV           RA,A
MOV           A, @10000000b  ;Enable comparator output status change
                             ;interrupt
IOW           IOCE
SLEP                         ;Sleep
```

6.5.2 Summary of Wake-up and Interrupt Modes Operation

All categories under Wake-up and Interrupt modes are summarized below.

The controller can be awakened from Sleep mode and Idle mode. The Wake-up signals are listed as follows**:**

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	If enable EXWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If enable EXWE bit Wake-up + interrupt (if interrupt is enablee) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Port 6 pin change	If enable ICWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCC overflow interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Comparator interrupt	If enable CMPxWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	If enable CMPxWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction

(Continuation)

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
AD conversion complete interrupt	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	Interrupt (if interrupt is enabled) or next instruction **Fs and Fm don't stop**	Interrupt (if interrupt is enabled) or next instruction
TC2 interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TC3 interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. If interrupt is enabled → interrupt+ next instruction

2. If interrupt is disabled → next instruction

6.5.3 Summary of Register Initial Values

Legend: ***x:*** *Not used* ***P:*** *Previous value before reset*
U: *Unknown or don't care* ***t:*** *Check tables under Section 6.5.4*

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC6	Bit Name	×	×	×	×	C63	C62	C61	C60
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x07	IOC7	Bit Name	C77	×	×	×	C73	C72	C71	C70
		Power-on	1	0	0	0	1	1	1	1
		/RESET and WDT	1	0	0	0	1	1	1	1
		Wake-up from Pin Change	P	0	0	0	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	IOC8	Bit Name	×	×	×	×	C83	×	×	×
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
N/A	CONT	Bit Name	INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	IAR7	IAR6	IAR5	IAR4	IAR3	IAR2	IAR1	IAR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	A7	A6	A5	A4	A3	A2	A1	A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	×	×	×	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	0	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	P5 (Bank 0)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	P6 (Bank 0)	Bit Name	x	x	x	x	P63	P62	P61	P60
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x07	P7 (Bank 0)	Bit Name	P77	x	x	x	P73	P72	P71	P70
		Power-on	1	0	0	0	1	1	1	1
		/RESET and WDT	1	0	0	0	1	1	1	1
		Wake-up from Pin Change	P	0	0	0	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	P8 (Bank 0)	Bit Name	x	x	x	x	P83	x	x	x
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0X09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (Bank 0)	Bit Name	CMP2 WE	ICWE	ADWE	EXWE	×	CMP1 WE	CMP3 WE	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	0	P	0	0
0X0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	x	x	x
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0X0C	RC (Bank 0)	Bit Name	×	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0E	RE (Bank 0)	Bit Name	×	TIMER SC	CPUS	IDLE	×	×	×	×
		Power-on	0	1	1	1	0	0	0	0
		/RESET and WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	0	0	0	0
0x0F	RF (ISR) (Bank 0)	Bit Name	CMPIF3	ADIF	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0x8	R8 (Bank 1)	Bit Name	RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	Option RCM1	Option RCM0	0	0	0	0	0	0
		/RESET and WDT	Option RCM1	Option RCM0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9	R9 (Bank 1)	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XA	RA (Bank 1)	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 1)	Bit Name	CMPIF1	CMPIF2	TCIF3	TCIF2	×	×	×	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	0	0	0	0
0x05	R5 (Bank 2)	Bit Name	ADE8	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6 (Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	R7 (Bank 2)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	×	OPADEN	OPADS
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
0x8	R8 (Bank 2)	Bit Name	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9 (Bank 2)	Bit Name	×	×	×	×	×	×	ADD1	ADD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	P	P
0x0F	RF (Bank 2)	Bit Name	×	×	×	×	/PH73	/PH72	/PH71	/PH70
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0X06	R6 (Bank 3)	Bit Name	MLB	×	×	×	×	RBit 10	RBit 9	RBit 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	0	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	R7 (Bank 3)	Bit Name	CP1OUT	CO1S1	CO1S0	CP2OUT	CO2S1	CO2S0	×	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	0	0
0XD	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE (Bank 3)	Bit Name	TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 3)	Bit Name	×	×	×	×	/PD73	/PD72	/PD71	/PD70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0A	IOCA	Bit Name	WDTE	EIS	×	×	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	0	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	×	×	×	×	OD3	OD2	OD1	OD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0D	IOCD	Bit Name	×	×	×	×	/PH3	/PH2	/PH1	/PH0
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0E	IOCE	Bit Name	CMPIE1	CMPIE2	TCIE3	TCIE2	×	×	×	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	0	0	0	0

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	IOCF	Bit Name	CMPIE3	ADIE	×	×	×	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	0	0	P	P	P
0x10~ 0x2F	R10~ R2F	Bit Name	R7	R6	R5	R4	R3	R2	R1	R0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.5.4 Status of RST, T, and P of the Status Register

A RESET condition is initiated by the following events**:**

1) Power-on condition

2) High-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of T and P, listed in Table 6-3 are used to check how the processor wakes up. Table 6-4 shows the events that may affect the status of T and P.

■ **Values of RST, T and P after Reset:**

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

■ **Status of T and P Being Affected by Events**

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous value before reset*

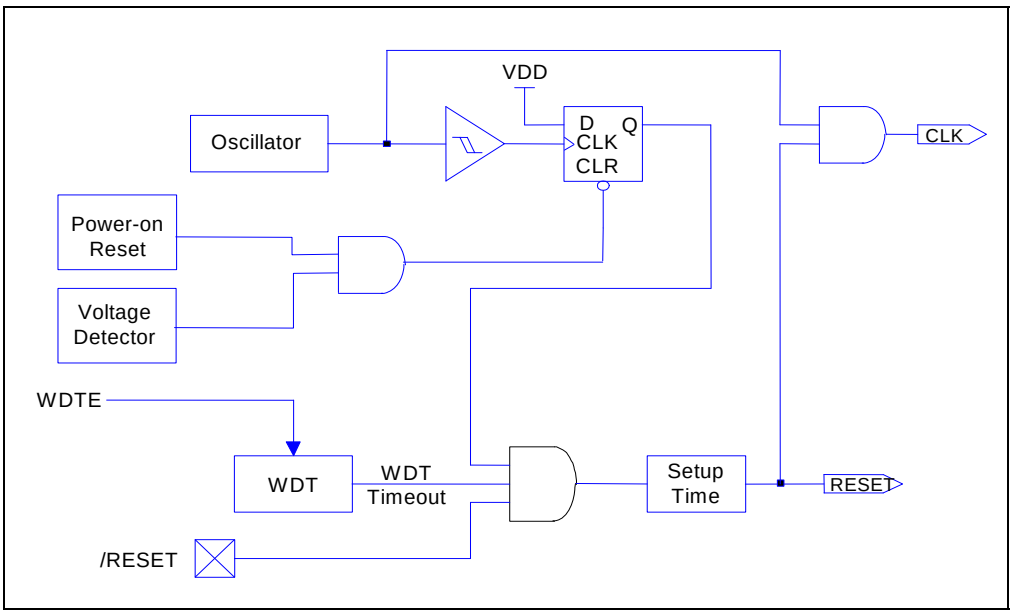


Figure 6-15 Controller Reset Block Diagram

6.6 Interrupt

The A96F902N has 8 interrupts (4 external, 4 internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	Comparator 1	ENI + CMPIE1=1	CMPIF1	000F	4
External	Comparator 2	ENI + CMPIE2=1	CMPIF2	0015	5
Internal	TC2	ENI + TCIE2=1	TCIF2	0024	6
Internal	TC3	ENI + TCIE3=1	TCIF3	0027	7
Internal	AD	ENI + ADIE=1	ADIF	0030	8
External	Comparator3	ENI + CMPIE3=1	CMPIF3	0033	9

RF is the interrupt status register that records the interrupt requests in the relative flags/ bits. IOCF is the interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt is equipped with an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise). **However, in Low Crystal oscillator (LXT) mode, the noise rejection circuit will be disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register are saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, the ACC, R3, and R4 are pushed back.

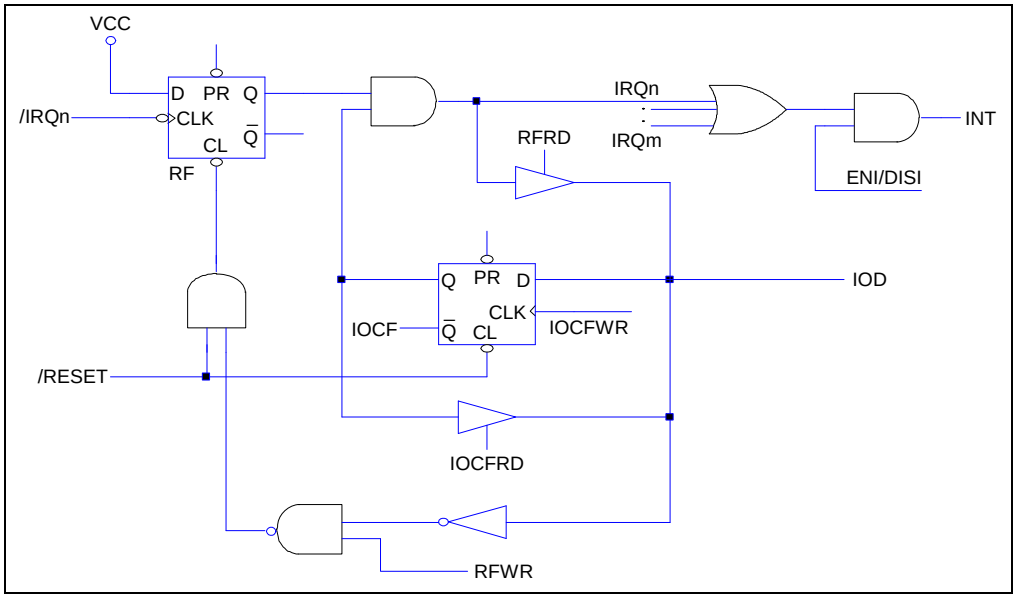


Figure 6-16 Interrupt Input Circuit

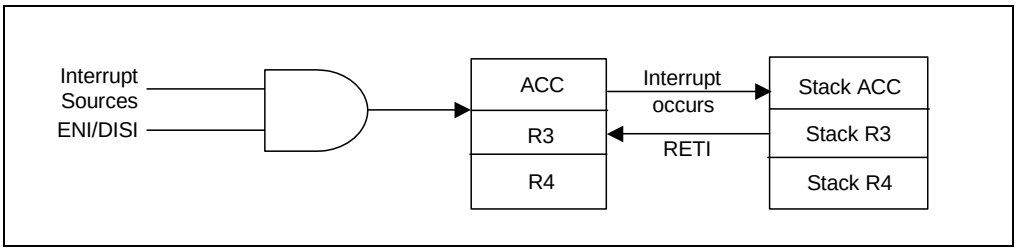


Figure 6-17 Interrupt Back-up Diagram

6.7 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is based on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.7.1 Data EEPROM Control Register

6.7.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM contents (RD can be set by software and is cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software and is cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit

0: Write to the EEPROM is prohibited.

1: Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating.

Bits 2 ~ 0: Not used, set to "**0**" at all time.

6.7.1.2 RC (128 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (128 bytes EEPROM address register) holds the address to be accessed. According the operation, the RD (128 bytes EEPROM Data register) holds the data to be written, or the data read; at the address in the RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7: Not used, set to "**0**" at all time.

Bits 6 ~ 0: 128 bytes EEPROM address

6.7.1.3 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

6.7.2 Programming Step / Demonstration Example

■ **Programming Step:**

Follow these steps to write or read data from the EEPROM**:**

Step 1. Set the RB.EEPC bit to "**1**" for enable EEPROM power.

Step 2. Write the address to RC (128 bytes EEPROM address) as follows**:**

1) (a) Set the RB.EEWE bit to "**1**", if the write function is employed.

(b) Write the 8-bit data value to be programmed in the RD (256 bytes EEPROM data).

(c). Set the RB.WR bit to "**1**", then; execute write function.

2) Set the RB.READ bit to "**1**", after which; execute read function.

Step 3. Wait for the RB.EEDF or RB.WR to be cleared

Step 4. For the next conversion, start from Step 2 again.

Step 5. If you want to save power, make sure the EEPROM data is not used by clearing the RB.EEPC.

■ **Demonstration Programs Example:**

```
;Define control register and write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC     ;Set the EEPROM power on
MOV A,@0x0A
MOV RC,A        ;Assign the address from EEPROM
BS RB, EEWE     ;Enable the EEPROM write function
MOV A,@0x55
MOV RD,A        ;Set the data for EEPROM
BS RB,WR        ;Write value to EEPROM
JBC RB,EEDF     ;Check whether the EEPROM bit is completed or not
JMP $-1
```

6.8 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 10-bit analog multiplexer, three control registers (AISR/R5 (Bank 2), ADCON/R6 (Bank 2), ADOC/R7 (Bank 2)), two data registers (ADDH, ADDL//R8, R9), and an ADC with 10-bit resolution. The analog reference voltage (Vref) and analog ground are connected via separate input pins. The functional block diagram of the ADC is shown below.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2, ADIS1, and ADIS0.

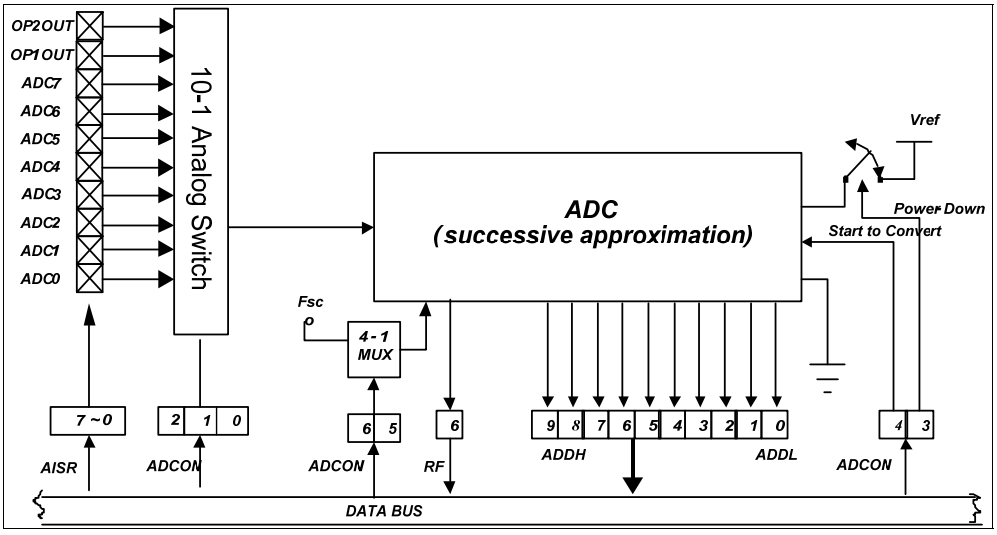


Figure 6-18 Analog-to-Digital Conversion Functional Block Diagram

6.8.1 ADC Control Register (AISR/R5, ADCON/R6, ADOC/R7)

6.8.2 Bank 2 R5 AISR (ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE8	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1

The AISR register defines the ADC pins as analog input or as digital I/O.

Bit 7 (ADE8): AD converter enable bit of P57 pin

0: Disable ADC8, P57 act as I/O pin

1: Enable ADC8 act as analog input pin

Bit 6 (ADE7): AD converter enable bit of P56 pin

0: Disable ADC7, P56 act as I/O pin

1: Enable ADC7 act as analog input pin

Bit 5 (ADE6): AD converter enable bit of P77 pin

0: Disable ADC6, P77 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 4 (ADE5): AD converter enable bit of P73 pin

0: Disable ADC5, P73 act as I/O pin

1: Enable ADC5 act as analog input pin

Bit 3 (ADE4): AD converter enable bit of P63 pin.

0: Disable ADC4, P63 act as I/O pin

1: Enable ADC4 act as analog input pin

Bit 2 (ADE3): AD converter enable bit of P62 pin.

0: Disable ADC3, P62 act as I/O pin

1: Enable ADC3 act as analog input pin

Bit 1 (ADE2): AD converter enable bit of P61 pin

0: Disable ADC2, P61 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 0 (ADE1): AD converter enable bit of P60 pin

0: Disable ADC1, P60 act as I/O pin

1: Enable ADC1 act as analog input pin

The following table shows the priority of P60/AD1//INT.

P60/ADC0//Int Pin Priority		
Hight	Medium	Low
/INT	AD1	P60

6.8.3 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the Vref of the ADC.

0: Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): Prescaler of oscillator clock rate of ADC

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
01	F_{OSC}	1 MHz
10	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0: Reset upon completion of AD conversion. This bit cannot be reset by software.

1: A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating.

Bit 2~0 (ADIS2~ADIS0): AD input select bits

ADIS2	ADIS1	ADIS0	AD Input Pin
0	0	0	AD1
0	0	1	AD2
0	1	0	AD3
0	1	1	AD4
1	0	0	AD5
1	0	1	AD6
1	1	0	AD7
1	1	1	AD8

6.8.4 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	OPADEN	OPADS

Bit 7 (CALI): Calibration enable bit for A/D offset

0: Calibration disable

1: Calibration enable

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	Offset
0	**0**	**0**	0LSB
0	**0**	**1**	1LSB
0	**1**	**0**	2LSB
0	**1**	**1**	3LSB
1	**0**	**0**	4LSB
1	**0**	**1**	5LSB
1	**1**	**0**	6LSB
1	**1**	**1**	7LSB

Bits 2: Not used, set to "**0**" at all time

Bit 1 (OPADEN): OPOUT connects to ADC Enable bit

0: ADC is not dedicated to OP output.

1: ADC is dedicated to OP output.

OPADEN	ADIS2	ADIS1	ADIS0	AD Input Select
1	×	×	×	OPx output
0	×	×	×	ADx

Bit 0 (OPADS): OPOUT connects to ADC select

0: OP1 output connects to AD

1: OP2 output connects to AD

6.8.5 ADC Data Buffer (ADDH, ADDL/R8, R9)

When the A/D conversion is completed, the result is loaded to the ADDH, ADDL. The ADRUN bit is cleared, and the ADIF is set.

6.8.6 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, the acquisition time must be completely done before the conversion can be started.

6.8.7 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the A96F902N, the conversion time per bit is 1μs. The following table shows the relationship between Tct and the maximum operating frequencies.

CKR0: CKR1	Operation Mode	Max. Operating Frequency	Max. Conversion Rate Per Bit	Max. Conversion Rate(10bit)
00	Fosc/4	4 MHz	4 MHz (1μs)	(10+9)*1μs=19us(52.6kHz)
01	Fosc	1 MHz	1 MHz (1μs)	(10+9)*1μs=19us(52.6kHz)
10	Fosc/16	16 MHz	16 MHz (1μs)	(10+9)*1μs=19us(52.6kHz)
11	Fosc/2	2 MHz	2 MHz (1μs)	(10+9)*1μs=19us(52.6kHz)

AD convertion time (10bits)**:** 3 fsys (DGD) + 1.5 A/D (DGD) + 4A/D(AMD) + 10A/D (AMD).

NOTE

- *The pin that is not used as analog input pin, can be used as a regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.8.8 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during Sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillators, TCC, TC2, TC3, and A/D conversion.

The AD Conversion is considered completed when**:**

1. ADRUN bit of R6 register Is cleared to "**0**".
2. Wake-up from A/D conversion remains in operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of ADPD bit is.

6.8.9 Programming Steps/Considerations

■ **Programming Steps**

Follow the steps below to obtain data from the ADC**:**

1. Write to the eight bits (ADE8 ~ ADE1) on the R5 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, and voltage reference pin).
2. Write to the R6/ADCON register to configure the AD module**:**
   a) Select A/D input channel (ADIS1 ~ ADIS0)
   b) Define the A/D conversion clock rate (CKR1 ~ CKR0)
   c) Select the input source of the VREFS of the ADC
   d) Set the ADPD bit to "**1**" to begin sampling
3. Set the ADWE bit, if the wake-up function is employed.
4. Set the ADIE bit, if the interrupt function is employed.
5. Write "ENI" instruction, if the interrupt function is employed.
6. Set the ADRUN bit to "**1**".
7. Wait for wake-up or for ADRUN bit to clear to "**0**"
8. Read ADDATA, ADOC conversion data registers
9. Clear the interrupt flag bit (ADIF) when A/D interrupt function occurrs.

10. For the next conversion, repeat from Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

> **NOTE**
> *To obtain an accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.*

■ **Sample Demo Programs**

```
;Define a General Registers
R_0 == 0              ;Indirect addressing register
PSW == 3              ;Status register
PORT5 == 5
PORT6 == 6
RE== 0XE              ;wake-up control resister
RF== 0XF              ;Interrupt status register

;Define the Control Register
IOC50 == 0X5          ;Control Register of Port 5
IOC60 == 0X6          ;Control Register of Port 6
C_INT== 0XF           ;Interrupt Control Register

;ADC Control Registers
ADDATA == 0x8         ;The contents are the results of ADC
AISR == 0x08          ;ADC intput select register
ADCON == 0x6          ; 7   6   5    4    3    2    1    0
                      VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0

;Define Bits in ADCON
ADRUN == 0x4          ;ADC is executed as the bit is set
ADPD == 0x3           ;Power Mode of ADC

;Program Starts
ORG 0                 ;Initial address
JMP INITIAL

ORG 0x30              ;Interrupt vector
;
;
(User's program)
;
;
CLR RF                ;To clear the ADIF bit
BS ADCON, ADRUN       ;To start executing the next AD conversion
                      ; if necessary
RETI
```

```
INITIAL:
MOV A, @0B00000001          ;To define P60 as an analog input
MOV AISR, A
MOV A, @0B00001000          ;To select P60 as an analog input
                            ; channel, and AD power on
MOV ADCON, A                ;To define P60 as an input pin and
                            ; set clock rate at fosc/16

En_ADC:
MOV A, @0BXXXXXXX1          ;To define P60 as an input pin, and
                            ; the others are dependent on
                            ; on applications
IOW PORT6
MOV A, @0BXXXX1XXX          ;Enable the ADWE wake-up function
                            ; of ADC. "X" is per application.
MOV RE, A
MOV A, @0BXXXX1XXX          ;Enable the ADIE interrupt function
                            ; of ADC. "X" is per application.
IOW C_INT

ENI                         ;Enable the interrupt function
BS ADCON, ADRUN             ;Start to run the ADC

;If the interrupt function is employed, the following three lines
; may be ignored.
POLLING:
JBC ADCON, ADRUN            ;To check the ADRUN bit continuously
JMP POLLING                 ;ADRUN bit will be reset as the AD
                            ; conversion is completed.
;
;
(User program)
;
;
```

6.9 Timer/Counter 2

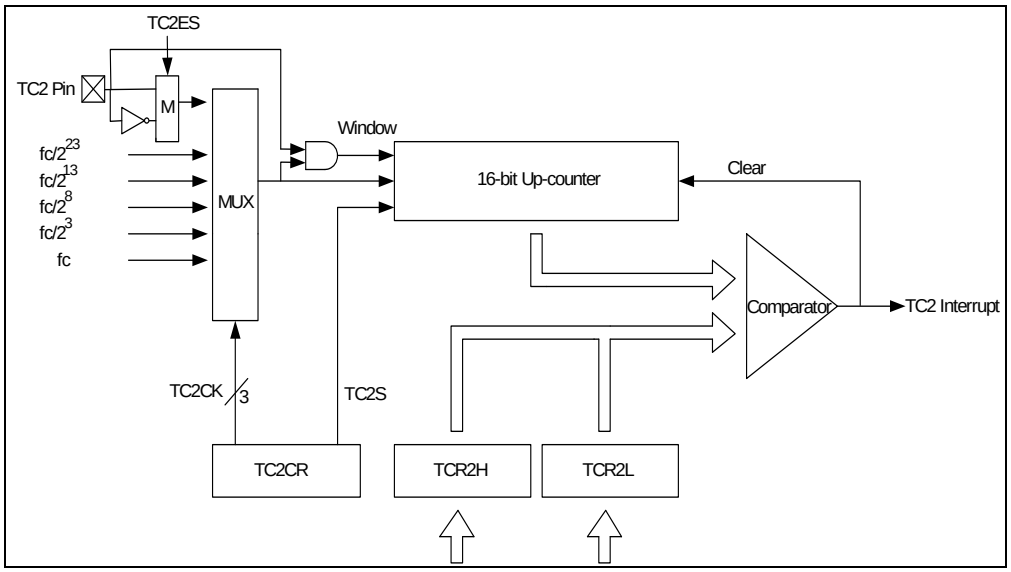


Figure 6-19 Timer / Counter 2 Mode Configuration

6.9.1 Timer Mode

In Timer mode, counting up is performed by using the internal clock. When the contents of the up-counter match with TCR2 (TCR2H+TCR2L), interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

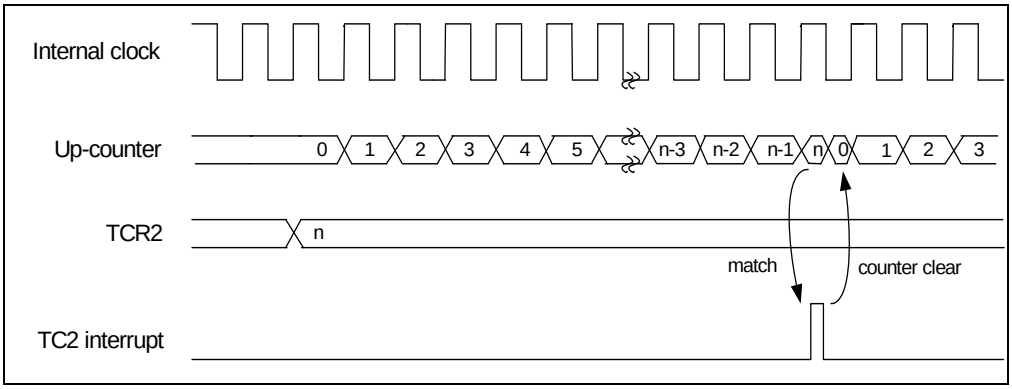


Figure 6-20 Timer Mode Timing Diagram

6.9.2 Counter Mode

In Counter mode, counting up is performed by using the external clock input pin (TC2 pin) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter match with TCR2 (TCR2H+TCR2L), interrupt is then generated and counter is cleared. Counting up resumes after the counter is cleared.

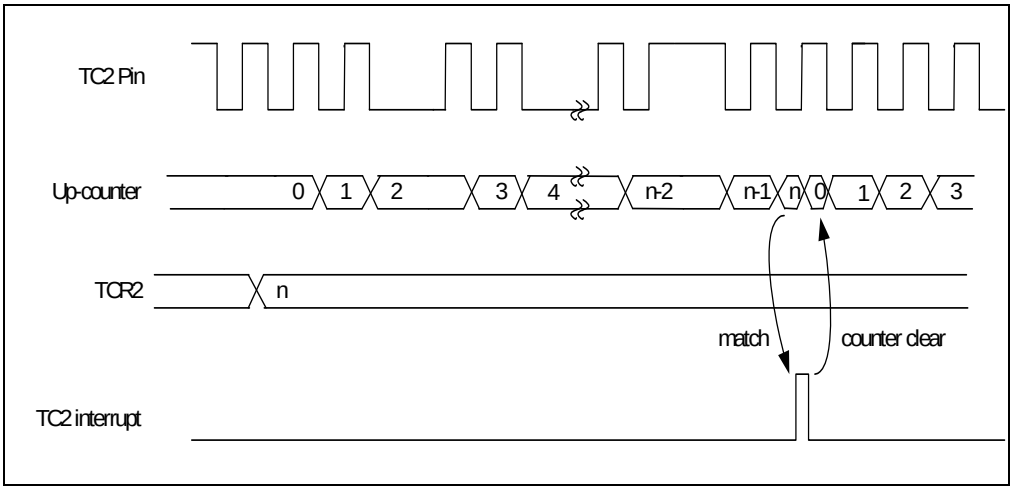


Figure 6-21 Counter Mode Timing Diagram (INT2ES = 1)

6.9.2 Window Mode

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and of the TC2 pin (window pulse). When the contents of the up-counter match with TCR2 (TCR2H+TCR2L), interrupt is then generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

While writing to the TCR2L, the comparison is inhibited until TCR2H is written.

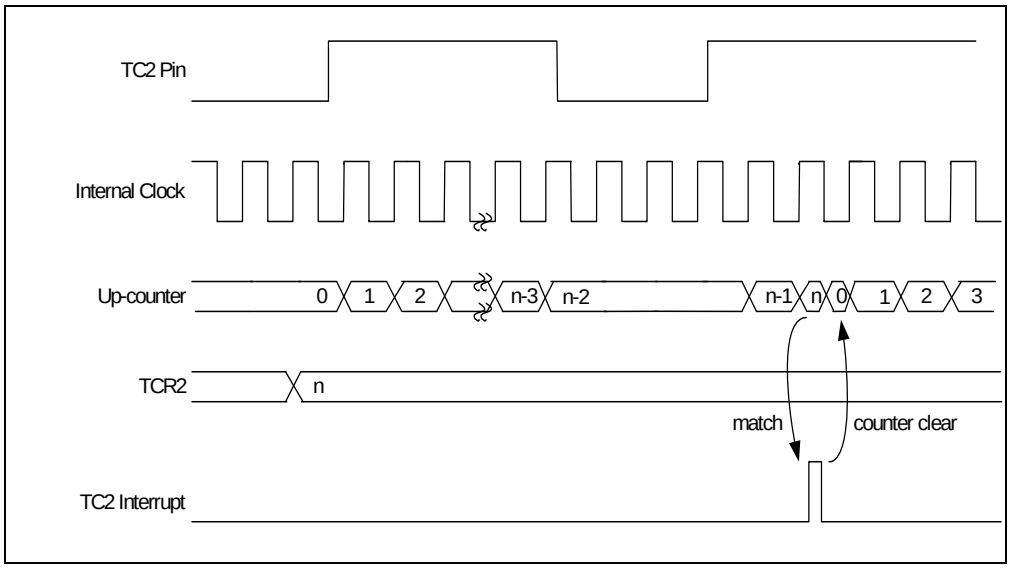


Figure 6-22 Window Mode Timing Diagram

6.10 Timer/Counter 3

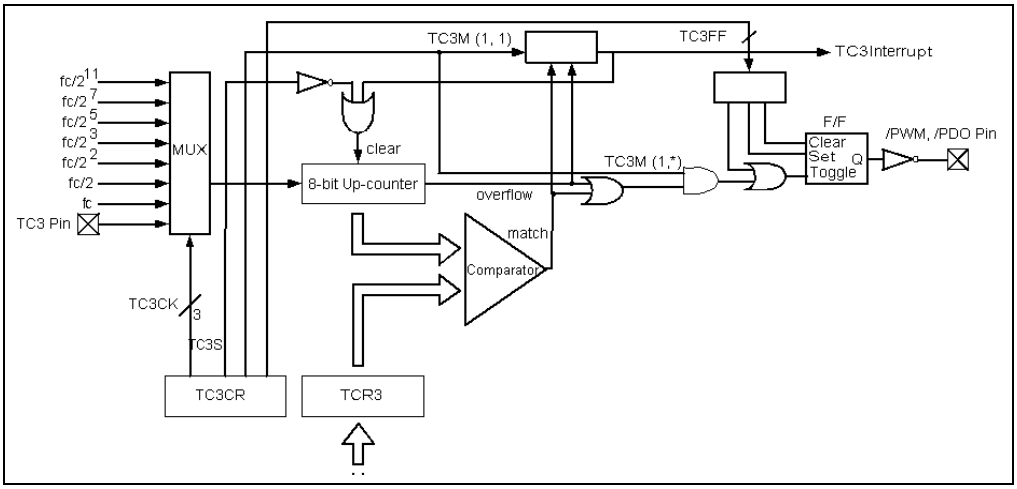


Figure 6-23 Timer / Counter 3 Mode Configuration

■ Timer Mode

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match with TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

■ Counter Mode

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter match with TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

■ Programmable Divider Output (PDO) Mode

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

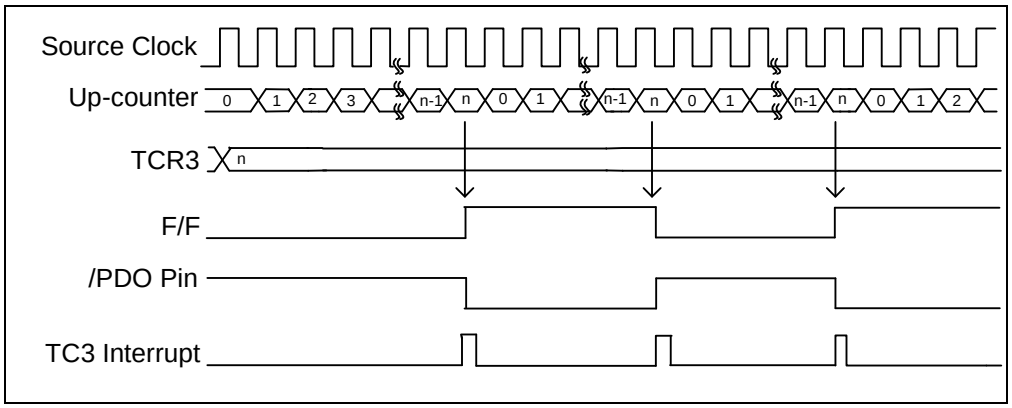


Figure 6-24 PDO Mode Timing Diagram

■ Pulse Width Modulation (PWM) Output Mode

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. Then the counter continues counting, and the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output; will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the TRC3 is shifted for the first time by setting TC3S to "**1**" after data is loaded to TCR3.

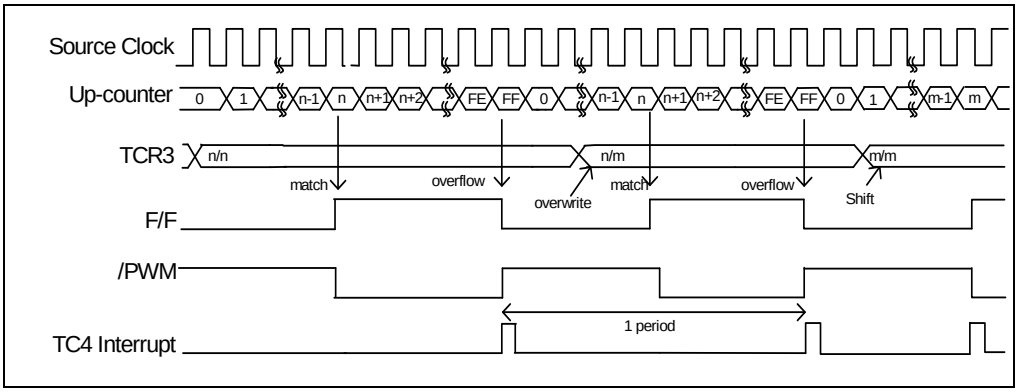


Figure 6-25 PWM Mode Timing Diagram

6.11 Comparator

The A96F902N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up A96F902N from sleep mode. The comparator circuit diagram is depicted in the figure below.

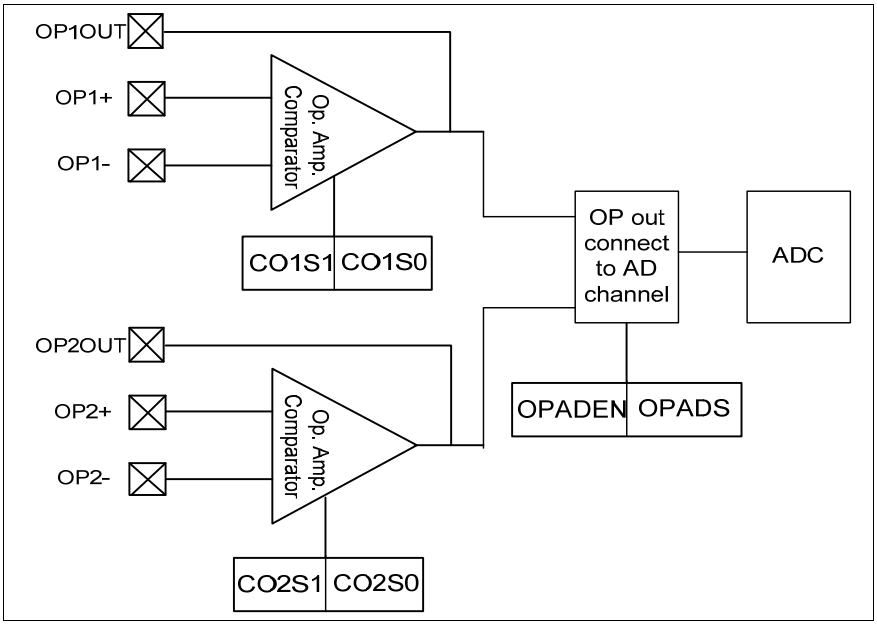


Figure 6-26 Operational Amplifier Comparator Block Diagram

6.11.1 External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations**:**

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.11.2 Comparator Outputs

- The compared result is stored in the CPxOUT of Bank 3 R7.
- The comparator outputs are sent to CO (P70) by programming Bit 5, Bit 6<CO1S1, CO1S0> of the Bank3 R7 register to <1, 0>. See Section 6.1.31, *Bank 3 R7 (CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

The following figure shows the Comparator Output block diagram.

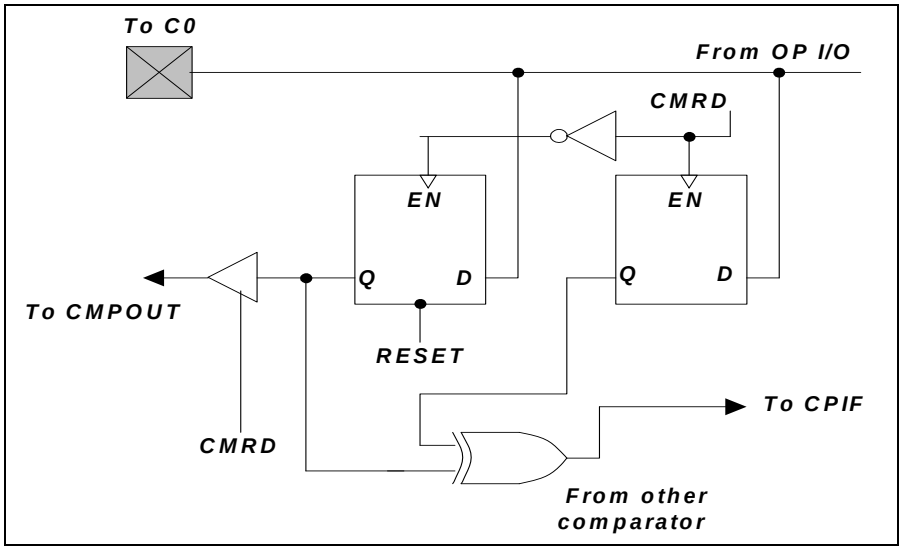


Figure 6-27 Comparator Output Configuration

6.11.3 Using Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output. In this case, the Schmitt trigger function can be disabled for power saving purposes, by setting Bit 6, Bit 5<CO1S1, CO1S0> of the Bank3 R7 register to <1, 1>. See Section 6.1.31, Bank3 R7 *(CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

6.11.4 Comparator Interrupt

- CMPIE1 (IOCE.7) must be enabled for the “ENI” instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CP1OUT, Bank 3 R7<6>.
- CMPIF1 (RF.7), the comparator interrupt flag, can only be cleared by software.

6.11.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will Wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into Sleep mode.

6.12 Oscillator

6.12.1 Oscillator Modes

The device can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). You can select one of such modes by programming OSC2, OCS1, and OSC0 in the Code Option register. The following table depicts how these four modes are defined.

■ **Oscillator Modes as Defined by OSC2 ~ OSC0**

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)[1]	0	0	0
HXT (High Crystal oscillator mode)[2]	0	0	1
LXT1 (Low Crystal 1 oscillator mode)[3]	0	1	0
LXT2 (Low Crystal 2 oscillator mode)[4]	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

[1] The Frequency range of HXT mode is 16 MHz ~ 6 MHz.
[2] The Frequency range of XT mode is 6 MHz ~ 1 MHz.
[3] The Frequency range of LXT1 mode is 1 MHz ~ 100kHz.
[4] The Frequency range of LXT2 mode is 32kHz.

In LXT, XT, HXT, and ERC modes, OSCI and OSCO are implemented. They cannot be used as normal I/O pins.

In IRC mode, P55 is used as normal I/O pin.

The maximum operating frequency of the crystal/resonator on the different VDD is shown below**:**

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Max Fxt. (MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	5.0	20.0

6.12.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The A96F902N can be driven by an external clock signal through the OSCI pin as illustrated below.

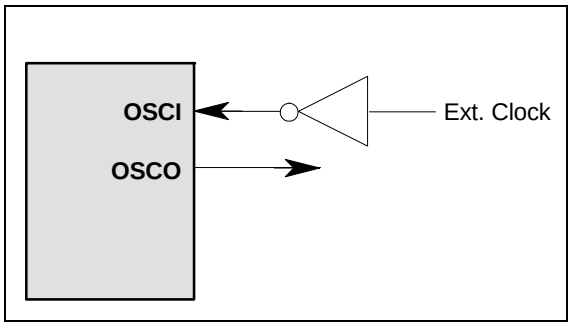


Figure 6-28 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation as depicted in the following figure. The same thing applies to HXT mode or LXT mode.

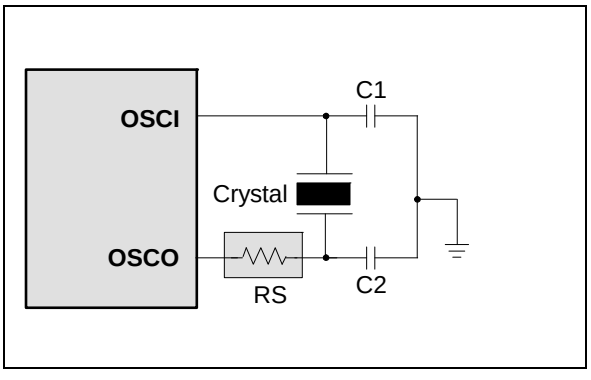


Figure 6-29 Crystal/Resonator Circuit

The following table provides the recommended values of C1 and C2. Since each resonator has its own attributes, you should refer to its specification for appropriate values of C1 and C2. A serial resistor RS, may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100 kHz	67pF	67pF
		200 kHz	30pF	30pF
		455 kHz	50pF	50pF
		1.0 MHz	30pF	30pF
	HXT2 (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	30pF	30pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768 kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100 kHz	67pF	67pF
		200 kHz	30pF	30pF
		455 kHz	30pF	30pF
		1.0 MHz	30pF	30pF
	XT (1~6 MHz)	455 kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	30pF	30pF
		6.0 MHz	30pF	30pF
	HXT (6~20 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	30pF	30pF
		10.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
		20.0 MHz	15pF	15pF

6.12.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Figure 6-30) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable since the NMOS cannot correctly discharge the capacitance current.

Based on the above reasons, it must be kept in mind that the supply voltage, operation temperature, RC oscillator components, the package types, as well s the PCB layout, could affect the system frequency.

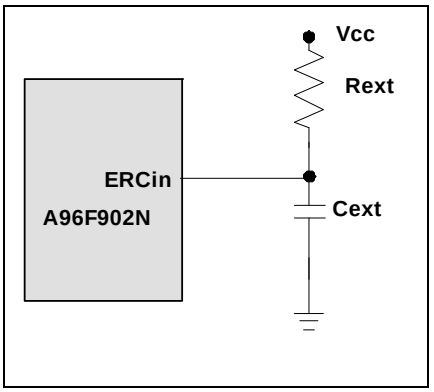


Figure 6-30 External RC Oscillator Mode Circuit

■ **External RC Oscillator Frequencies**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

NOTE: *Measured based on DIP packages. Theoretical values for design reference only.*

6.12.4 Internal RC Oscillator Mode

A96F902N offers a versatile internal RC mode with a default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (8MHz, 16MHz, and 1MHz) that can be set by Code Option (Word 1), RCM1 and RCM0 when COBS=0, or set by Bank 1 R8 Bit7, 6 when COBS=1. All these four main frequencies can be calibrated by programming the Code Option (Word 1) bits, C4~C0.

■ **Internal RC Drift Rate (Ta=25°C, VDD=5 V ± 5%, VSS=0V)**

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.2V~5.5V)	Process	Total
1 MHz	± 3%	± 4%	± 2.5%	± 9.5%
4 MHz	± 3%	± 4%	± 2.5%	± 9.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%

6.13 Code Option Register

The A96F902N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.13.1 Code Option Register (Word 0)

Word 0													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**NRHL**	**NRE**	**RESETENB**	**CLKS1**	**CLKS0**	**ENWDTB**	**OSC2**	**OSC1**	**OSC0**	**PR2**	**PR1**	**PR0**
1	-	8/fc	Disable	Enable	High	High	Enable	High	High	High	High	High	High
0	-	32/fc	Enable	Disable	Low	Low	Disable	Low	Low	Low	Low	Low	Low

Bit 12: Not used, always set to "**0**"

Bit 11 (NRHL): Noise rejection high/low pulse define bit. INT pin is falling edge trigger.

1: Pulses equal to 8/fc [s] is regarded as signal.

0: Pulses equal to 32/fc [s] is regarded as signal (default).

> **NOTE**
> *The noise rejection function is turned off under Low Crystal oscillator (LXT) and Sleep modes.*

Bit 10 (NRE): Noise rejection enable. INT pin is falling edge trigger.

1: Disable noise rejection

0: Enable noise rejection (default) but under Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 9 (RESETENB): Reset pin enable bit

1: Enable, P83//RESET=>RESET pin.

0: Disable, P83//RESET=>P83 (default)

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks	**0**	**0**
2 clocks	**0**	**1**
8 clocks	**1**	**0**
16 clocks	**1**	**1**

Refer to Section 6.17, *Instruction Set*.

Bit 6 (ENWDTB): Watchdog timer enable bit

1: Enable

0: Disable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator mode selection bits

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)[1]	0	0	0
HXT (High Crystal oscillator mode)[2]	0	0	1
LXT1 (Low Crystal 1 oscillator mode)[3]	0	1	0
LXT2 (Low Crystal 2 oscillator mode)[4]	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

[1] The Frequency range of HXT mode is 16 MHz ~ 6 MHz.
[2] The Frequency range of XT mode is 6 MHz ~ 1 MHz.
[3] The Frequency range of LXT1 mode is 1 MHz ~ 100kHz.
[4] The Frequency range of LXT2 mode is 32kHz.

Bit 2 ~ Bit 0 (PR2 ~ PR0): Protect Bit. PR2~PR0 are protect bits. The protect types are follows**:**

PR2	PR1	PR0	Protect
1	1	1	Enable
0	0	0	Disable

6.13.2 Code Option Register (Word 1)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	COBS	TCEN	-	-	C4	C3	C2	C1	C0	RCM1	RCM0	LVR1	LVR0
1	High	TCC	-	-	High	High	High	High	High	High	High	High	High
0	Low	P77	-	-	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 (COBS): Code Option bit selection

0: IRC frequency select for code option (default)

1: IRC frequency select internal register by Bank1 R8(7,6)

Bit 11 (TCEN): TCC enable bit

0: P77/TCC is set as P77.

1: P77/TCC is set as TCC.

Bit 10 ~ Bit 9: Fixed at "**1**"

Bit 8 ~ Bit 4 (C4 ~ C0): Internal RC mode calibration bits. C4 ~ C0 must be set to "**0**" only (auto-calibration).

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
0	**0**	4
0	**1**	16
1	**0**	8
1	**1**	1

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low voltage reset enable bits

LVR1	LVR0	Reset Level	Release Level
0	**0**	NA	NA
0	**1**	2.7V	2.9V
1	**0**	3.5V	3.7V
1	**1**	4.0V	4.2V

NOTE: *LVR1, LVR0="**0, 0**": LVR disable, power- on reset point of A96F902N is 2.0V.*
*LVR1, LVR0="**0, 1**": If Vdd < 2.7V, the A96F902N will reset.*
*LVR1, LVR0="**1, 0**": If Vdd < 3.5V, the A96F902N will reset.*
*LVR1, LVR0="**1, 1**": If Vdd < 4.0V, the A96F902N will reset.*

6.13.3 Customer ID Register (Word 2)

Word 0													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**SC3**	**SC2**	**SC1**	**SC0**	**-**	**EFTIM**	**-**	**-**	**SFS**	**X**	**X**	**X**	**X**
1	High	High	High	High	-	20MHz	-	-	128kHz	High	High	High	High
0	Low	Low	Low	Low	-	10MHz	-	-	16kHz	Low	Low	Low	Low

Bits 12 ~ 9 (SC3 ~ SC0): sub-frequency calibrator (WDT frequency auto calibration)

Bit 8: Fixed at "**0**"

Bit 7 (EFTIM): EFT improvement. If MCU is at VDD=5V with working frequency of <12 MHz, or at VDD=3V with working frequency of <6 MHz, enabling this function can improve the performance of the electrical fast transient (EFT) test. If MCU is at VDD=5V and working frequency is >12 MHz, choose EFTIM=**1**

0: 10 MHz

1: 20 MHz

Bits 6~5: Fixed to "**0**"

Bits 4 (SFS): Sub-frequency select.

0: 16kHz (WDT frequency)

1: 128kHz.

Bits 3~0: Customer's ID code

6.14 Power on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes into steady state. The A96F902N is equipped with a built-in Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd rises fast enough (50 ms or less). However, under critical applications; extra devices may still be required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuit shown in Figure 6-31 uses an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to achieve minimum operation voltage. This circuit is used when the power supply has slow rising time. As the current leakage from the /RESET pin is ±5μA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the moment of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin), will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

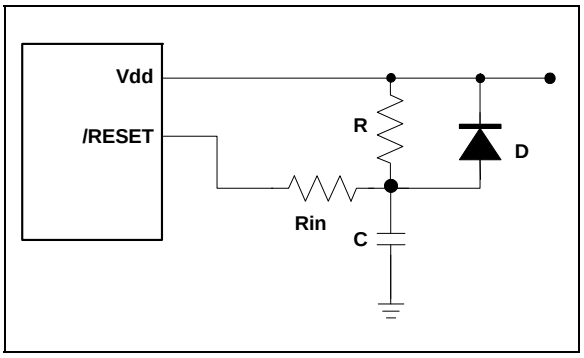


Figure 6-31 External Power-up Reset Circuit

6.16 Residue-Voltage Protection

When battery is replaced, the device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figures below show how to accomplish a proper residue-voltage protection circuit.

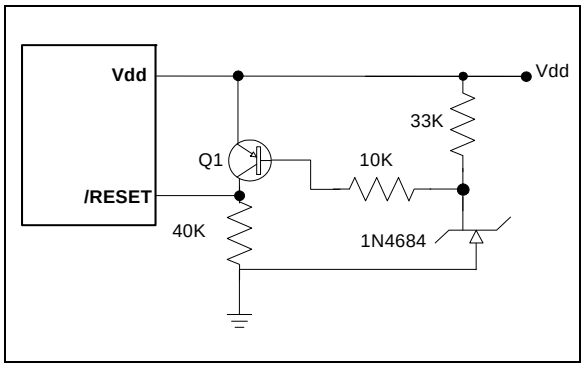


Figure 6-32 Circuit 1 for the Residue Voltage Protection

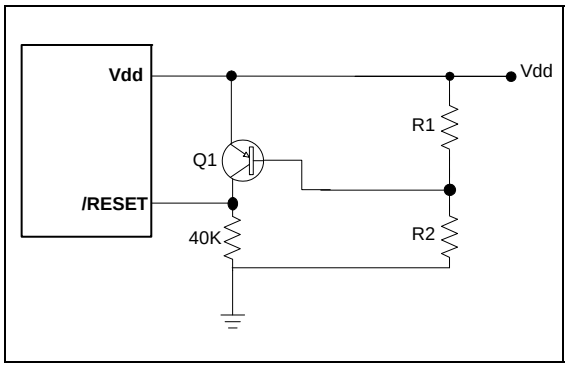


Figure 6-33 Circuit 2 for the Residue Voltage Protection

6.17 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

A) Change one instruction cycle to consist of four oscillator periods.

B) "JMP", "CALL", "RET", "RETL", "RETI" commands are executed with one instruction cycle. The conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case A is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc / 2 as indicated in Figure 6-11 (*TCC and WDT Block Diagram*) of Section 6.3.

In addition, the Instruction Set also has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table:

The following symbols are used in the following table**:**

"**R**" *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

"**b**" *Bit field designator that selects the value for the bit located in the Register "**R**" and which affects the operation.*

"**K**" *8 or 10-bit constant or literal value*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z

[1] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

(Continuation)

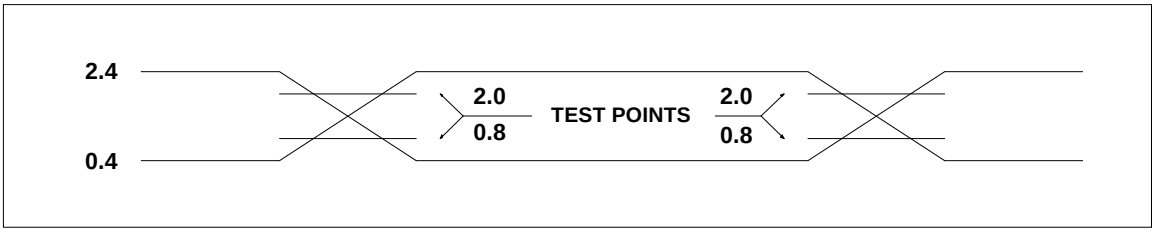
Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	K → R4(7:6)	None
1 1110 1010 kkkk	1EAK	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC4	None
1 1110 1011 kkkk	1EBK	LJMP k	Next instruction : k kkkk kkkk kkkk k→PC4	None
1 1110 11rr rrrr	1Err	TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

[2] *This instruction is not recommended for interrupt status register operation.*

[3] *This instruction cannot operate under interrupt status register.*

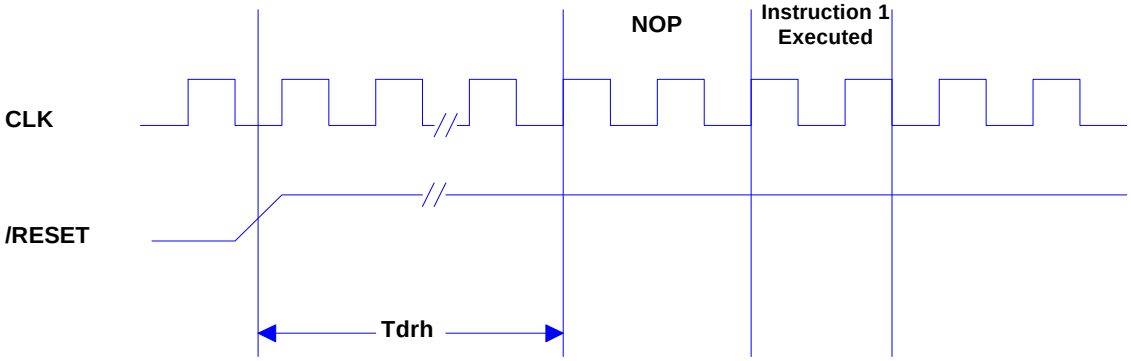
7 Timing Diagrams

AC Test Input/Output Waveform

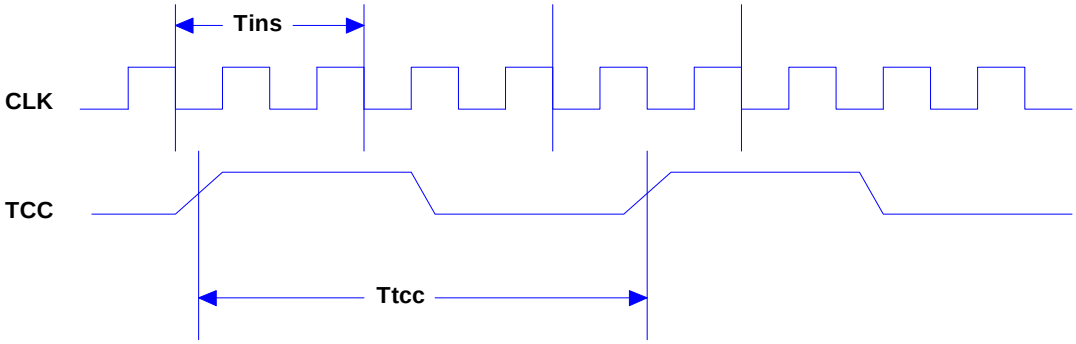


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



8 Absolute Maximum Ratings

■ **A96F902N**

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2	to	5.5V
Working frequency	DC	to	20MHz*
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

**This parameter is theoretical value only and has not been tested.*

9 DC Electrical Characteristic

■ **Ta=25°C, VDD=5.0V±5%, VSS=0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	-	8	MHz
	Crystal: VDD to 5V		DC	-	20	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz, 1 MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high , VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low , VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigge)	Ports 5, 6, 7, 8	-	0.7VDD (2.8V)	-	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-	0.3VDD (2.2V)	-	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	-	0.7VDD	-	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-	0.3VDD	-	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	-	0.7VDD	-	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-	0.3VDD	-	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V

(Contiuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = 0.9VDD	-3	-	-	mA
IOL1	Output Low Voltage (Ports 5, 7, 8)	VOL = 0.1VDD	14	-	-	mA
IOL2	Output Low Voltage (Port 6)	VOL = 0.1VDD	14	-	-	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-	-	-80	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	-	-	30	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	-	-	2	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	-	-	5	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type), output pin floating, WDT disabled	-	43	-	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type), output pin floating, WDT enabled	-	43	-	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type), output pin floating, WDT enabled	-	-	1	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type), output pin floating, WDT enabled	-	-	2.8	mA
ICC5	Operating supply current at two clocks	/RESET= 'High', Fosc=1MHz (IRC type), Voltage = 3V, output pin floating, WDT enabled	-	180	-	μA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "**Min.**", "**Typ.**", & "**Max.**" (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25℃. These data are for design reference only.*

9.1 Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.4V~ 5.5V Temperature = -40°C ~ 85°C	-	4.5	-	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9.2 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	-	4	-	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9.3 A/D Converter Characteristics

■ **Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF	Analog reference voltage	VAREF-VASS= 2.5V to 5.5V	2.5	-	Vdd	V
VASS	–	–	-	Vss	-	V
VAI	Analog input voltage	–	VASS	-	VAREF	V
IAI1	Ivdd	VAREF = Vdd	1150	1300	1450	μA
	Ivref	–	-10	0	10	μA
IAI2	Ivdd	VAREF = VREF	700	800	900	μA
	Ivref	–	450	500	550	μA
RN	Resolution	VAREF=Vdd	8	9	-	Bits
LN	Linearity error	VAREF=Vdd	0	± 2	+/-4	LSB
DNL	Differential nonlinear error	VAREF=Vdd	0	± 0.5	+/-0.9	LSB
FSE	Full scale error	VAREF=Vdd	± 0	± 1	± 2	LSB
OE	Offset error	VAREF=Vdd	± 0	± 1	± 2	LSB
ZAI	Recommended impedance of analog voltage source	VAREF=Vdd	0	8	10	KΩ
TAD1	A/D clock period	VAREF=Vdd=2.5~5.5V Ta= -40~85°C	4	-	-	μs
TAD2	A/D clock period	VAREF=Vdd=3~5.5V Ta= -40~85°C	1	-	-	μs
TCN	A/D conversion time	VAREF=Vdd	14	-	14	TAD
PSR	Power supply rejection	Vdd=Vdd-10% to Vdd+10%	± 0	-	± 2	LSB

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *There is no current consumption when ADC is off other than minor leakage current.*
- *AD conversion result will not decrease when an increase of input voltage and no missing code will result.*
- *These parameters are subject to change without further notice.*

9.4 Comparator Characteristics

■ **Vdd=2.5V, Vss=0V, Ta=25°C**

VOS	Input offset voltage	RL = 5.1K[1]	–	–	5	mV
Vcm	Input common-mode voltages range[2]	–	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	uA
TRS	Response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), overdrive=30mV[3]	–	0.7	–	us
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load),	–	300	–	ns
VS	Operating range	–	2.5	–	5.5	V

[1] *The output voltage is in the unit gain circuitry and over the full input common-mode range.*

[2] *The input common-mode voltage or any of the the input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.*

[3] *The response time specified is a 100mV input step with 30mV overdrive.*

10 AC Electrical Characteristics

■ **-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

***N**: *Selected prescaler ratio*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "**Min.**", "**Typ.**", & "**Max.**" (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25℃. These data are for design reference only.*

10.1 Device Characteristics

The following graphs were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphs, the data may be out of the specified warranted operating range.

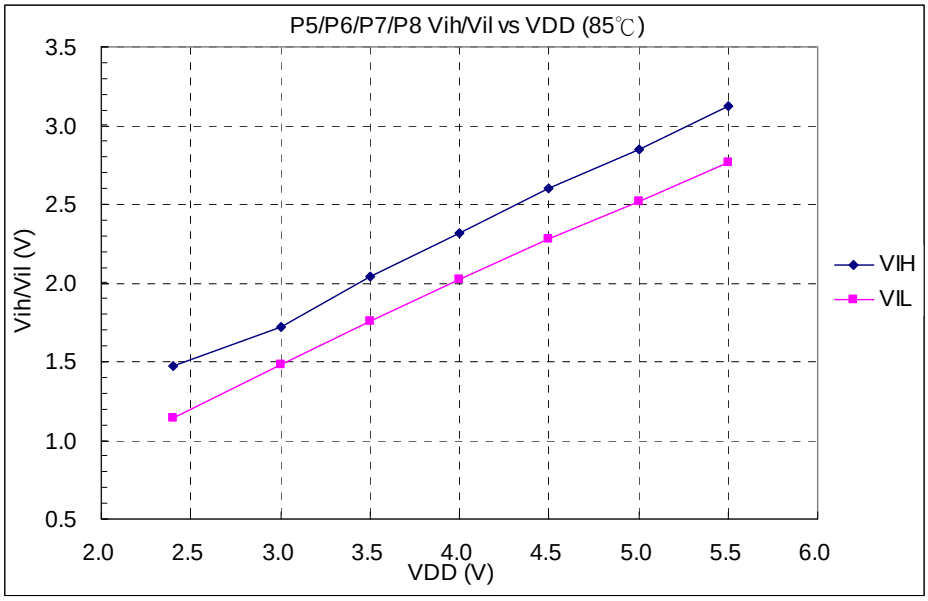


Figure 10-1 VIH/VIL vs. VDD (85°C)

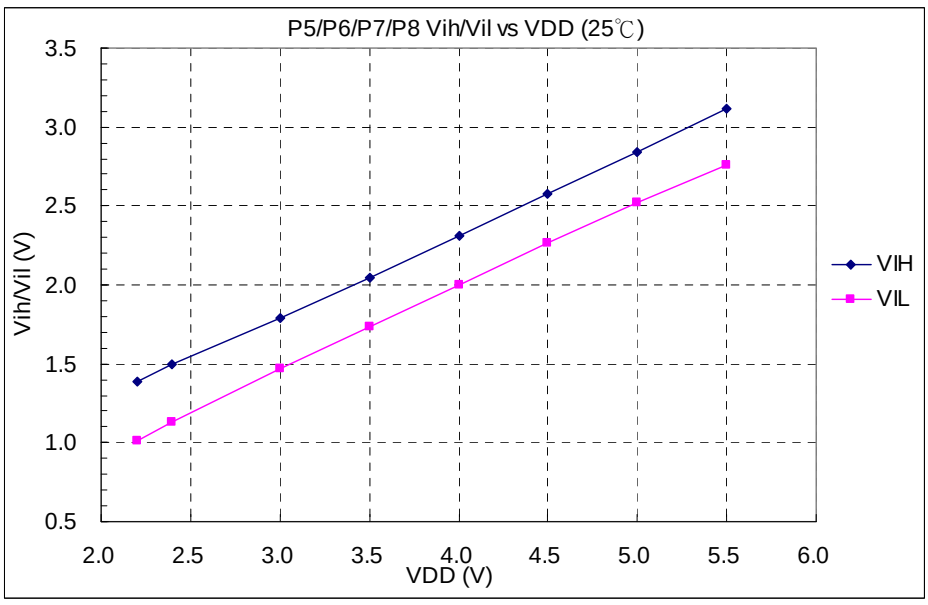


Figure 10-2 VIH/VIL vs. VDD (25°C)

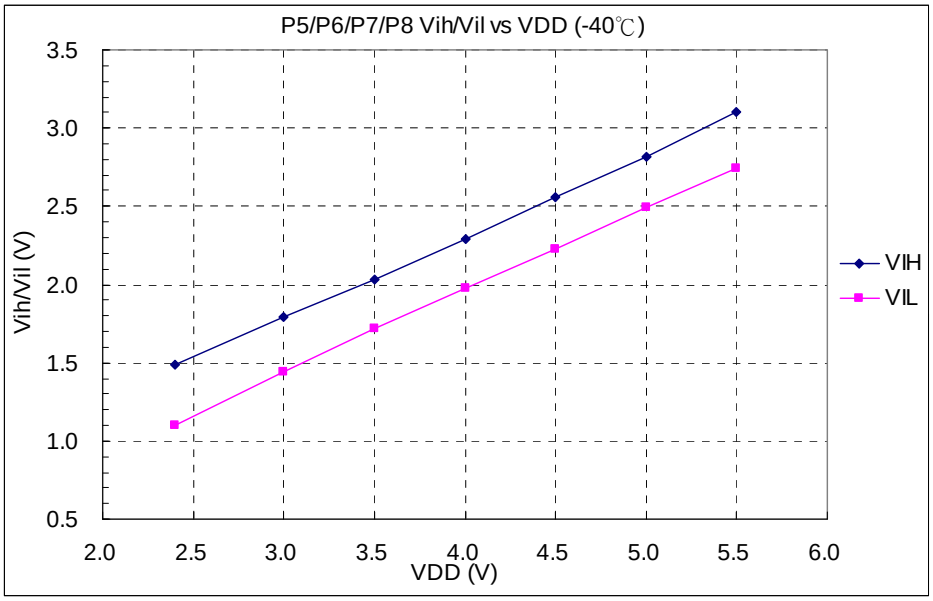


Figure 10-3 VIH/VIL vs. VDD (-40°C)

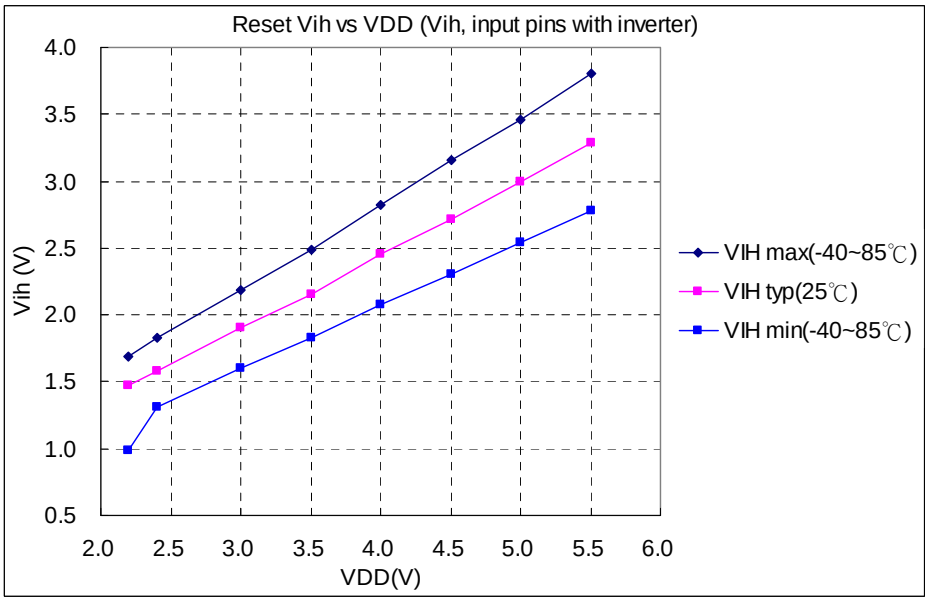


Figure 10-4 VIH of RESET Pin vs. VDD

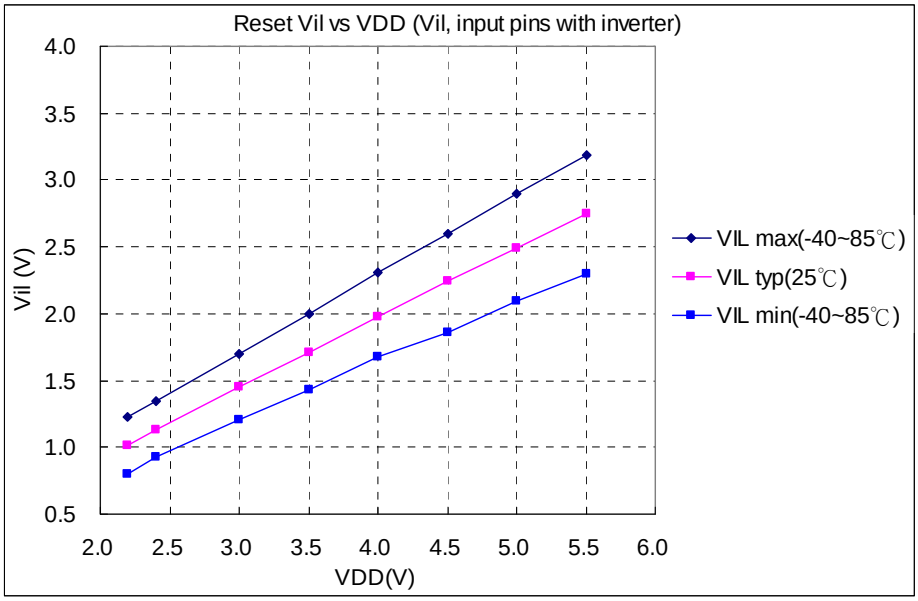


Figure 10-5 VIL of RESET Pin vs. VDD

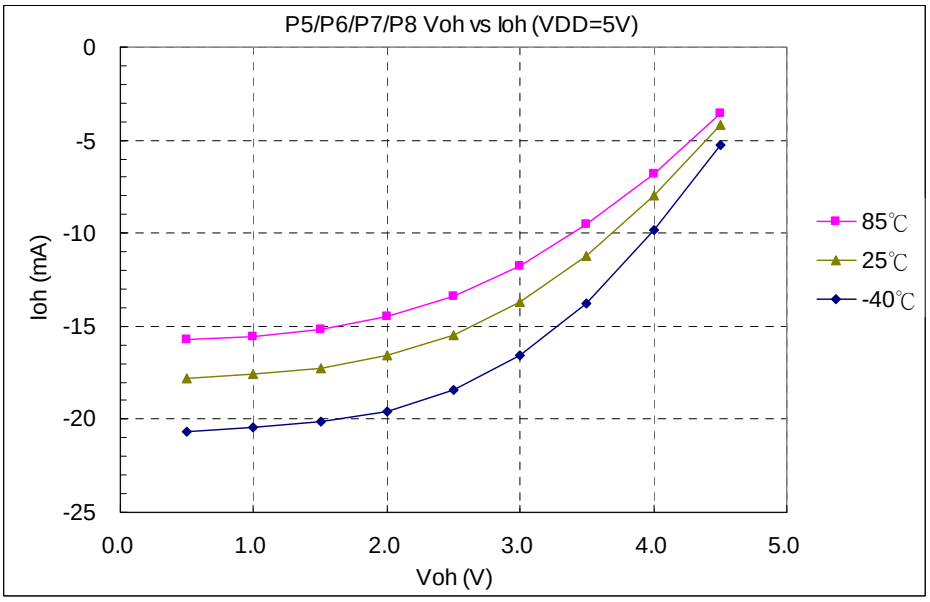


Figure 10-6 VOH vs. IOH, VDD=5V

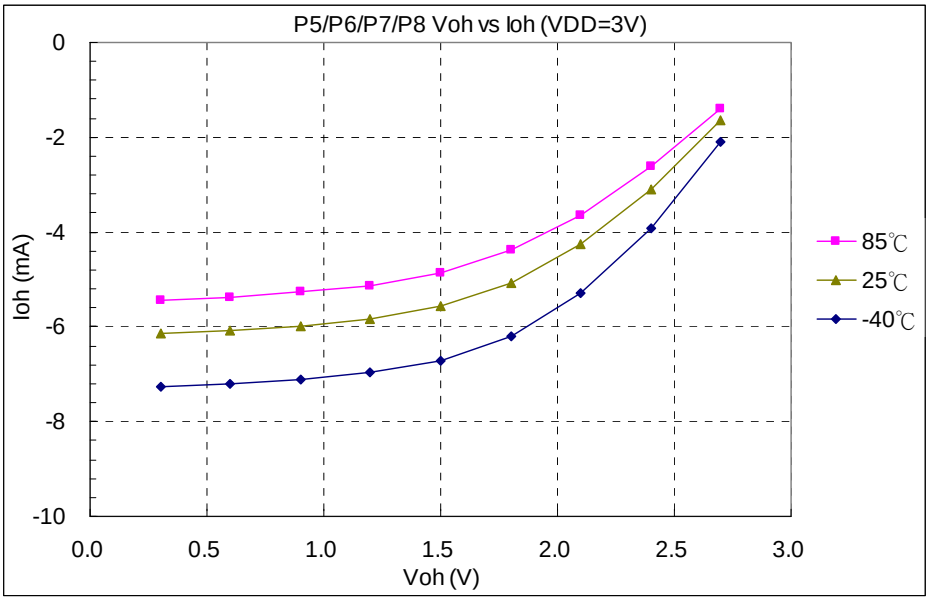


Figure 10-7 VOH vs. IOH, VDD=3V

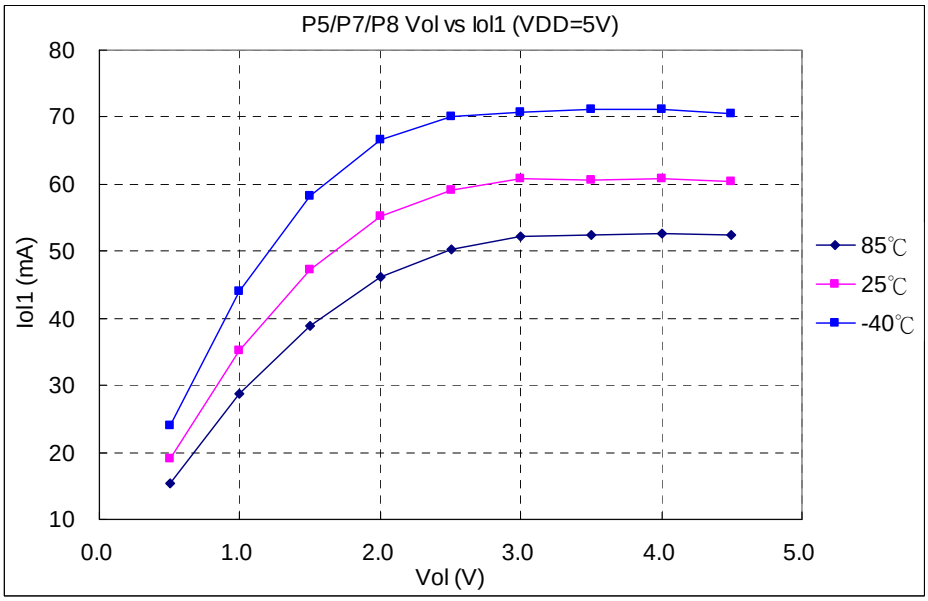


Figure 10-8 VOL vs. IOL, VDD=5V

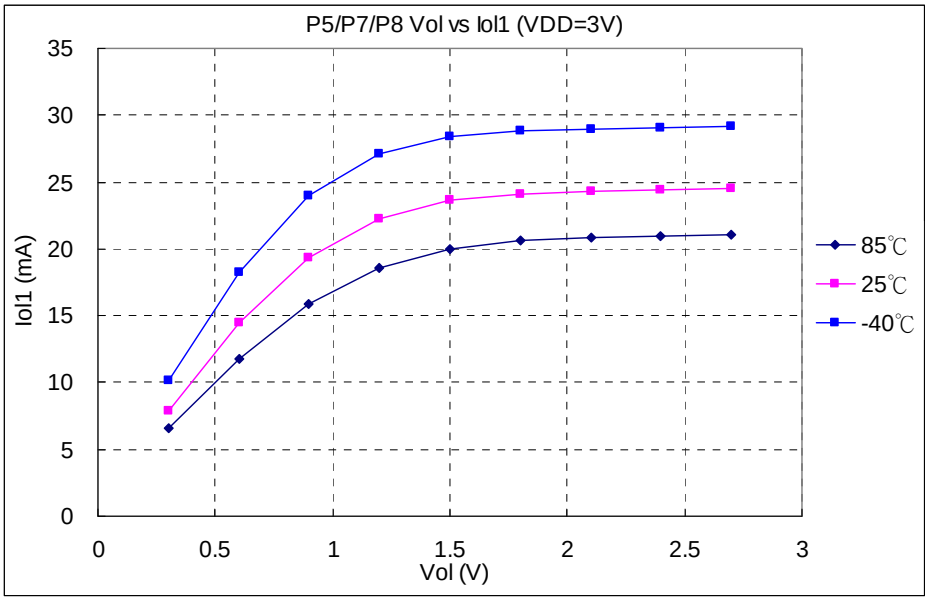


Figure 10-9 VOL vs. IOL, VDD=3V

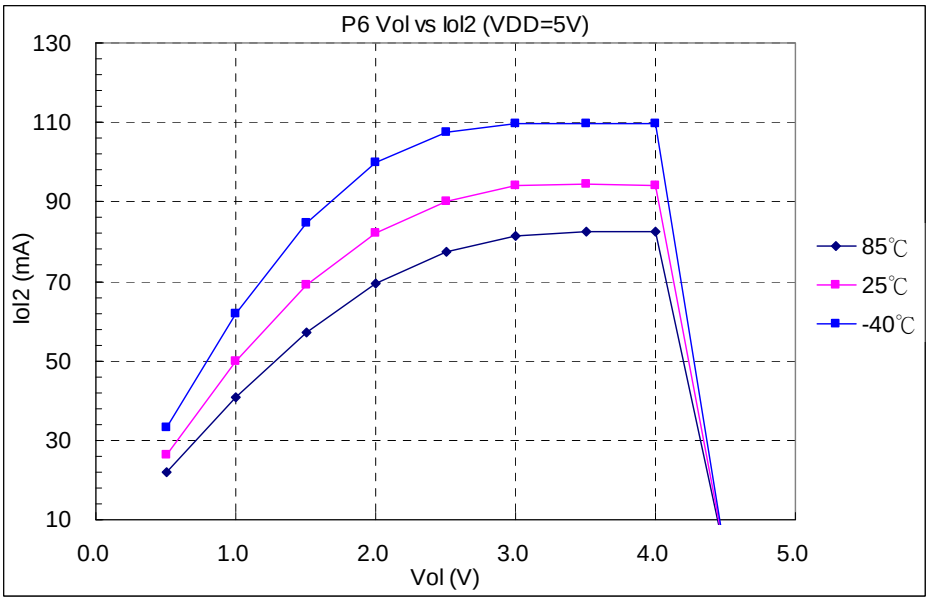


Figure 10-10 VOL of P6 vs. IOL, VDD=5V

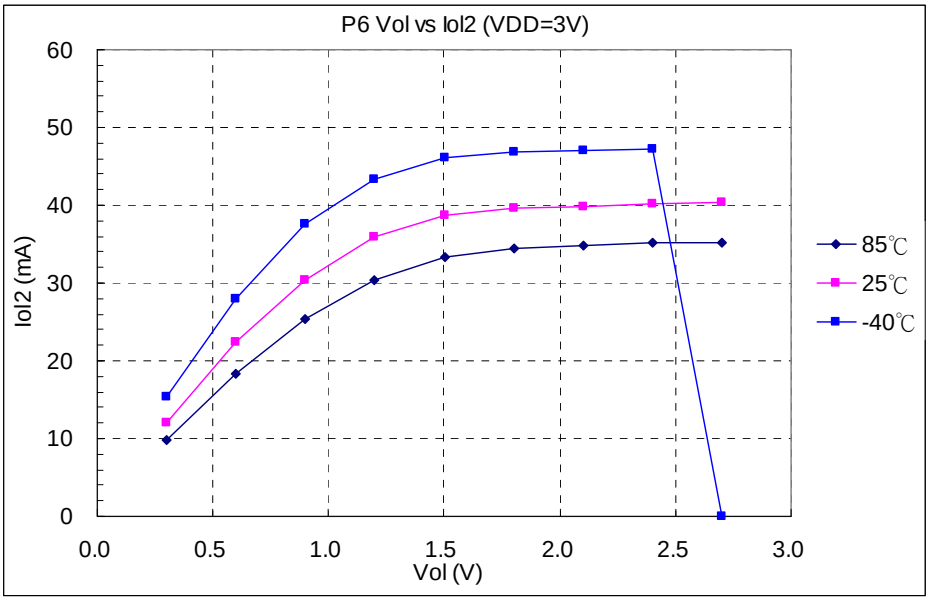


Figure 10-11 VOL of P6 vs. IOL, VDD=3V

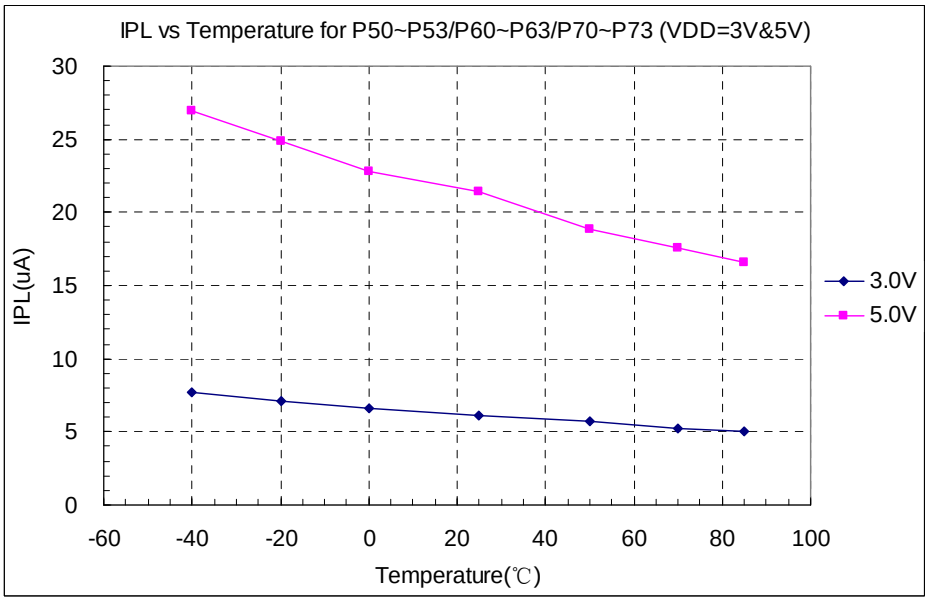


Figure 10-12 IPH of Port 6 & Port 7 vs. Temperature, VDD=3V & 5V

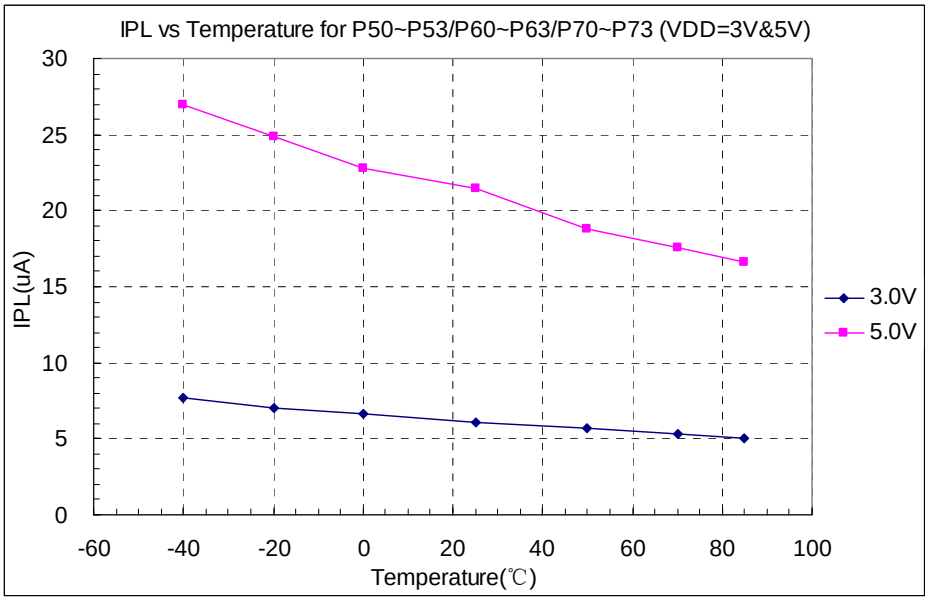


Figure 10-13 IPL of Ports 5 & 6 vs. Temperature, VDD=3V & 5V

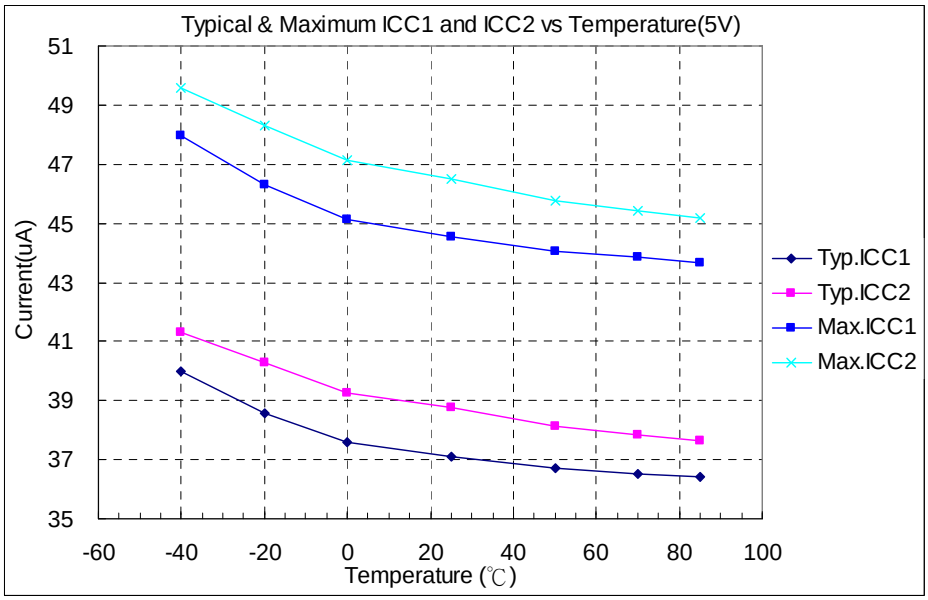


Figure 10-14 ICC1 and ICC2 vs. Temperature, VDD=5V

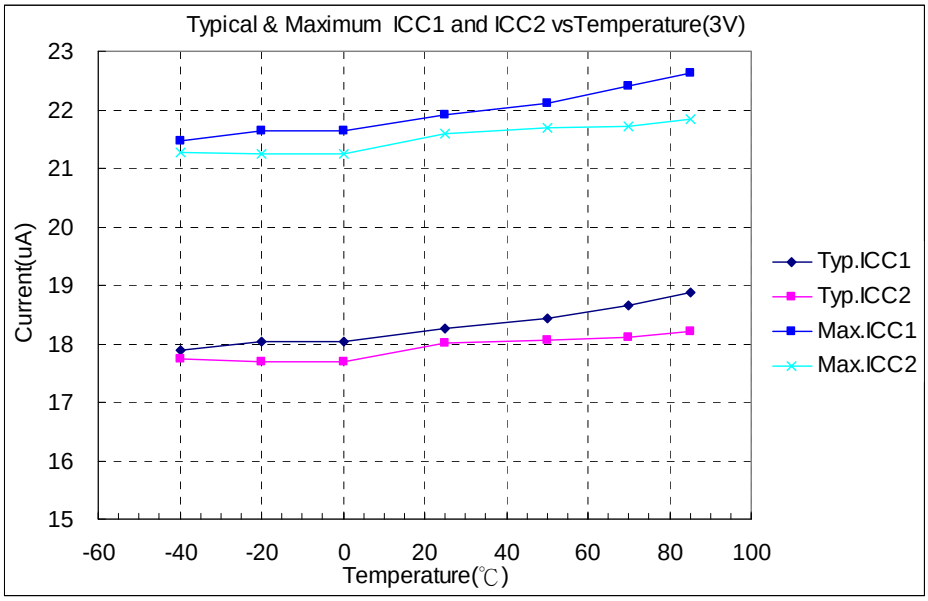


Figure 10-15 ICC1 and ICC2 vs. Temperature, VDD=3V

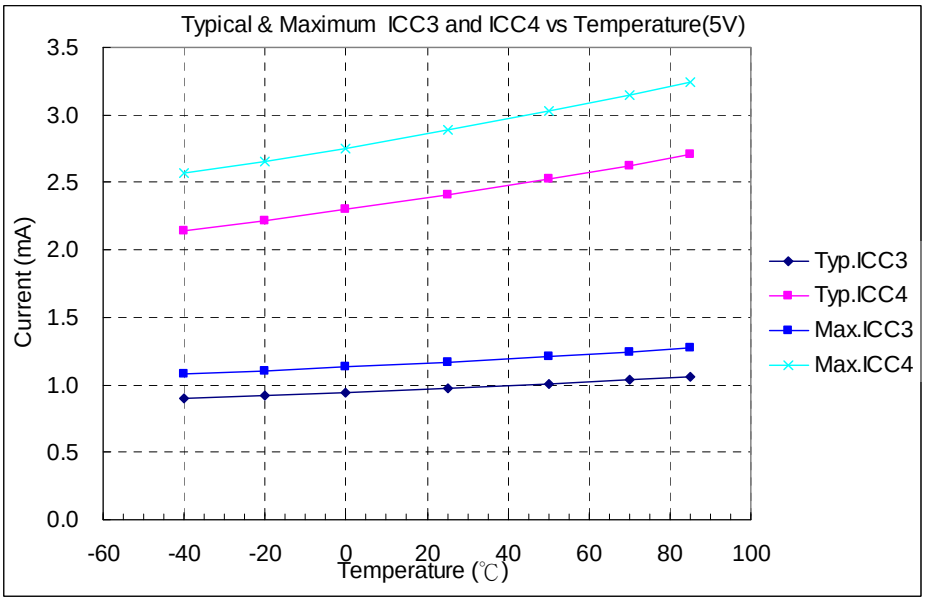


Figure 10-16 ICC3 and ICC4 vs. Temperature, VDD=5V

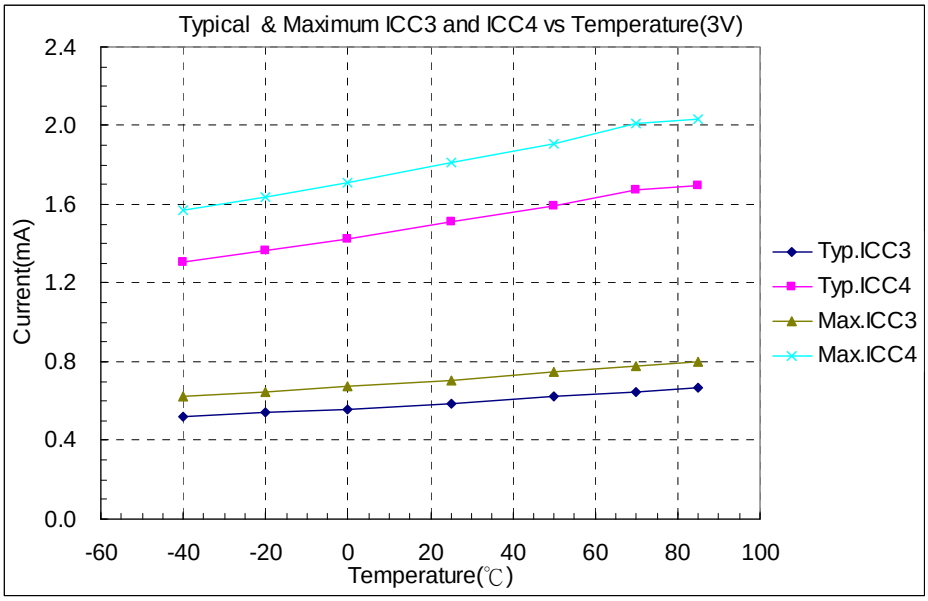


Figure 10-17 ICC3 and ICC4 vs. Temperature, VDD=3V

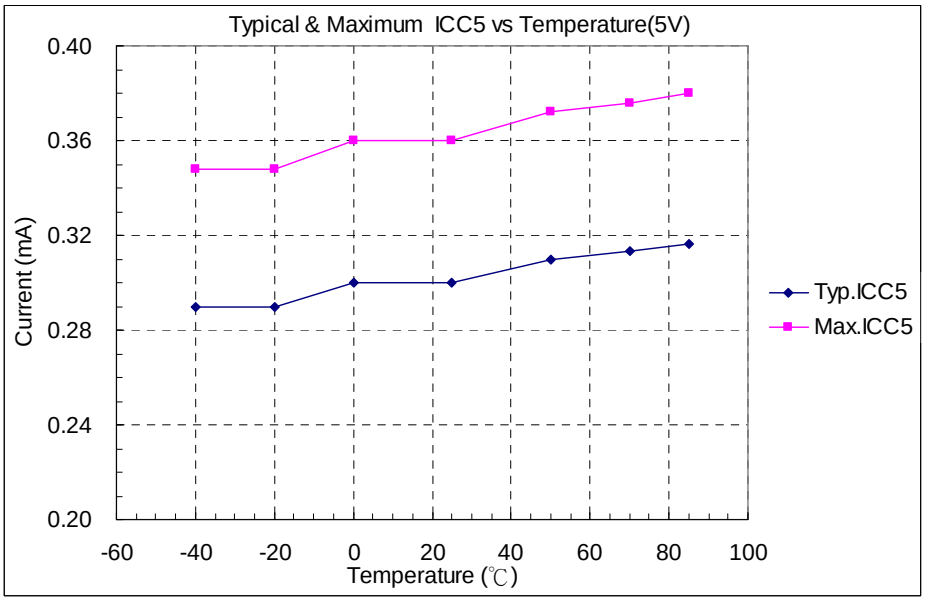


Figure 10-18 ICC5 vs. Temperature, VDD=5V

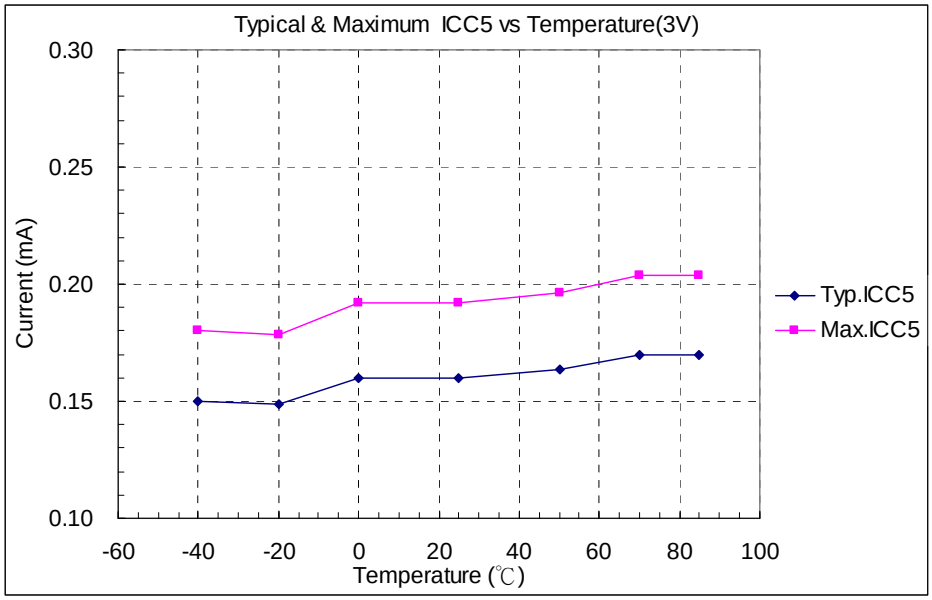


Figure 10-19 ICC5 vs. Temperature, VDD=3V

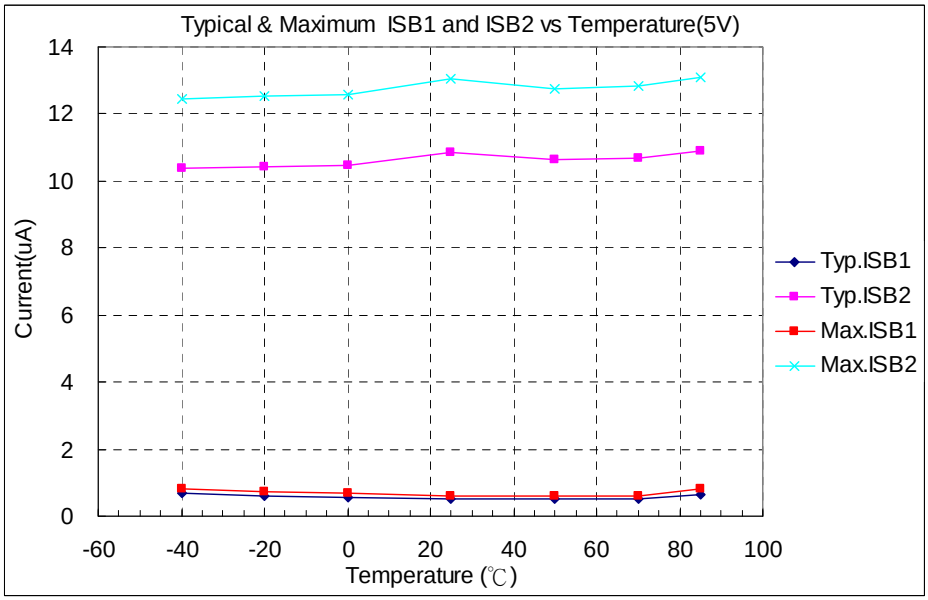


Figure 10-20 ISB1 and ISB2 vs. Temperature, VDD=5V

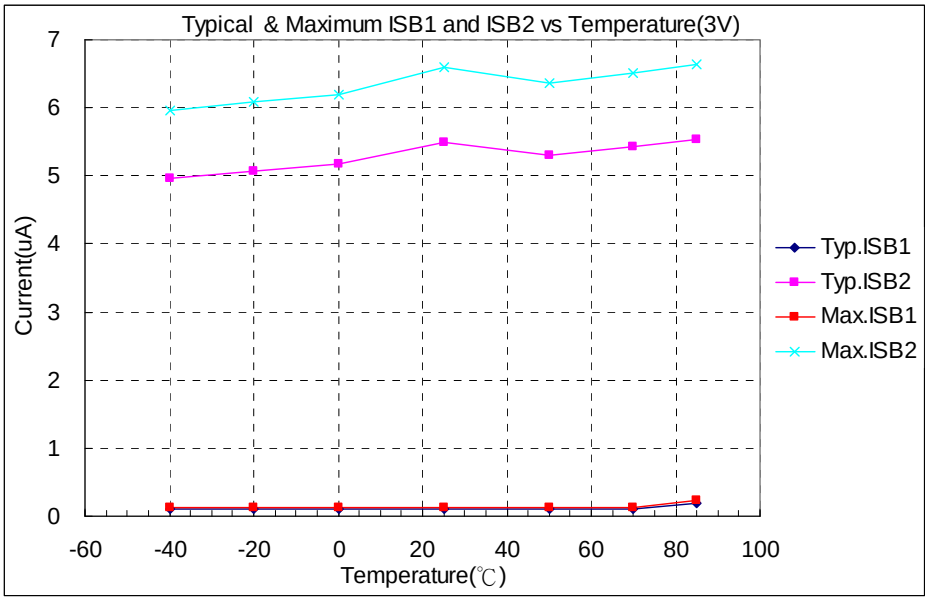


Figure 10-21 ISB1 and ISB2 vs. Temperature, VDD=3V

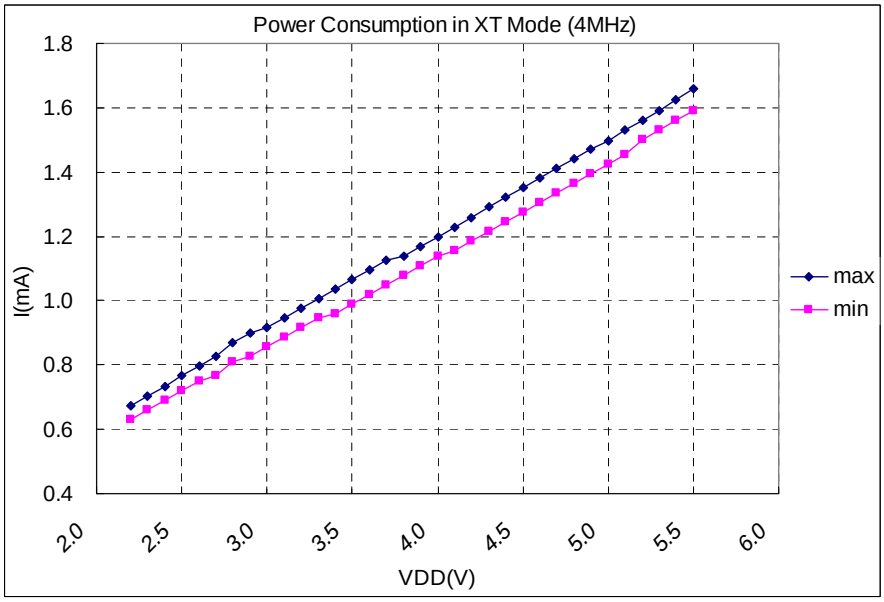


Figure 10-22 Power Consumption in HXT Mode (4MHz)

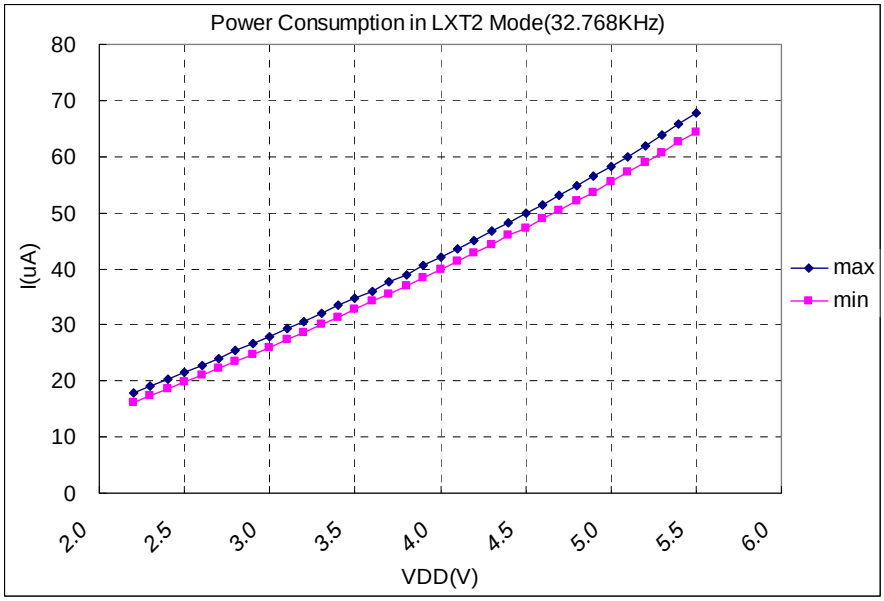


Figure 10-23 Power Consumption in LXT Mode (32765Hz)

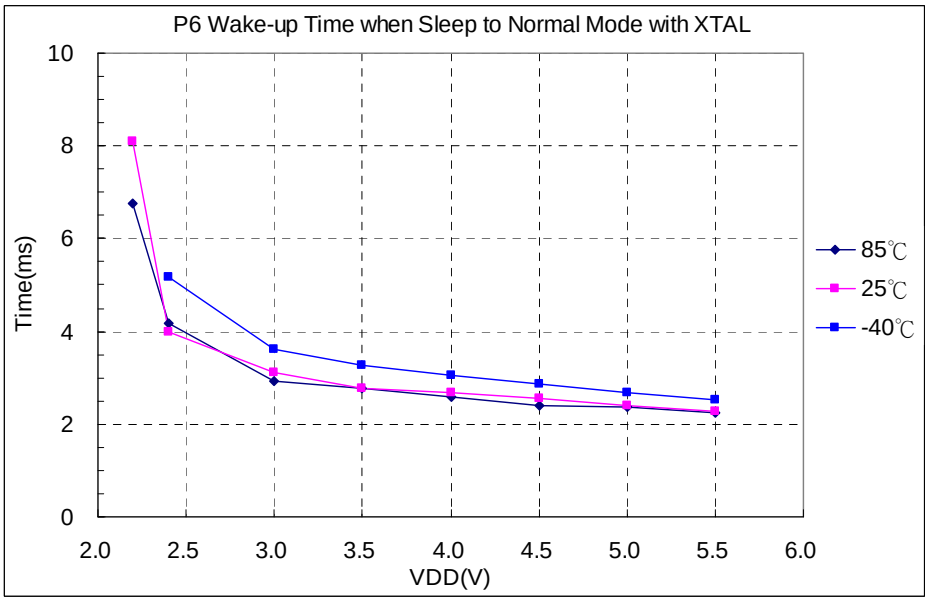


Figure 10-24 P6 Wake-up Time when Sleep to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

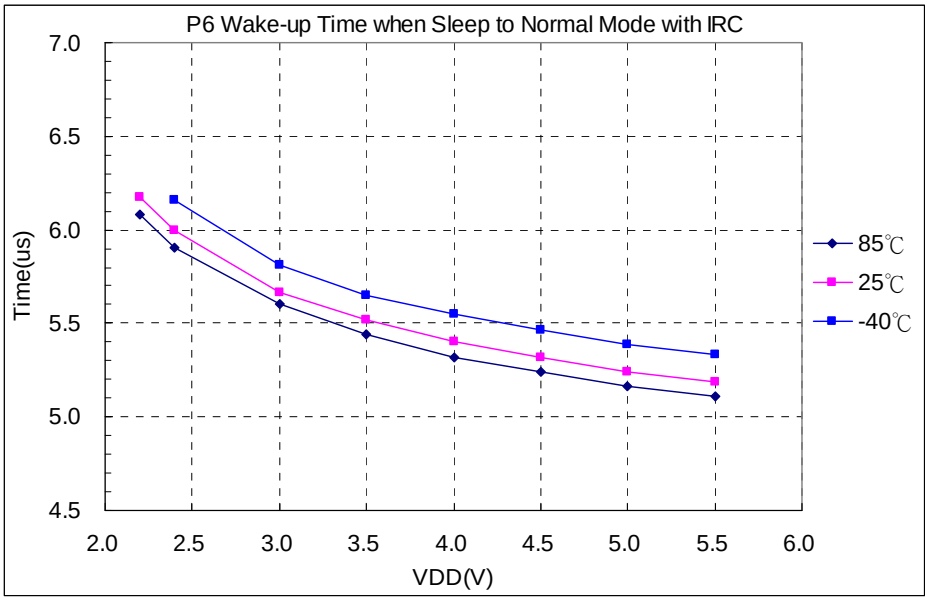


Figure 10-25 P6 Wake-up Time when Sleep to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

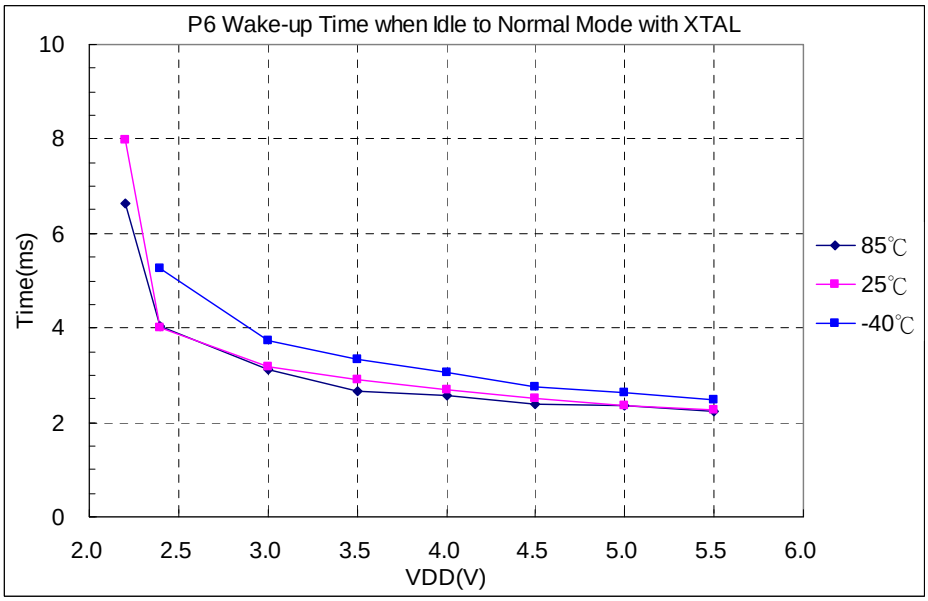


Figure 10-26 P6 Wake-up Time when Idle to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

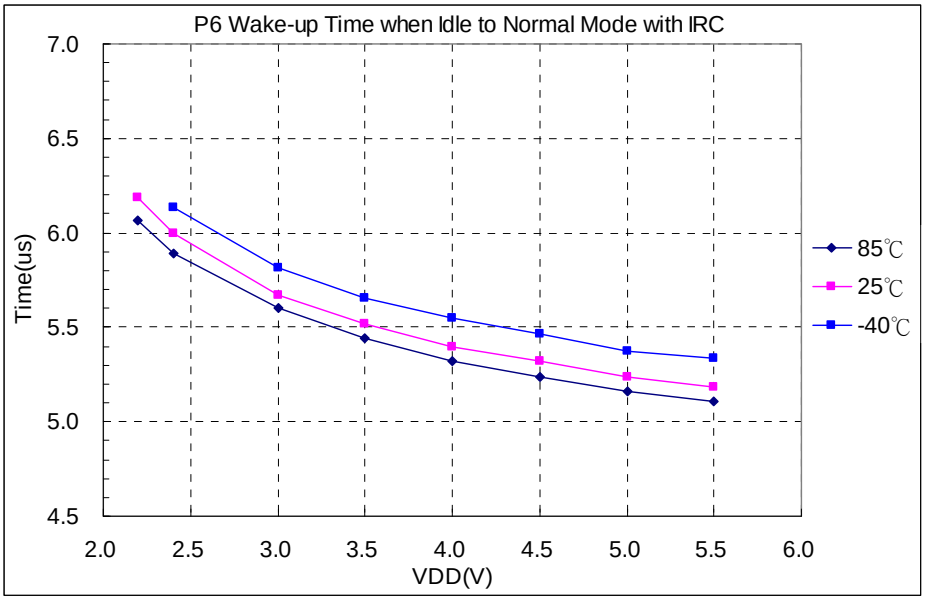


Figure 10-27 P6 Wake-up Time when Idle to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

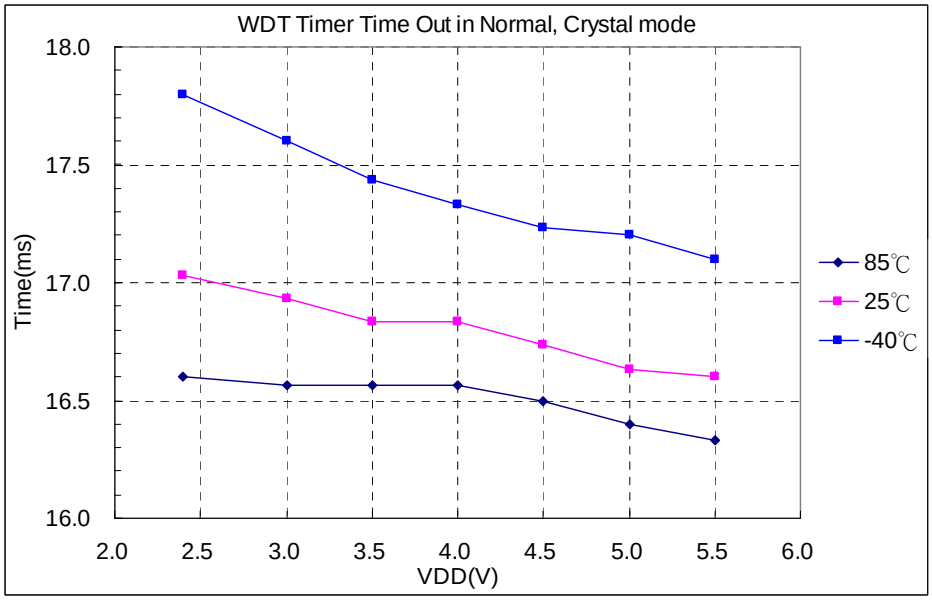


Figure 10-28 WDT Timer Time Out in Normal, Crystal Mode (Sub. Freq.=16kHz, 4 MHz)

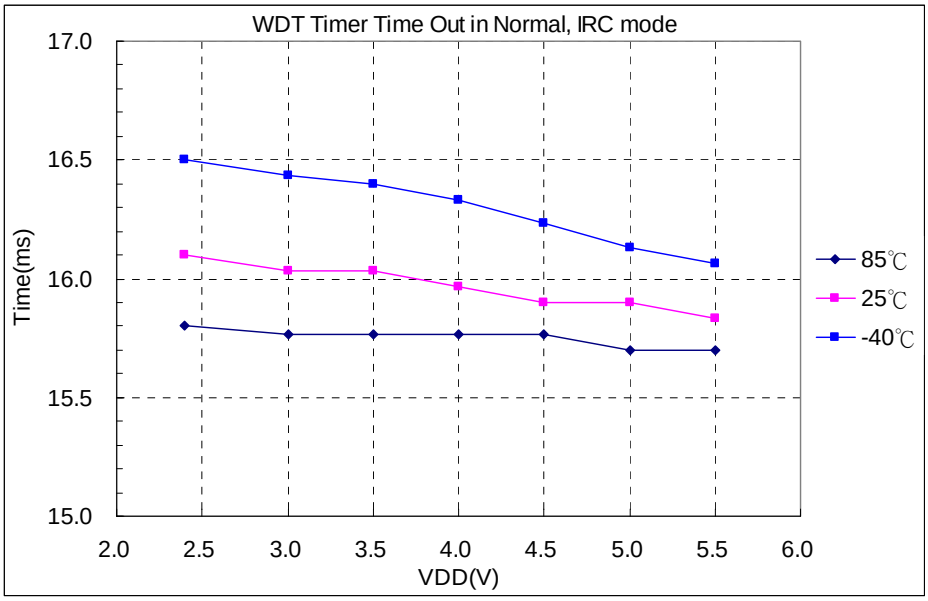


Figure 10-29 WDT Timer Time Out in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

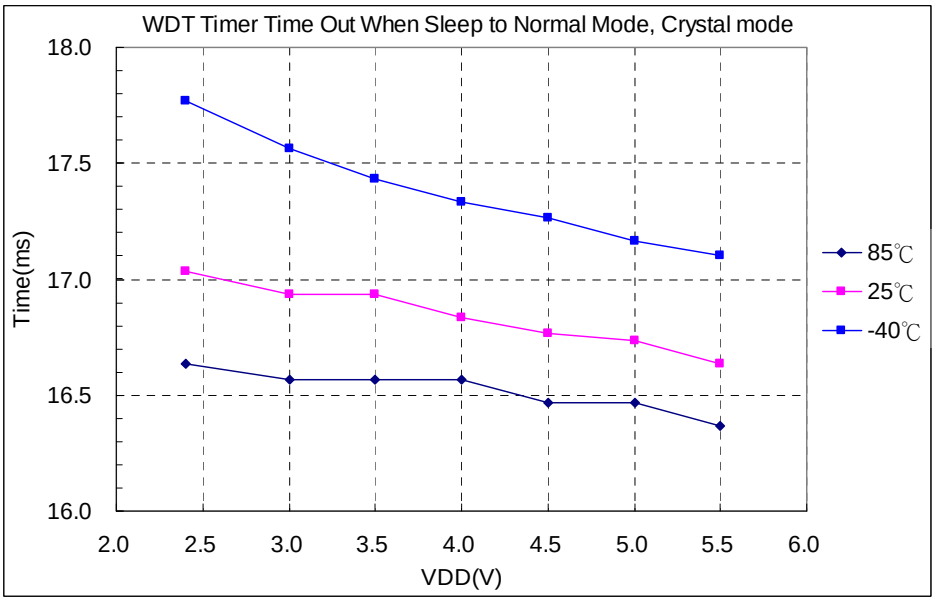


Figure 10-30 WDT Timer Time Out when Sleep to Normal, Crystal Mode (4MHz)

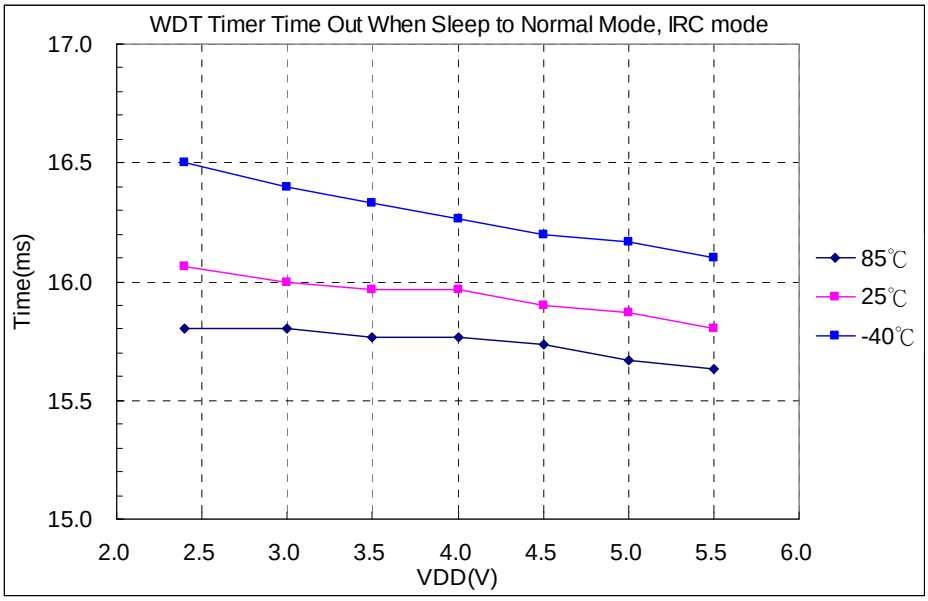


Figure 10-31 WDT Timer Time Out when Sleep to Normal, IRC Mode (4MHz)

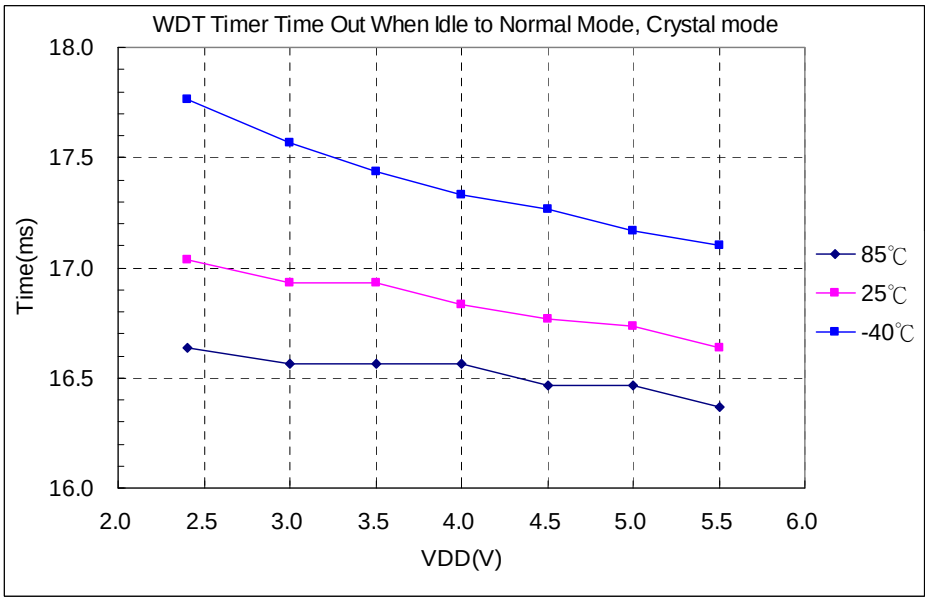


Figure 10-32 WDT Timer Time Out when Idle to Normal, Crystal Mode (4MHz)

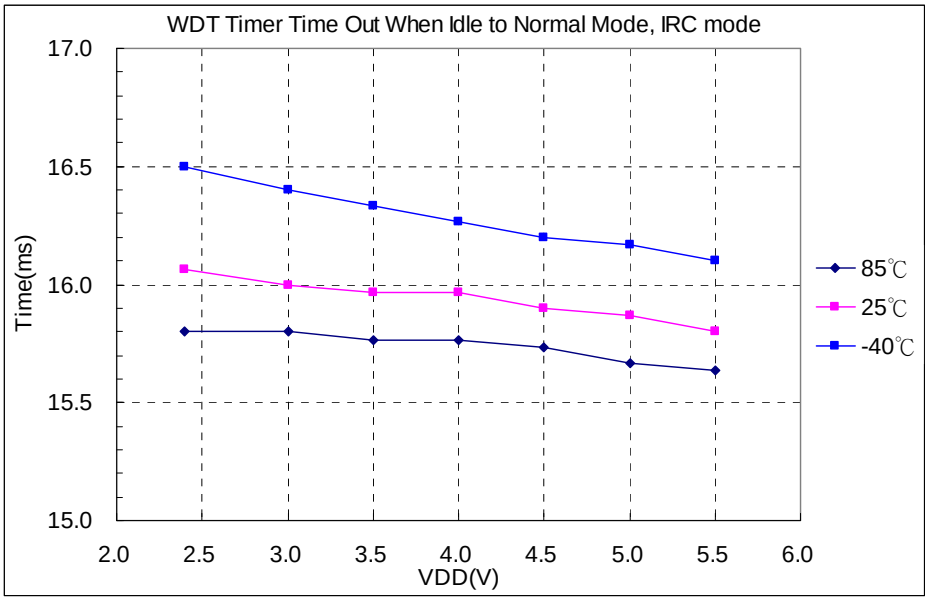


Figure 10-33 WDT Timer Time Out when Idle to Normal, IRC Mode (4MHz)

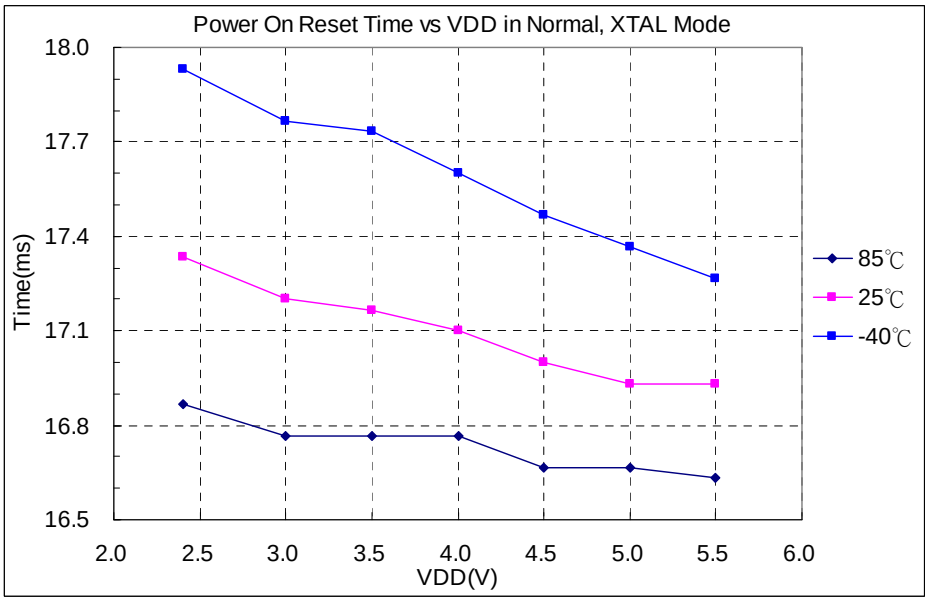


Figure 10-34 Power on Reset Time in Normal, Crystal Mode (Sub. Freq.=16kHz, 4 MHz)

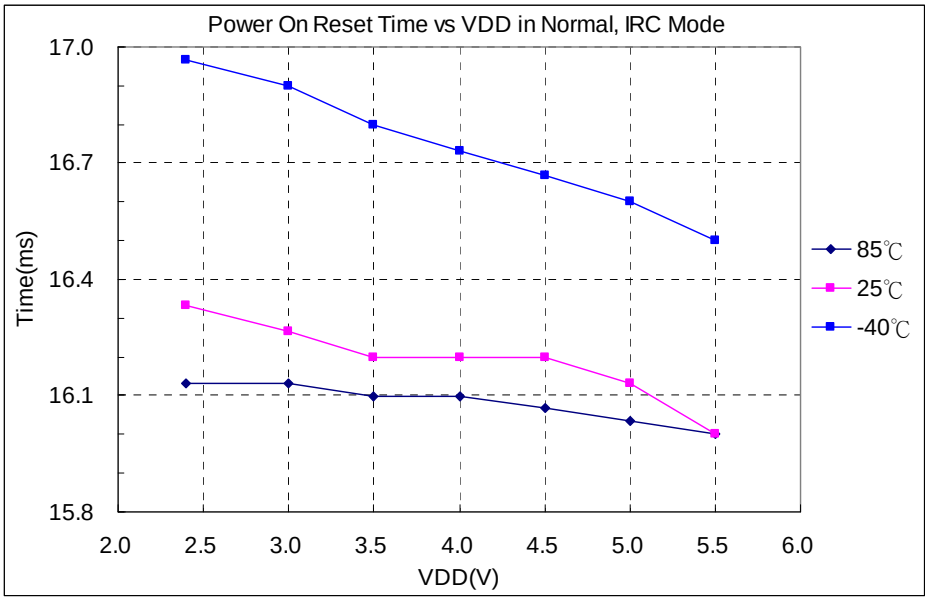


Figure 10-35 Power on Reset Time in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

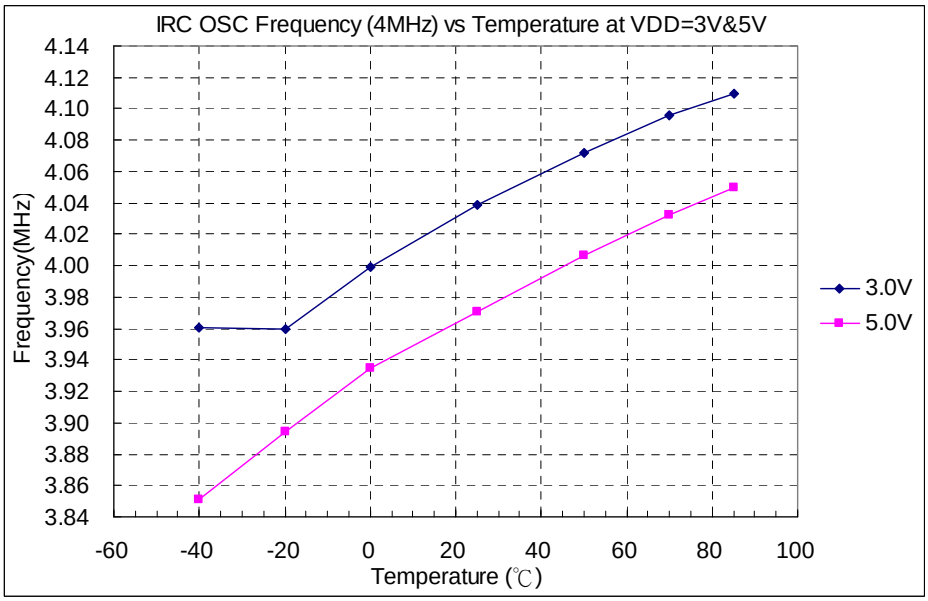


Figure 10-36 IRC OSC Freq, vs. Temp. (4MHz)

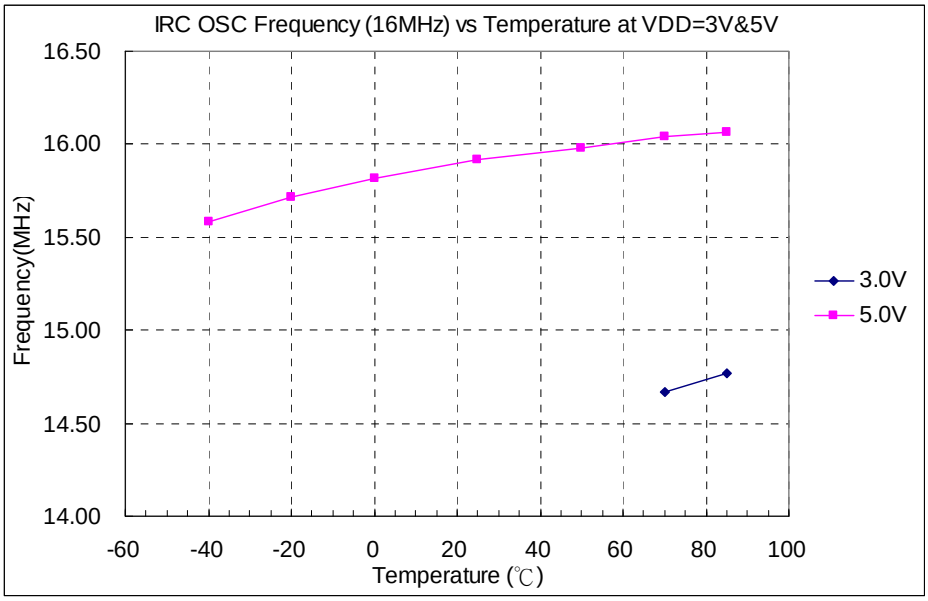


Figure 10-37 IRC OSC Freq, vs. Temp. (16MHz)

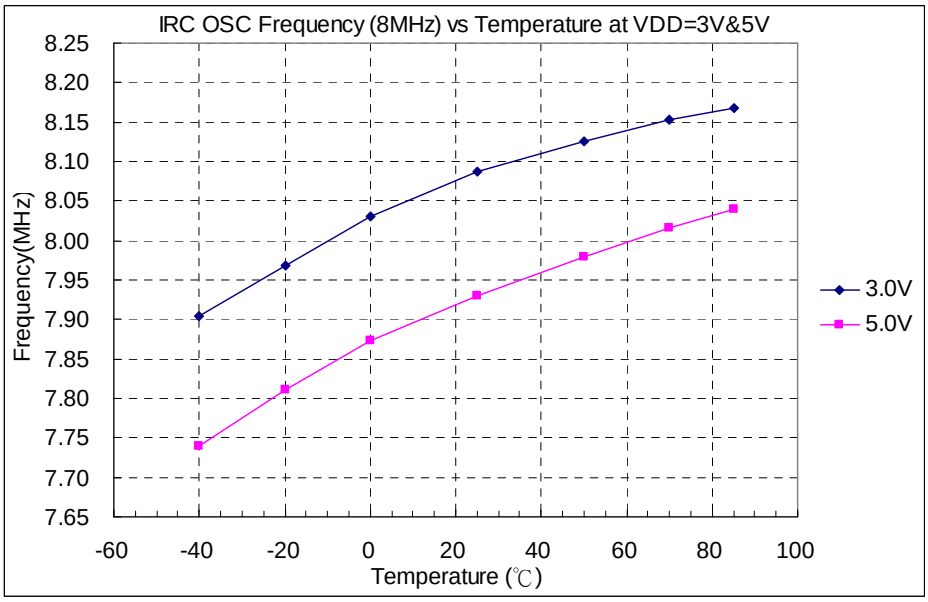


Figure 10-38 IRC OSC Freq, vs. Temp. (8MHz)

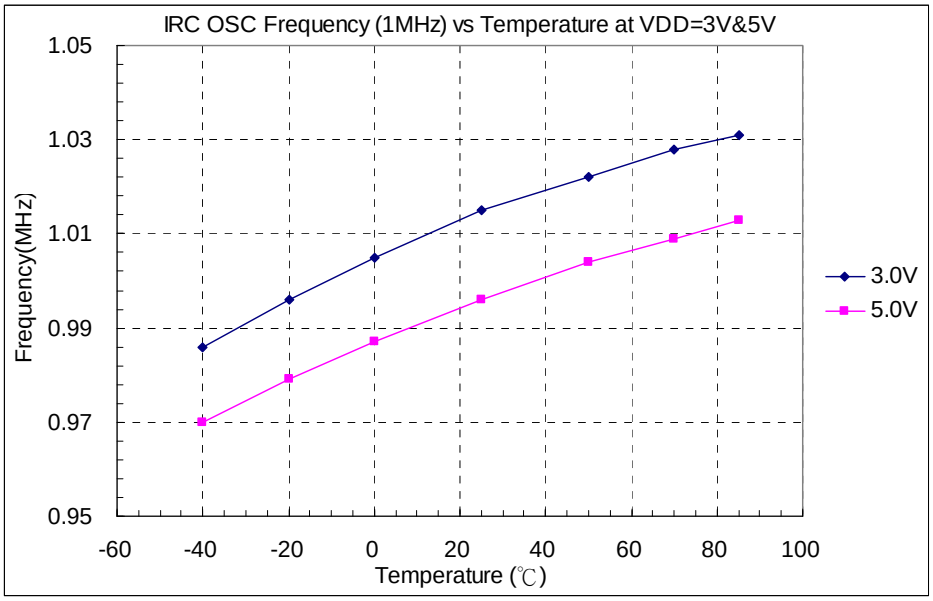


Figure 10-39 IRC OSC Freq, vs. Temp. (1MHz)

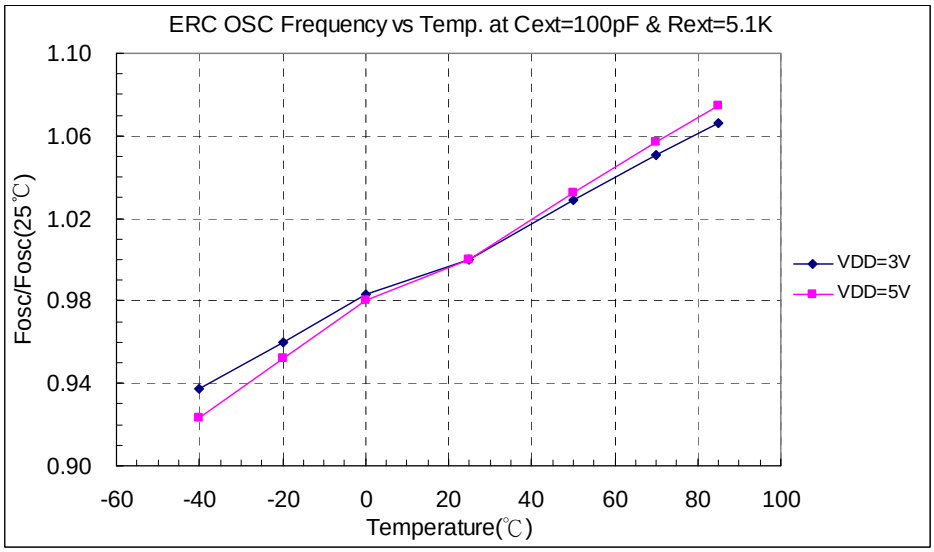


Figure 10-40 ERC OSC Frequency vs. Temp (CEXT=100pf, REXT=5.1k)

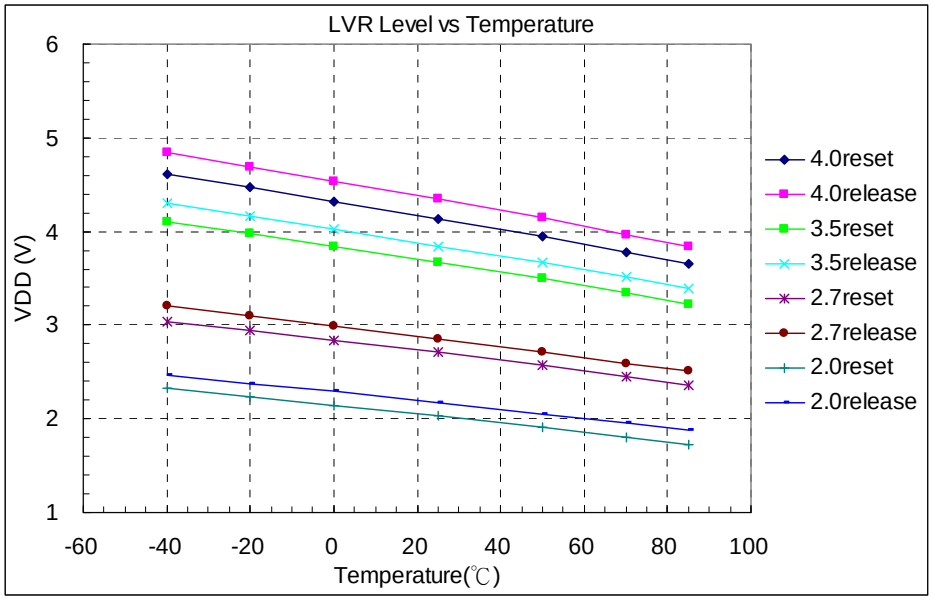


Figure 10-41 LVR Level vs Temperature

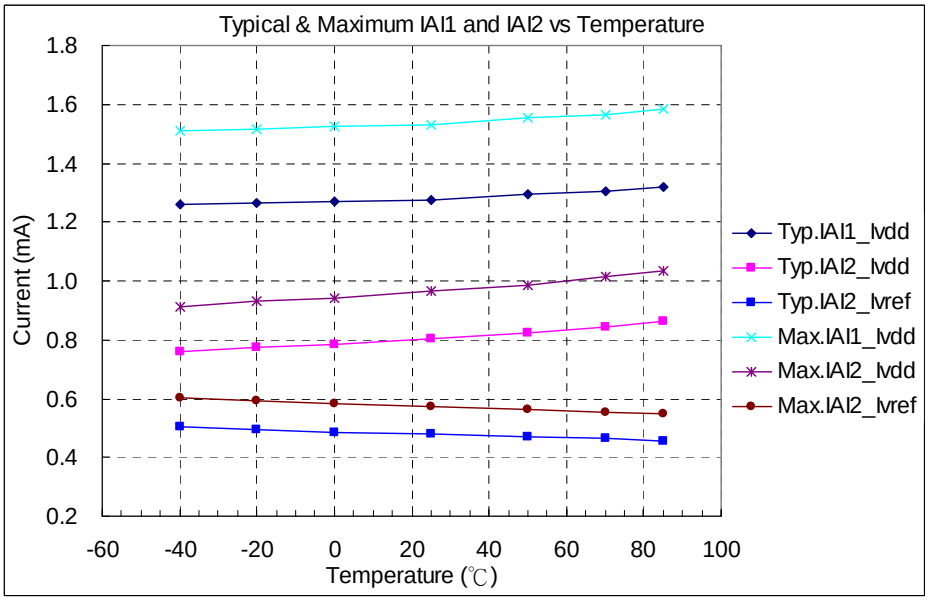


Figure 10-42 Typical & Maximum IAI1 and IAI2 vs Temperature

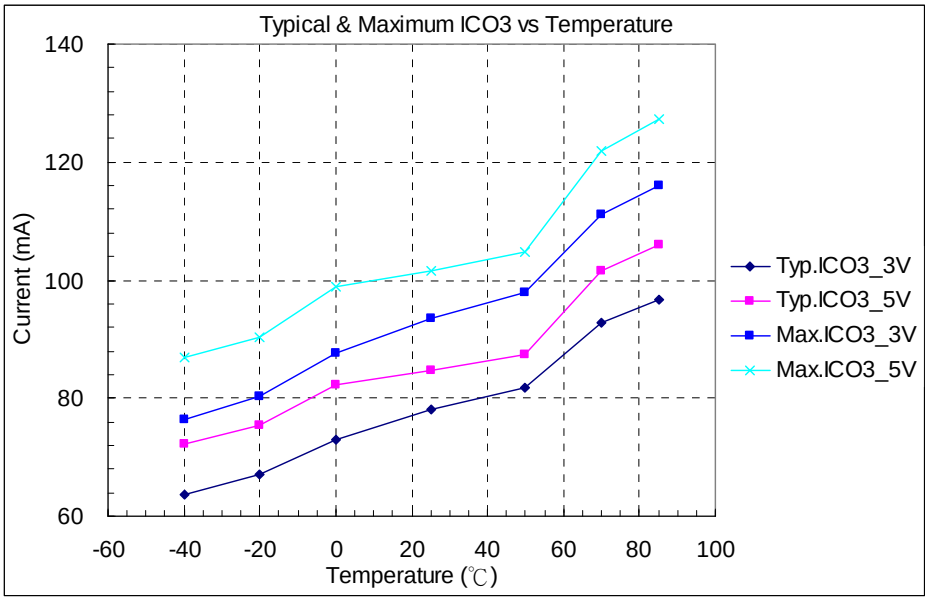


Figure 10-43 Typical & Maximum ICO3 vs Temperature

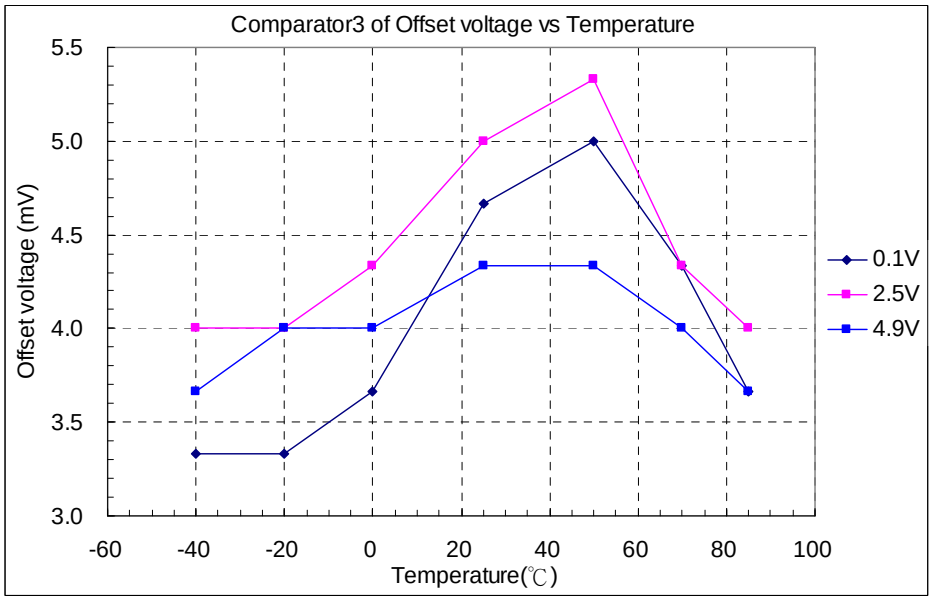


Figure 10-44 Comparator3 of Offset voltage vs Temperature

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
A96F902ND20	PDIP	20	300 mil
A96F902NSO20	SOP	20	300 mil
A96F902ND18	PDIP	18	300 mil
A96F902NSO18	SOP	18	300 mil
A96F902ND16	PDIP	16	300 mil
A96F902NSO16	SOP	16	300 mil

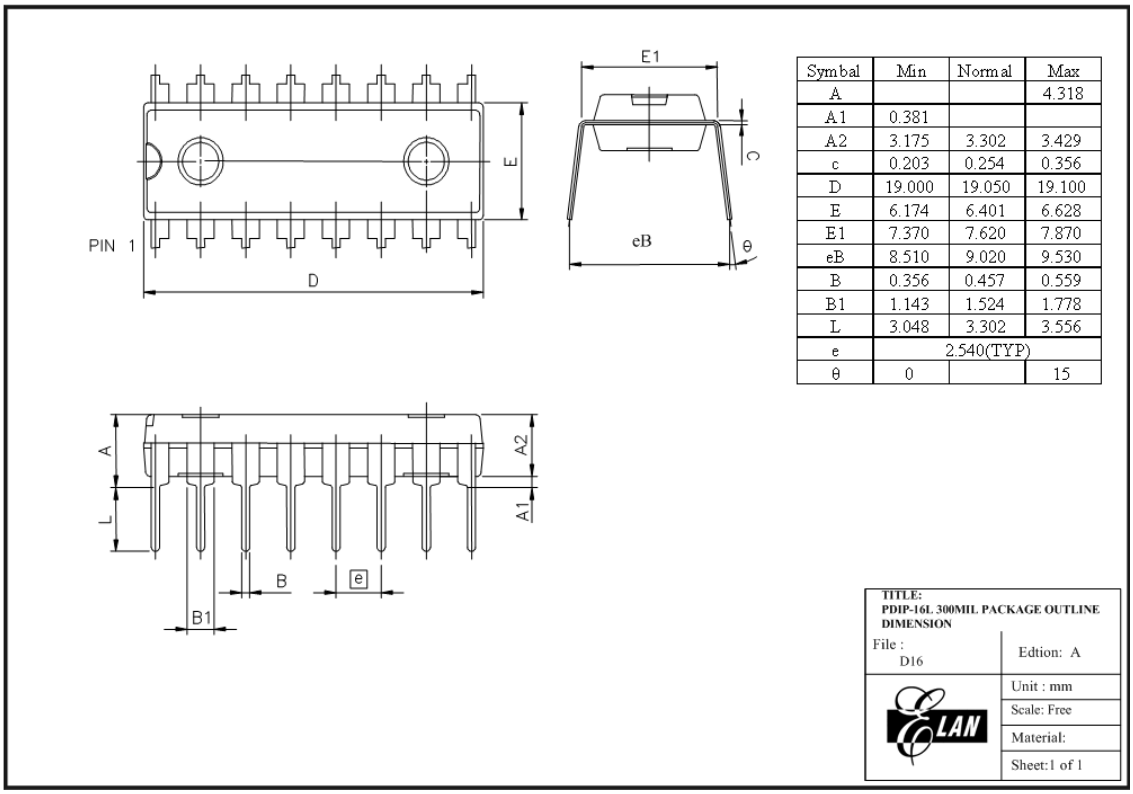
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents should be less than 100ppm and complies with Sony specifications.

Part No.	A96F902NS/J
Electroplate Type	Pure Tin
Ingredient (%)	Sn:100%
Melting Point (°C)	232°C
Electrical Resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 A96F902ND16 300mil



Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE:
PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION

File : D16 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-1 A96F902N 16-Pin PDIP Package Type

B.2 A96F902NSO16 300mil

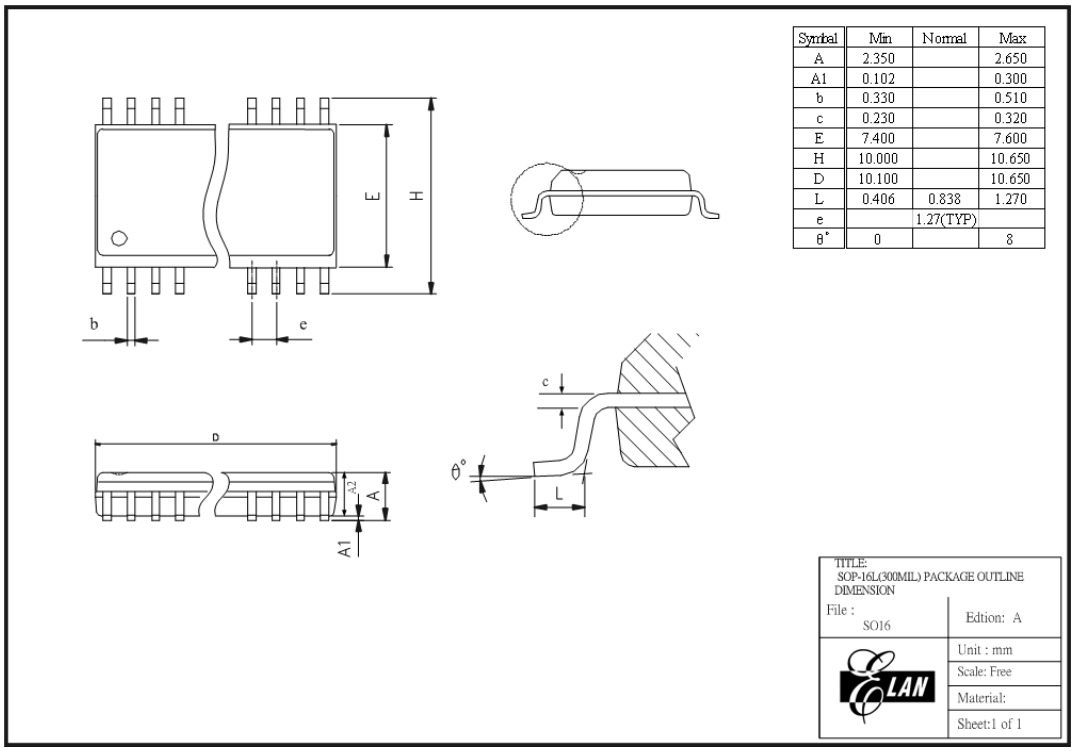
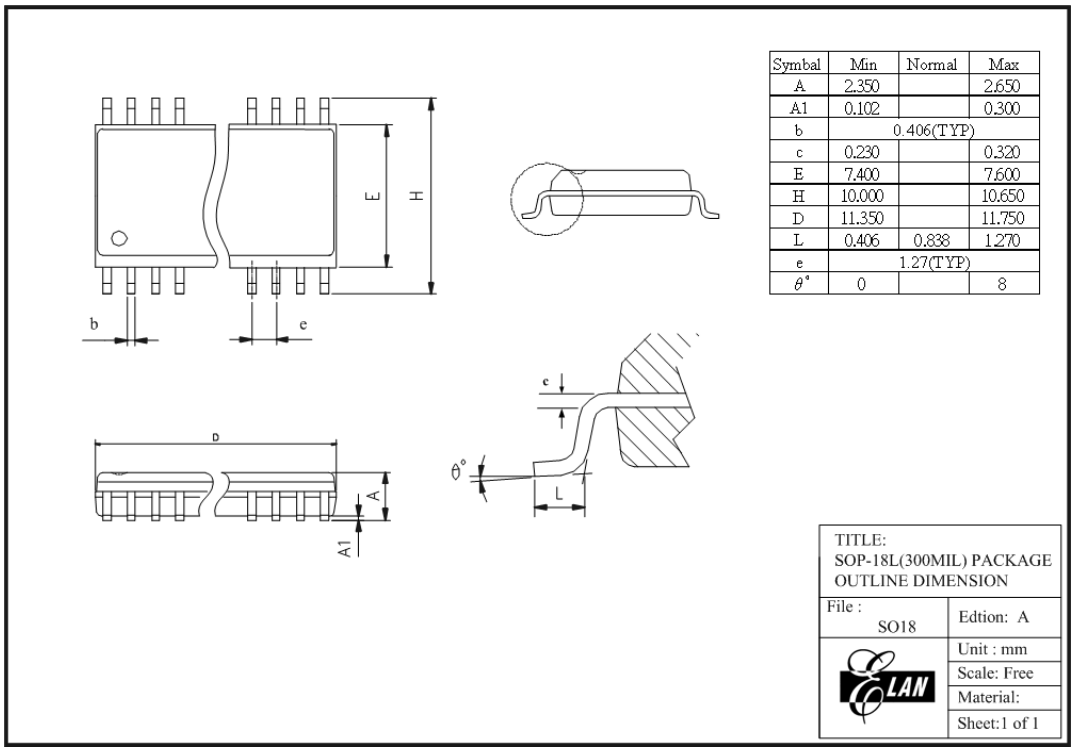


Figure B-2 A96F902N 16-Pin SOP Package Type

B.3 A96F902ND18 300mil

Figure B-3 A96F902N 18-Pin PDIP Package Type

B.4 A96F902NSO18 300mil



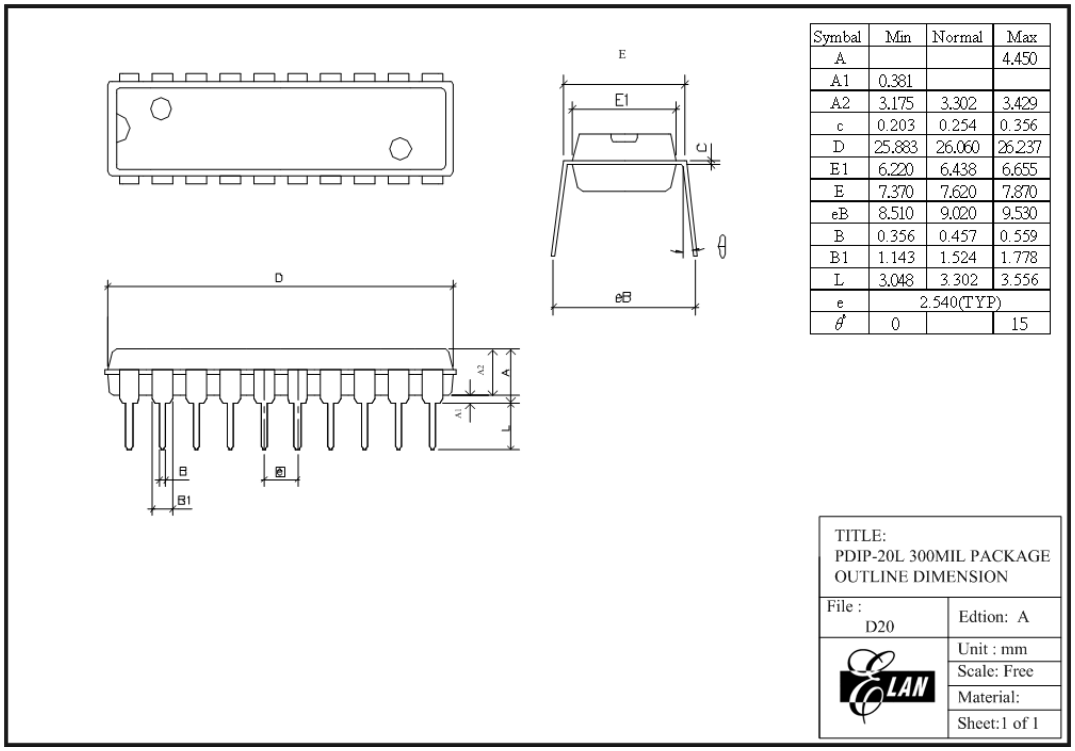
Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 A96F902N 18-Pin SOP Package Typ

B.5 A96F902ND20 300mil



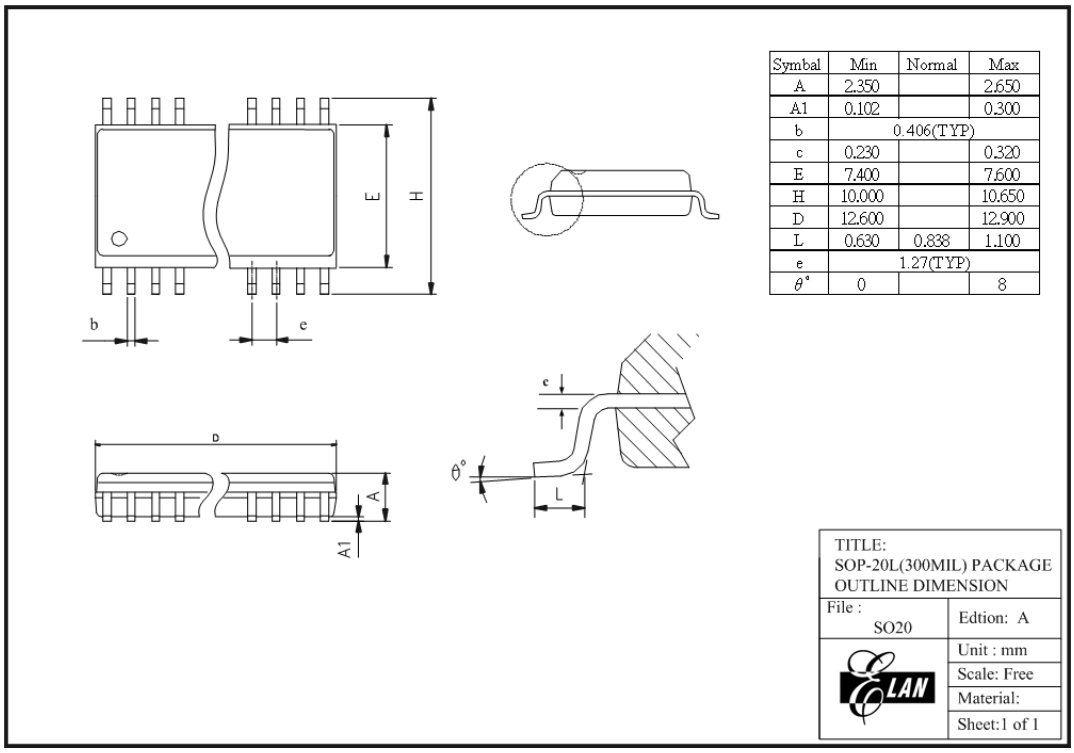
Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e		2.540(TYP)	
θ°	0		15

TITLE: PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION

File : D20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-5 A96F902N 20-Pin PDIP Package Type

B.6 A96F902NSO20 300mil



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-6 A96F902N 20-Pin SOP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-Condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature Cycle Test	–65°C (15mins)~150°C (15mins), 200 cycles	–
Pressure Cooker Test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High Temperature / High Humidity Test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-Temperature Storage Life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-Temperature Operating Life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

C.1 Address Trap Detect

An Address Trap Detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.