EM78F568N

8-BIT Microcontroller

Product Specification

DOC. VERSION 0.9

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2009/09/21

1 GENERAL DESCRIPTION

EM78F568N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is equipped with 8K*15-bits Electrical Flash Memory, two comparators, three 8 bits timers, one 16 bits timer, two 10 bits PWM, 8 channels AD with 12 bits resolution, SPI, UART and I2C.

With its Flash-ROM feature, the EN78F568N is able to offer a convenient way of developing and verifying users' programs. Moreover, users can take advantage of EMC Writer to easily program his development code.

2 FEATURES

- CPU configuration
  - **Support 8K×15** bits program ROM
  - **304×8** bits on chip registers (SRAM)
  - More than 10 years data retention
  - **8** level stacks for subroutine nesting
  - Less than 2 mA at 5V/4MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
  - Four operation mode

Mode	CPU	Main clock	WDT clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- I/O port configuration
  - 5 bidirectional I/O ports: P5, P6, P7, P8, P9
  - Pin change wake-up port : P6
  - **40** programmable pull-down I/O pins
  - **40** programmable pull-high I/O pins
  - **40** programmable open-drain I/O pins
  - **40** programmable high-sink/drive I/O pins
  - External interrupt : P60
- Operating voltage range:
  - 2.4V~5.5V at 0°C~70°C (commercial)
  - 2.6V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks):
  - Crystal mode:
    DC ~ 20MHz at 5V
    DC ~ 8MHz at 3V
    DC ~ 4MHz at 2.4V
  - ERC mode:
    DC ~ 20MHz at 5V
    DC ~ 8MHz at 3V
    DC ~ 4MHz at 2.4V
  - IRC mode
    DC ~ 16MHz at 4.5V~5.5V
    DC ~ 4MHz at 2.4V~5.5V
  - Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.2V~5.5V)	Process	Total
455kHz	±5%	±5%	±4%	±14%
4MHz	±5%	±5%	±4%	±14%
8MHz	±5%	±5%	±4%	±14%
16MHz	±5%	±5%	±4%	±14%

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Two Pulse Width Modulation (PWMA,B) with 10-bit resolution which shared with Timer A,B
  - Two 8 bits Timer/Counter:
    TC1: Timer/Counter/Capture mode selection
    TC3: Timer/Counter/PWM/PDO(programmable divider output)
    Mode selection
  - One 16 bits Timer/Counter:
    TC2: Timer/Counter/Window mode selection
  - 4 programmable Level Voltage Detector (LVD): Vdd power monitor and support low voltage detector interrupt flag
  - **8** channels Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - One pair of comparator
  - Serial transmitter/receiver interface (SPI): three wire synchronous communication
  - Universal asynchronous receiver transmitter interface (UART): two wire asynchronous communication
  - Power-down (Sleep) mode
  - High EFT immunity(4MHZ,4clocks)
  - I2C function with 7/10 bits address & 8 bits data transmit/receive mode
- 19 available interrupts(5 external, 14 internal)
  - External interrupt(P60)
  - TCC overflow interrupt
  - TC1,TC2, TC3 overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - ADC completion interrupt
  - PWMA, PWMB period match completion
  - Comparator 1/2 high/low interrupt
  - I2C transfer/receive/stop interrupt
  - UART TX, RX , RX error interrupt
  - SPI interrupt
  - LVD interrupt
- Programmable free running Watchdog Timer
  - Watchdog Timer: 16.5ms ± 5% with Vdd =5V at 25°C, Temperature range ± 5% (-40°C ~+85°C)
  - Watchdog Timer: 18ms ± 5% with Vdd = 3V at 25°C Temperature range ± 5% (-40°C~+85°C)
  - Two clocks per instruction cycle
- Package Type:
  - 44 pin QFP: EM78F568NQ44J/S
  - 40 pin DIP: EM78F568ND40J/S
  - 28 pin DIP: EM78F568ND28J/S
  - 28 pin SKDIP: EM78F568NK28J/S
  - 28 pin SOP: EM78F568NSO28J/S

  Note: Green products do not contain hazardous substances.
- 99.9% single instruction cycle commands
- There are 4 kinds of oscillation ranges in crystal mode

Crystal ranges	Oscillator Mode
20MHz~6MHz	HXT
6MHz~1MHz	XT
1MHz~100KHz	LXT1
32.768KHz	LXT2

3 PIN CONFIGURATIONS

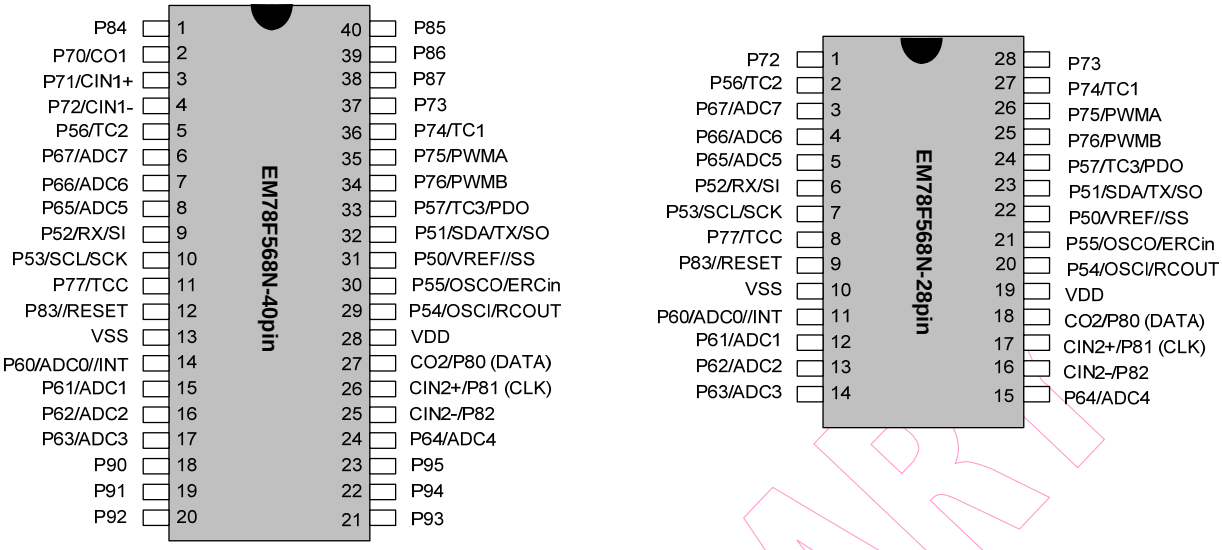


Fig 1-1 40 pin DIP & 28 pin DIP/SKDIP/SOP pin assignment

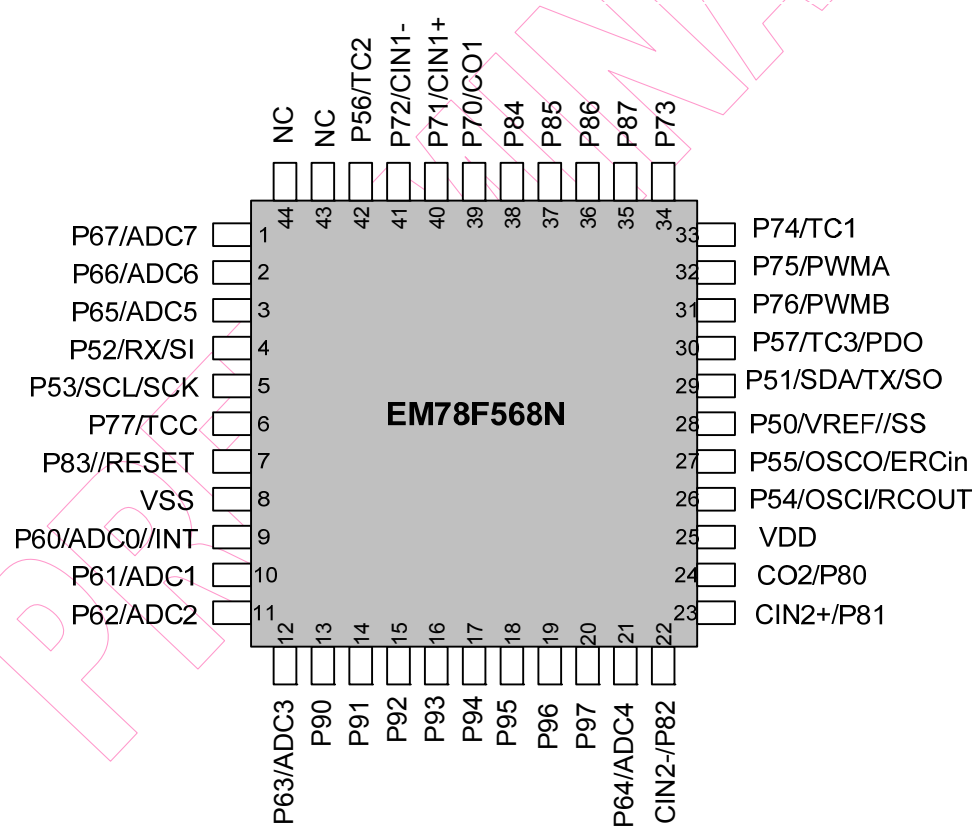


Fig 1-2 44 pin QFP pin assignment

4 PIN DESCRIPTIONS

Table 1 EM78F568N 40 pin DIP pin description

Symbol	Pin No.	Type	Function
OSCI	29	I	External clock crystal resonator RC oscillator input pin.
OSCO	30	I/O	Clock output from internal oscillator
/RESET	12	I	Schmitt trigger input pin. If this pin remains logic low, the controller is reset.
TCC	11	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
P60~P63 P64 P65~P67	14~17 24 8~6	I/O	P60~P67 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
ADC0~ADC3 ADC4 ADC5~ADC7	14~17 24 8~6	I	Analog to Digital Converter input pins
P50~P51 P52~P53 P54~P55 P56 P57	31~32 9~10 29~30 5 33	I/O	P50~P57 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
CIN1-,CIN1+, CO1 CIN2-,CIN2+, CO2	4,3,2 25,26,27	I	CINX- → the Vin- input pins of the comparators. CINX+ → the Vin+ input pins of the comparators. COX → the output of the comparator.
PWMA, PWMB	35, 34	O	Pulse width modulation outputs.
/SS,SCK,SO,SI	31,10,32,9	I,I/O,I,O	SPI serial clock input/output (/SCK). SPI serial data input (SI) SPI serial data output (SO) SPI slave mode enable (/SS)
TX,RX	32,9	O,I	UART data transmit output (TX). UART data receive input (RX).
VREF	31	I	External reference voltage for ADC
/INT	14	I	External interrupt pin triggered by falling or rising edge(set by EIESCR).
TC1	36	I	8-bit timer/counter 1(TC1)
TC2	5	I,O	16-bit timer/counter 2(TC2) or programmable divider output (PDO).
TC3/PDO	33	I	8-bit timer/counter 3(TC3)
P70~P72 P73~P76 P77	2~4 37~34 11	I/O	P70 ~P77 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
P80~P82 P83 P84 P85~P87	27~25 12 1 40~38	I/O	P80 ~P87 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
P90~P92 P93~P95	18~20 21~23	I/O	P90 ~P97 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
VSS	13	-	Ground.
VDD	28	-	Power supply pin.
SCL	10	I/O	I2C serial clock
SDA	32	I/O	I2C serial data

Table 2 EN78F568N 44 pin QFP pin description

Symbol	Pin No.	Type	Function
OSCI	26	I	External clock crystal resonator RC oscillator input pin.
OSCO	27	I/O	Clock output from internal oscillator
/RESET	7	I	Schmitt trigger input pin. If this pin remains logic low, the controller is reset.
TCC	6	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
P60~P63 P64 P65~P67	9~12 21 3~1	I/O	P60~P67 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
ADC0~ADC3 ADC4 ADC5~ADC7	9~12 21 3~1	I	Analog to Digital Converter input pins
P50~P51 P52~P53 P54~P55 P56 P57	28~29 4~5 26~27 42 30	I/O	P50~P57 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
CIN1-,CIN1+, CO1 CIN2-,CIN2+, CO2	41,40,39 22,23,24	I	CINX- → the Vin- input pins of the comparators. CINX+ → the Vin+ input pins of the comparators. COX → the output of the comparator.
PWMA, PWMB	32, 31	O	Pulse width modulation outputs.
/SS,SCK,SO,SI	28,5,29,4	I,I/O,I,O	SPI serial clock input/output (/SCK). SPI serial data input (SI) SPI serial data output (SO) SPI slave mode enable (/SS)
TX,RX	29,4	O,I	UART data transmit output (TX). UART data receive input (RX).
VREF	28	I	External reference voltage for ADC
/INT	9	I	External interrupt pin triggered by falling or rising edge(set by EIESCR).
TC1	33	I	8-bit timer/counter 1(TC1)
TC2	42	I,O	16-bit timer/counter 2(TC2) or programmable divider output (PDO).
TC3/PDO	30	I	8-bit timer/counter 3(TC3)
P70~P72 P73~P76 P77	39~41 34~31 6	I/O	P70 ~P77 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
P80~P82 P83 P84 P85~P87	24~22 7 1 38~35	I/O	P80 ~P87 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
P90~P97	13~20	I/O	P90 ~P97 are bi-directional I/O ports. All can be pulled-down and pulled-high internally by software control. They also can open drain and enable high sink/drive mode by software control.
VSS	8	-	Ground.
VDD	25	-	Power supply pin.
SCL	5	I/O	I2C serial clock
SDA	29	I/O	I2C serial data

5 FUNCTIONAL BLOCK DIAGRAM

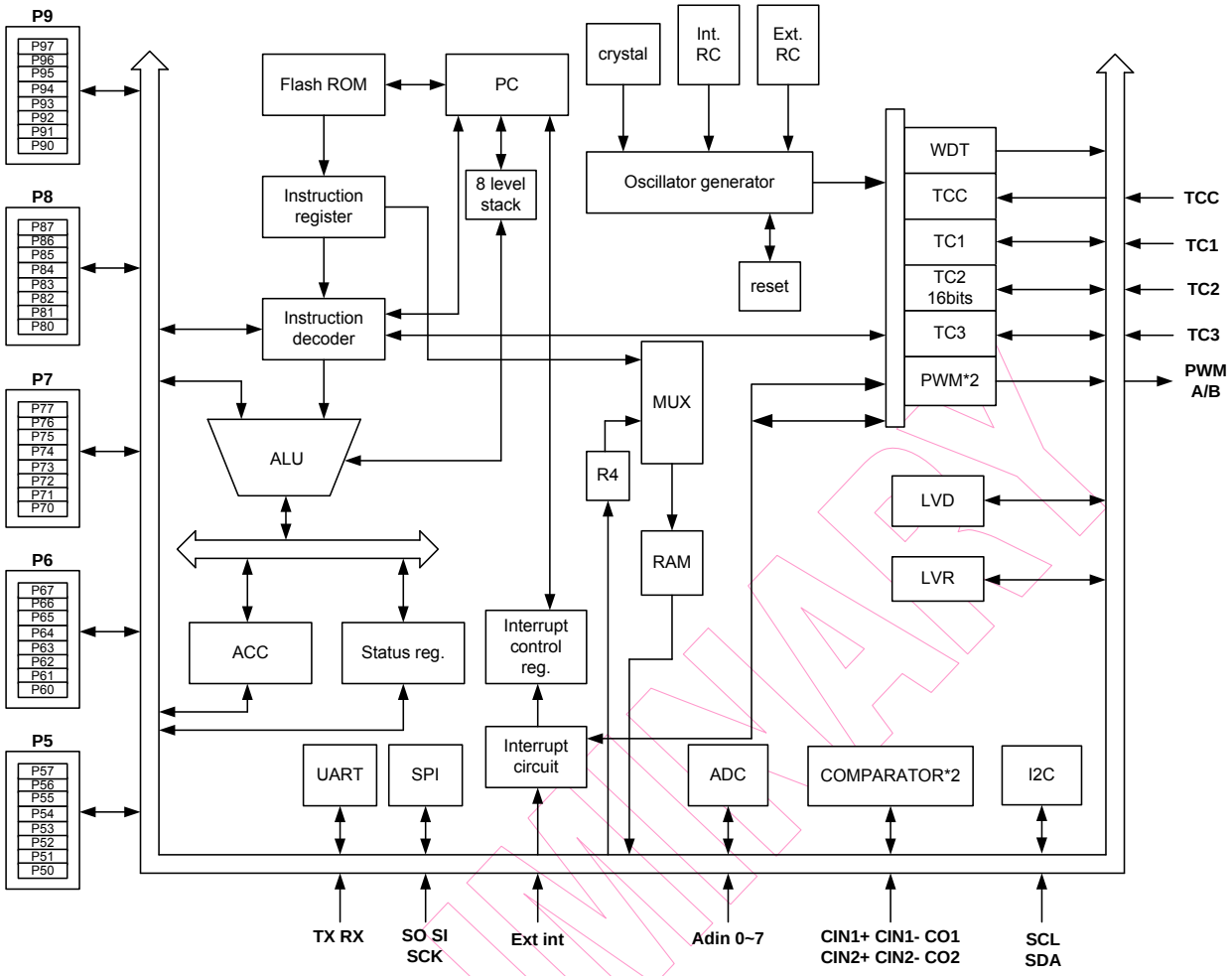


Fig. 2 Function Block Diagram

6 FUNCTION DESCRIPTIONS

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	SBS0	0	0	0	GBS0

Bits 7~5: no used bits, fixed 0 all the time.

Bit 4(SBS0): special register bank select bit. It is used to select bank 0/1 of special register R5~R4F.

0: Bank 0

1: Bank 1

Bits 3~1: no used bits, fixed 0 all the time.

Bit 0(GBS0): general register bank select bit. It is used to select Bank 0/1of general register R80~RFF.

0: Bank 0

1: Bank 1

6.1.3 R2: PC (Program Counter)

- Depending on the device type, R2 and hardware stack are 12-bits wide. The structure is depicted in Fig.3.
- Generating 8K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 8K (213).

- "LCALL" instruction loads the lower 13 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 8K (213).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.
- Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6",·····) will cause the ninth bit and the above bits (A8~A11) of the PC not change.
- All instruction are single instruction cycle (fclk/2,fclk/4,fclk/8,fclk/16). The instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

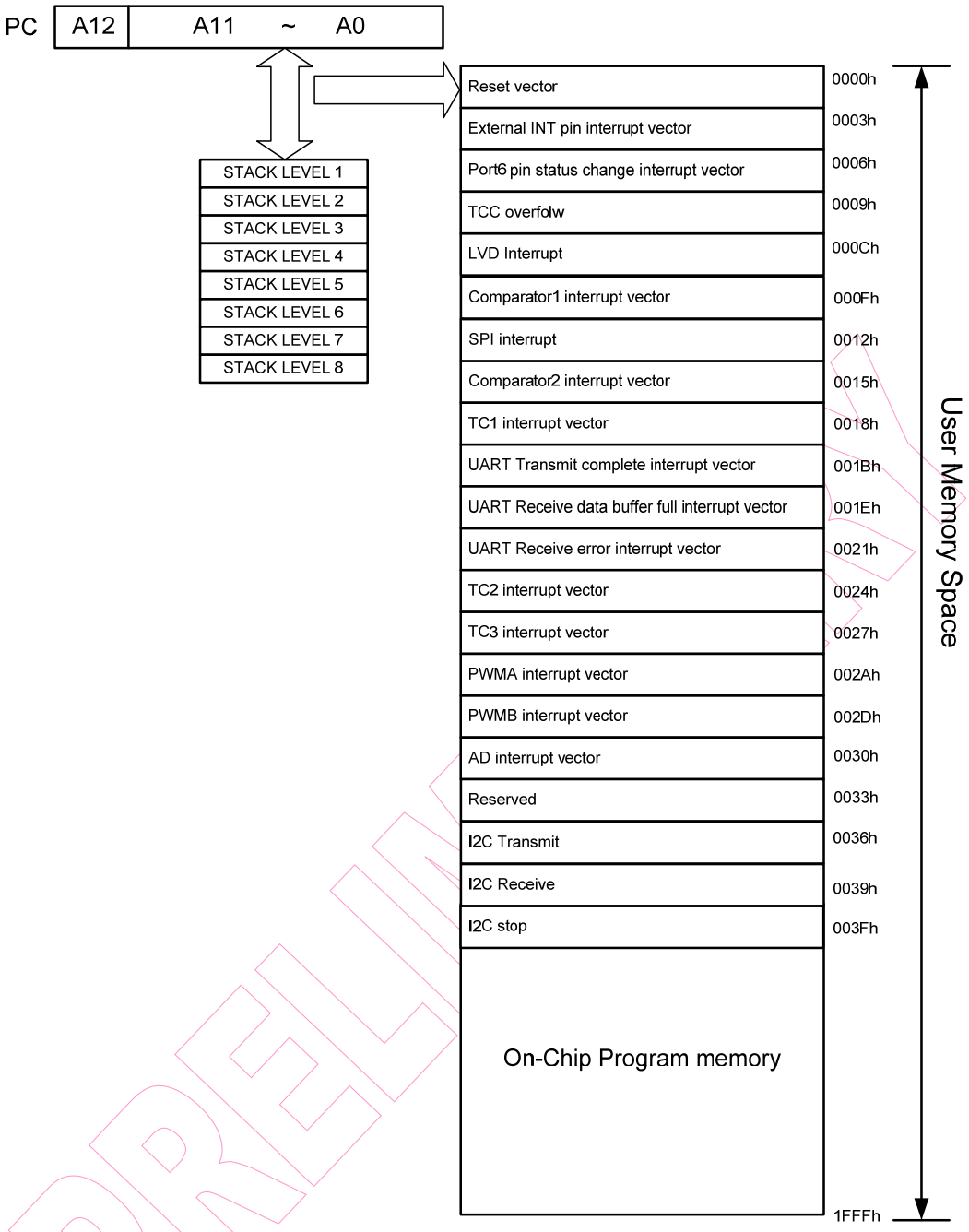


Fig. 3 Program Counter Organization

Address	BANK 0	BANK 1
0X00	IAR (Indirect Addressing Reg.)	
0X01	BSR (Bank Selection Control Reg.)	
0X02	PC (program counter)	
0X03	SR (Status Reg.)	
0X04	RSR (RAM Selection Reg.)	
0X05	Port 5	P5PHCR
0X06	Port 6	P6PHCR
0X07	Port 7	P7PHCR
0X08	Port 8	P8PHCR
0X09	Port 9	P9PHCR
0X0A	-	-
0x0B	OMCR (Operating Mode Control Reg.)	P5PLCR
0X0C	ISR1 (Interrupt Status Reg. 1)	P6PLCR
0X0D	ISR2 (Interrupt Status Reg. 2)	P7PLCR
0X0E	ISR3 (Interrupt Status Reg. 3)	P8PLCR
0X0F	-	P9PLCR
0X10	EIESCR	-
0X11	WDTCR	P5HD/SCR
0X12	LVDCR	P6HD/SCR
0X13	TCCCR	P7HD/SCR
0X14	TCCDATA	P8HD/SCR
0X15	IOCR5	P9HD/SCR
0X16	IOCR6	-
0X17	IOCR7	P5ODCR
0X18	IOCR8	P6ODCR
0X19	IOCR9	P7ODCR
0X1A	-	P8ODCR
0X1B	-	P9ODCR
0X1C	IMR1 (Interrupt Mask Reg. 1)	-
0X1D	IMR2 (Interrupt Mask Reg. 2)	IRCS
0X1E	IMR3 (Interrupt Mask Reg. 3)	-
0X1F	-	-
0X20	P5WUCR	-
0X21	P5WUECR	-
0X22	P7WUCR	-

0X23	P7WUECR	I2CCR1(I2C status and control reg. 1)
0X24	ADCR1 (ADC Control Reg. 1)	I2CCR2(I2C status and control reg. 2)
0X25	ADCR2 (ADC Control Reg. 2)	I2CSA(I2C slave address reg.)
0X26	ADICL (ADC Input Select Low Byte Reg.)	I2CDA(I2C device address reg.)
0X27	-	I2CDB(I2C data buffer)
0X28	-	I2CA
0X29	ADDH (AD Data High 8-bits Reg.)	-
0X2A	ADDL (AD Data Low 4-bits Reg.)	PWMER(PWM Enable Control Reg.r)
0x2B	SPICR (SPI Control Reg.)	TIMEN(Timer/PWM Enable Control Reg.)
0X2C	SPIS (SPI Status Reg.)	-
0X2D	SPIR (SPI Read Buffer)	-
0X2E	SPIW (SPI Write Buffer)	-
0X2F	WUCR1	PWMACR(PWM A control reg.)
0X30	-	PWMBCR(PWM B control reg.)
0X31	-	-
0X32	URCR1 (UART Control Reg. 1)	TACR(Timer A control reg.)
0X33	URCR2 (UART Control Reg. 2)	TBCR(Timer B control reg.)
0X34	URS (UART Status Register)	-
0X35	URRD (UART Receive Data Buffer Reg.)	TAPRD(Timer A Period buffer)
0X36	URTD (UART Transmit Data Buffer Reg.)	TBPRD(Timer B Period buffer)
0X37	TBPTL	-
0X38	TBPTH	TADT(Timer A Duty Buffer)
0X39	CMP1CR(Comparator 1 Control Reg.)	TBDT(Timer B Duty Buffer)
0X3A	-	-
0x3B	-	PRDxL
0X3C	CMP2CR	DTxL
0X3D	-	-
0X3E	-	-
0X3F	-	-
0X40	-	-
0X41	-	-
0X42	-	-
0X43	CPIRLCON	-
0X44	-	-
0X45	-	-
0X46	-	-
0X47	-	-

0X48	TC1CR	-
0X49	TCR1DA	-
0X4A	TCR1DB	-
0x4B	TC2CR	-
0X4C	TCR2DH	-
0X4D	TCR2DL	-
0X4E	TC3CR	-
0X4F	TCR3D	-
0X50	GENERAL PURPOSE REGISTER	
0X51		
. .		
0X7F		
0X80	BANK 0	BANK 1
0X81		
. . .		
0XFE		
0XFF		

Fig. 4 Data Memory Configuration

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	T	P	Z	DC	C

Bits 7~5: no used bits, fixed 0 all the time.

Bit 4(T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3(P): Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2(Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1(DC): Auxiliary carry flag

Bit 0(C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 7~0(RSR7~RSR0): these bits are used to select registers (address: 00~FF) in the indirect address mode. Users can see the configuration of the data memory more detail in Fig. 4.

6.1.6 Bank0 R5 ~ R9 (Port 5 ~ Port 9)

R5, R6, R7, R8 and R9 are I/O data registers.

6.1.7 Bank0 RA (Unused)

6.1.8 Bank0 RB OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	0

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator for WDT internal RC time base

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will decide SLEP instruction which mode to go.

0: "IDLE=0"+SLEP instruction => sleep mode

1: "IDLE=1"+SLEP instruction => idle mode

CPU operation mode

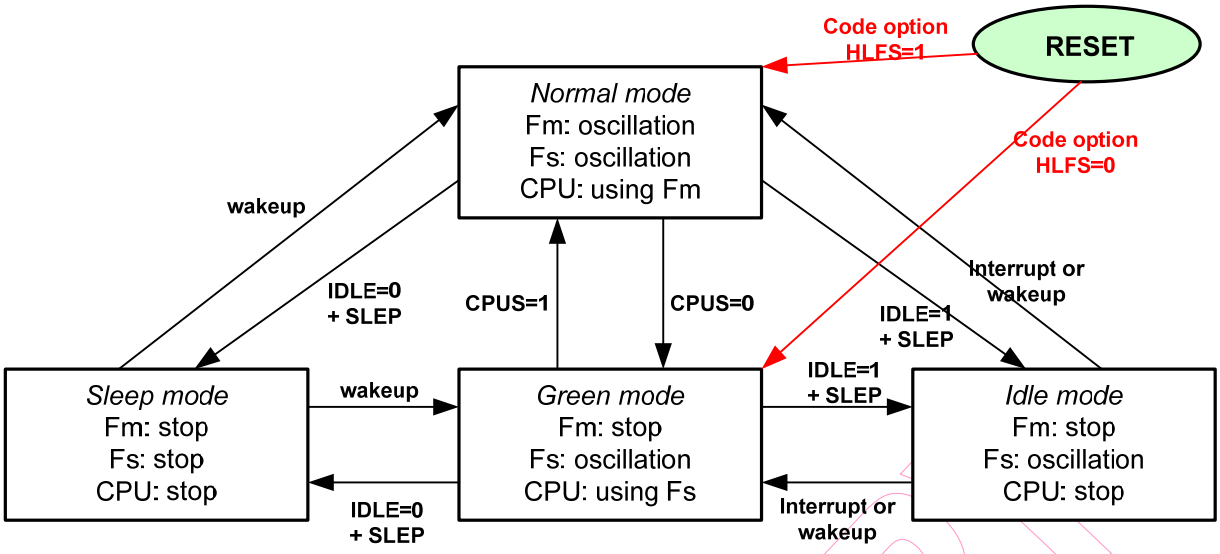


Fig. 5 CPU operation mode

Bit 5(TC1SS): TC1 clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 4(TC2SS): TC2 clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 3(TC3SS): TC3 clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 2(TASS): Timer A clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 1(TBSS): Timer B clock source select bit

0: the Fs is used as Fc

1: the Fm is used as Fc

Bit 0: not used bit, fixed to “0” all the time.

6.1.9 Bank0 RC: ISR1 (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

"1" means interrupt request, and "0" means no interrupt occurs.

Bit 7(LVDIF): Low Voltage Detector interrupt flag.

When LVD1, LVD0 = "0,0", Vdd > 2.3V, LVDIF is "0", Vdd<= 2.3V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "0,1", Vdd > 3.3V, LVDIF is "0", Vdd<= 3.3V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1,0", Vdd > 4.0V, LVDIF is "0", Vdd<= 4.0V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1,1", Vdd > 4.5V, LVDIF is "0", Vdd<= 4.5V, set LVDIF to "1". LVDIF reset to "0" by software.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bit 5 (SPIF): SPI mode interrupt flag. flag cleared by software.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 2 (EXIF): External interrupt flag.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

6.1.10 Bank0 RD: ISR2 (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF

Bit 7 (CMP2IF): Comparator2 interrupt flag. Set when a change occurs in the output of Comparator2, reset by software.

Bit 6 (CMP1IF): Comparator1 interrupt flag. Set when a change occurs in the output of Comparator1, reset by software.

Bit 5(TC3IF): 8-bit timer/counter 3 interrupt flag. interrupt flag cleared by software.

Bit 4 (TC2IF): 16-bit timer/counter 2 interrupt flag. interrupt flag cleared by software.

Bit 3 (TC1IF): 8-bit timer/counter 1 interrupt flag. interrupt flag cleared by software.

Bit 2 (UERRIF): UART receiving error interrupt, cleared by software or UART disable.

Bit 1 (RBFF): UART receive mode data buffer full interrupt flag. flag cleared by software.

Bit 0 (TBEF): UART transmit mode data buffer empty interrupt flag. flag cleared by software.

6.1.11 Bank0 RE: ISR3 (Interrupt Status Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	**I2CSTPIF**	0	I2CRIF	I2CTIF

Bits 7~4: not used bits, fixed to "0" all the time.

Bit 3(I2CSTPIF): I2C slave received data stop interrupt flag.

Bit 2: not used bit, fixed to "0" all the time.

Bit 1(I2CRIF): I2C receive interrupt flag. Set when I2C receiving 1byte data and responds ACK signal. Reset by firmware or I2C disable.

Bit 0(I2CTIF): I2C transmit interrupt flag. Set when I2C transmits 1 byte data and receive handshake signal (ACK or NACK). Reset by firmware or I2C disable.

6.1.12 Bank0 RF(Unused)

6.1.13 Bank0 R10:EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	EIES

Bits 7~1: unused bit, set to 0 all the time

Bit 0(EIES) : external interrupt edge select bit

0: falling edge interrupt

1: rising edge interrupt

6.1.14 Bank0 R11: WDTCR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0

Bit 7(WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6(EIS): P60/ /INT switch control bit

0: P60

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 must be set to "1". When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6).

EIS is both readable and writable.

Bits 5(INT): interrupt enable flag.

0: interrupt masked by DISI or hardware interrupt

1: interrupt enabled by ENI/DISI instructions

Bits 4: no used bit, fixed to “0” all the time.

Bit 3(PSWE): Prescaler Enable Bit for WDT

0: Prescaler disable, WDT rate is 1:1

1: Prescaler enable, WDT rate is set from bits 2~0

Bits 2~0(PSW2~PSW0): WDT Prescale Bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.15 Bank0 R12: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bits 7~4: no used bits, fixed 0 all the time.

Bit 3(LVDEN): Low voltage detector enable bit

0: LVD disable

1: LVD enable

Bit 2(/LVD): Low voltage detector. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level which set by LVD1 and LVD0, this bit will be cleared.

0: the low voltage is detected

1: the low voltage is not detected or LVD function is disabled

Bits1~0(LVD1~LVD0): Low voltage detector level select bits

LVD1	LVD0	LVD voltage interrupt level
0	0	2.3
0	1	3.3
1	0	4.0
1	1	4.5

6.1.16 Bank0 R13: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TCCS	TS	TE	PSTE	PST2	PST1	PST0

Bit 7: unused bit, set to 0 all the time.

Bit 6(TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC Signal Source

0: Internal oscillator cycle clock. If P77 is used as I/O pin, TS must be 0.

1: Transition on the TCC pin

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin;

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler Enable Bit for TCC

0: prescaler disable, TCC rate is 1:1

1: prescaler enable, TCC rate is set as Bits 2~0.

Bits 2~0 (PST2~PST0): TCC Prescaler Bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.17 Bank0 R14: TCCDATA (TCC Data Register)

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. Writable and readable as any other registers.

6.1.18 Bank0 R15~R19 (IOCR5~IOCR9)

These registers are used to control I/O port direction. They are both readable and writable.

0: put the relative I/O pin as output

1: put the relative I/O pin into high impedance

6.1.19 Bank0 R1A~R1B (Unused)

6.1.20 Bank0 R1C: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bits 7(LVDIE): LVDIF interrupt enable bit.

0: Disable LVDIF interrupt

1: Enable LVDIF interrupt

Bit 6 (ADIE): ADIF interrupt enable bit.

0: Disable ADIF interrupt

1: Enable ADIF interrupt.

When the ADC Complete is used to enter interrupt vector or enter next instruction, the ADIE bit must be set to “Enable“.

Bit 5 (SPIE): Interrupt enable bit.

0: disable SPIF interrupt

1: enable SPIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit.

0: Disable PWMB interrupt

1: Enable PWMB interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit.

0: Disable PWMA interrupt

1: Enable PWMA interrupt

Bit 2 (EXIE): EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

6.1.21 Bank0 R1D: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0 : Disable CMP2IF interrupt

1 : Enable CMP2IF interrupt

When the Comparator output status changed is used to enter interrupt vector or enter next instruction, the CMP2IE bit must be set to “Enable“.

Bit 6 (CMP2IE): CMP1IF interrupt enable bit.

0 : Disable CMP1IF interrupt

1 : Enable CMP1IFinterrupt

When the Comparator output status changed is used to enter interrupt vector or enter next instruction, the CMP1IE bit must be set to “Enable“.

Bit 5 (TC3IE): Interrupt enable bit.

0: disable TC3IF interrupt

1: enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit.

0: disable TC2IF interrupt

1: enable TC2IF interrupt

Bit 3 (TC1IE): Interrupt enable bit.

0: disable TC1IF interrupt

1: enable TC1IF interrupt

Bit 2 (UERRIE): UART receive error interrupt enable bit.

0: disable UERRIF interrupt

1: enable UERRIF interrupt

Bit 1 (URIE): UART receive mode Interrupt enable bit.

0: disable RBFF interrupt

1: enable RBFF interrupt

Bit 0 (UTIE): UART transmit mode interrupt enable bit.

0: disable TBEF interrupt

1: enable TBEF interrupt

6.1.22 Bank0 R1E: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE

Bits 7~3: unused bits, set to 0 all the time.

Bit 3 (I2CSTPIE): I2CSTPIF interrupt enable bit.

0: Disable I2CSTP interrupt

1: Enable I2CSTP interrupt

Bit 2 : unused bit, set to 0 all the time

Bit 1 (I2CRIE): I2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 2 (I2CTIE): I2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

6.1.23 Bank0 R1F(Unused)

6.1.24 Bank0 R20: P5WUCR (Port 5 Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50

Bits 7~0(WU_P57~WU_P50): wake up function control for Port 5.

0: disable wake up function

1: enable wake up function

6.1.25 Bank0 R21: P5WUECR (Port 5 Wake Up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50

Bits 7~0(WUE_P57~WUE_P50): wake up signal edge selection for Port 5.

0: falling edge trigger

1: rising edge trigger

6.1.26 Bank0 R22: P7WUCR (Port 7 Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70

Bits 7~0(WU_P77~WU_P70): wake up function control for Port 7.

0: disable wake up function

1: enable wake up function

6.1.27 Bank0 R23: P7WUECR (Port 7 Wake Up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70

Bits 7~0(WUE_P77~WUE_P70): wake up signal edge selection for Port 7.

0: falling edge trigger

1: rising edge trigger

6.1.28 Bank0 R24: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0

Bit 7(VREFS): The input source of the VREF of the ADC.

0: The Vref of the ADC is connected to Vdd (default value), and the **P50/VREF pin carries out the function of P50**

1: The Vref of the ADC is connected to P50/VREF.

Note: the priority of P50/VREF PIN

P50/VREF PIN PRIORITY	
High	Low
VREF	P50

Bit 6(ADRUN): ADC starts to run

1: an A/D conversion starts. This bit can be set by software

0: reset on completion of the conversion. This bit can not be reset though software

Bit 5(ADPD): ADC Power-down mode.

1: ADC is operating

0: switch off the resistor reference to save power even while the CPU is operating.

Bits 4~3: unused bits, set to 0 all the time

Bit 2~0(ADIS2~ADIS0): Analog Input Selection

ADIS2	ADIS1	ADIS0	Analog Input Pin
0	0	0	AD0/P60
0	0	1	AD1/P61
0	1	0	AD2/P62
0	1	1	AD3/P63
1	0	0	AD4/P64
1	0	1	AD5/P65
1	1	0	AD6/P66
1	1	1	AD7/P67

Note: AD channel can only be changed when the ADIF bit and the ADRUN bit are both LOW.

6.1.29 Bank0 R25: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF2	VOF1	VOF0	**CKR2**	**CKR1**	**CKR0**

Bit 7(CALI): Calibration enable bit for A/D offset

0: Calibration disable;

1: Calibration enable.

Bit 6(SIGN): Polarity bit of offset voltage

0: Negative voltage;

1: Positive voltage.

Bits 5~3(VOF2~VOF0): Offset voltage bits

VOF2	VOF1	VOF0	OFFSET
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit 2~0(CKR2~CKR0): The prescaler of oscillator clock rate of ADC

CKR2 CKR1 CKR0	Operation Mode	Max. system operation frequency
000(default)	Fsco/4	4 MHz
001	Fsco/1	1 MHz
010	Fsco/2	2MHz
011	Fsco/8	8 MHz
100	Fsco/16	16 MHz
101	Fsco/32	32 MHz
110	Fsco/64	64 MHz
111	Internal RC	

6.1.30 Bank0 R26: ADICL (ADC Input Select Low Byte Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin.

0: Disable ADC7, P67 act as I/O pin.

1: Enable ADC7 act as analog input pin.

Bit 6 (ADE6): AD converter enable bit of P66 pin.

0: Disable ADC6, P66 act as I/O pin

1: Enable ADC6 act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin.

0: Disable ADC5, P65 act as I/O pin

1: Enable ADC5 act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin.

0: Disable ADC4, P64 act as I/O pin

1: Enable ADC4 act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0: Disable ADC3, P63 act as I/O pin

1: Enable ADC3 act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0: Disable ADC2, P62 act as I/O pin

1: Enable ADC2 act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin.

0: Disable ADC1, P61 act as I/O pin

1: Enable ADC1 act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0: Disable ADC0, P60 act as I/O pin

1: Enable ADC0 act as analog input pin

Note: the priority of P60/ADC0//INT PIN

P60/ADC1//INT PIN PRIORITY		
High	Medium	Low
/INT	ADC0	P60

6.1.31 Bank0 R27~R28(Unused)

6.1.32 Bank0 R29: ADDH (AD Data High Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Bits 7~0(AD11~AD4): AD high 8-bits data buffer. When A/D conversion is complete, the result of high 8 bits is stored into ADDH; the low 4 bits is stored into ADDL. Then the ADRUN bit is cleared and the ADIF is set.

6.1.33 Bank0 R2A: ADDL (AD Data Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD3	AD2	AD1	AD0

Bits 7~4: unused bits, set to 0 all the time.

Bits 3~0(AD3~AD0): AD low 4-bits data buffer.

6.1.34 Bank0 R2B: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select Bit

0: Data shift out on rising edge, and shifts in on falling edge. Data is on hold during low-level.

1: Data shift out falling edge, and shift in on rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable Bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, user is required to read the SPIR register although only the transmission is implemented. This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

0: Reset as soon as the shift is complete, and the next byte is read to shift.

1: Start to shift, and remain on "1" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

0: After the serial data output, the SDO remain high.

1: After the serial data output, the SDO remain low.

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select Bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.35 Bank0 R2C: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF

Bit 7 (DORD): Data Shift of Type Control Bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO Status Output Delay Times Options. When CPU oscillator source using Fs, it just delays 1 CLK time.

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: No used bit, set to 0 all the time.

Bit 3(OD3): Open drain control bit

0: Open drain disable for SDO

1: Open drain enable for SDO

Bit 2(OD4): Open drain control bit

0: Open drain disable for SCK

1: Open drain enable for SCK

Bit 1: unused bit, set to 0 all the time.

Bit 0 (RBF): Read Buffer Full Flag

0: Receiving not completed, and SPIR has not fully exchanged.

1: Receiving completed, and SPIR is fully exchanged.

6.1.36 Bank0 R2D: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bits 7~0(SRB7~SRB0): SPI Read Data Buffer

6.1.37 Bank0 R2E: SPIR (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bits 7~0(SWB7~SWB0): SPI Write Data Buffer

6.1.38 Bank0 R2F: WUCR1 (Wake Up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SPIWE	LVDWE	ICWE	ADWE	CMP2WE	CMP1WE	EXWE

Bits 7: unused bit, set to 0 all the time.

Bit 6 (SPIWE): SPI wake up enable bit. Acts when SPI works as slave mode.

0: Disable SPI wake up.

1: Enable SPI wake up.

Bit 5 (LVDWE): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

When the Low Voltage Detect is used to enter interrupt vector or to wake-up IC from sleep/idle with Low Voltage Detect running, the LVDWE bit must be set to "Enable".

Bit 4 (ICWE): Port 6 Input Status Change Wake-up enable bit.

0: Disable port 6 input status change wake-up

1: Enable port 6 input status change wake-up

When the Port 6 input status changed is used to enter interrupt vector or to wake-up IC from sleep/idle, the ICWE bit must be set to "Enable".

Bit 3 (ADWE): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter interrupt vector or to wake-up IC from sleep/idle with AD conversion running, the ADWE bit must be set to "Enable".

Bits 2~1 (CMP2WE~CMP1WE): Comparator 2~1 wake-up enable bits

0: Disable Comparator wake up

1: Enable Comparator wake up

When the Comparators 2~1 output status change is used to enter an interrupt vector or to wake up the IC from sleep, the CMPWE bit must be set to "Enable".

Bit 0 (EXWE): External Interrupts Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter an interrupt vector or to wake up the IC from sleep, the EXWE bits must be set to "Enable".

6.1.39 Bank0 R30~R31(Unused)

6.1.40 Bank0 R32: URCR1 (UART Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7(URTD8): Transmission data bit 8

Bits 6~5(UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART mode
0	0	Mode1: 7-bit
0	1	Mode1: 8-bit
1	0	Mode1: 9-bit
1	1	Reserved

Bits 4~2(BRAT2~BRAT0): transmit Baud rate selection

BRATE2	BRATE1	BRATE0	Baud rate	8MHz
0	0	0	Fc/13	38400
0	0	1	Fc/26	19200
0	1	0	Fc/52	9600
0	1	1	Fc/104	4800
1	0	0	Fc/208	2400
1	0	1	Fc/416	1200
1	1	0	TC3	
1	1	1	Reserved	

Bit 1(UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when write into URTD register. UTBE bit will be clear by hardware when enabling transmission. And UTBE bit is read-only . Therefore, write URTD register is necessary when want to start transmitting shifting.

Bit 0(TXE): Enable transmission

0: Disable

1: Enable

6.1.41 Bank0 R33: URCR2 (UART Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SBIM1	SBIM0	UINVEN	0	0	0

Bits 7~6: unused bits, set to 0 all the time.

Bits 5~4(SBIM1~SBIM0): Serial bus interface operating mode select

SBIM1	SBIM0	Operation mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	I2C mode

Bit 3(UINVEN): Enable UART TX and RX port inverse output.

0: Disable **TX** and **RX** port inverse output.

1: Enable **TX** and **RX** port inverse output.

Bits 2~0: unused bits, set to 0 all the time.

6.1.42 Bank0 R34: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7(URRD8): receiving data bit 8

Bit 6(EVEN): select parity check

0: Odd parity

1: Even parity

Bit 5(PRE): enable parity addition

0: Disable

1: Enable

Bit 4(PRERR): Parity error flag. Set to 1 when parity error happened, and clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error happened, and clear to 0 by software.

Bit 2(FMERR): Framing error flag. Set to 1 when framing error happen, and clear to 0 by software.

Bit 1(URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URS register. URBF will be clear by hardware when enabling receiving. And URBF bit is read-only. Therefore, read URS register is necessary to avoid overrun error.

Bit 0(RXE): Enable receiving

`0: Disable

1: Enable

6.1.43 Bank0 R35: URRD (UART Receive Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7~0(URRD7~URRD0): UART receive data buffer. Read only.

6.1.44 Bank0 R36: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7~0(URTD7~URTD0): UART transmit data buffer. Write only.

6.1.45 Bank0 R37: TBPTL (Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bits 7~0(TB7~TB0): table point address bits 7~0.

6.1.46 Bank0 R38: TBPTH (Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8

Bit 7(HLB): take MLB or LSB at machine code.

Bits 6~5(GP1~GP0): general purpose read/write bits

Bits 4~0: table point address bits 12~8.

6.1.47 Bank0 R39: CMP1CR (Comparator 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT

Bit 7 (C1RS): Comparator input reference source select bit

0: Cin1+ source external

1: Cin1+ source internal

Bit 6 (CP1OUT): the result of comparator output

Bits 5~4(CMP1COS1~CMP1COS0): Comparator 1/OP1 select bits

CMP1COS1	CMP1COS0	Function Description
0	0	Comparator 1 not used. P70, P71, P72 act as normal I/O pin
0	1	P71, P72, act as an Comparator 1 input pin and P70 acts as normal I/O pin
1	0	P71, P72 act as an Comparator1 input pin and P70 acts as Comparator1 output pin (CO1).
1	1	reserved

Bit 3 (CP1NS): negative end of Comparator 1 is connected to ground.

0: disable, P72/CIN1- as CIN1-.

1: enable, P72/CIN1- as P72

Bit 2 (CP1PS): positive end of Comparator 1 is connected to ground.

0: disable, P71/CIN1+ as CIN1+.

1: enable, P71/CIN1+ as P71

Bit 1 (CP1NRE): Noise Rejection Enable Bit for Comparator 1

0: Disable noise rejection

1:Enable noise rejection (default). **But in Low Crystal 2 Oscillator (LXT2) mode, Green mode and Idle mode, the noise rejection circuits are always disabled.**

Bit 0 (CP1NRDT): Comparator 1 Noise Rejection Delay Time. In Low XTAL1 oscillator (LXT1) mode the noise rejection high/low pulses always 4/Fm.

0:Comparator1 output H/L pulses equal to 4/Fm (0.5us at 8MHz) is regarded as signal.

1:Comparator1 output H/L pulses equal to 8/Fm (1us at 8MHz) is regarded as signal.

6.1.48 Bank0 R3A~R3B: unused

6.1.49 Bank0 R3C: CMP2CR (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT

Bit 7 (C2RS): Comparator 2 input reference source select bit

0: Cin2+ source external

1: Cin2+ source internal

Bit 6 (CP2OUT): the result of comparator 2 output

Bits 5~4(CMP1COS1~CMP1COS0): Comparator 2/OP2 select bits

CMP2COS1	CMP2COS0	Function Description
0	0	Comparator2 not used. P80, P81, P82 act as normal I/O pin
0	1	P81, P82, act as an Comparator2 input pin and P80 acts as normal I/O pin
1	0	P81, P82 act as an Comparator2 input pin and P80 acts as Comparator2 output pin (CO2).
1	1	reserved

Bit 3 (CP2NS): negative end of Comparator 2 is connected to ground.

0: disable, P82/CIN2- as CIN2-.

1: enable, P82/CIN2- as P82

Bit 2 (CP2PS): positive end of Comparator 2 is connected to ground.

0: disable, P81/CIN2+ as CIN2+.

1: enable, P81/CIN2+ as P81

Bit 1 (CP2NRE): Noise Rejection Enable Bit for Comparator 2

0: Disable noise rejection

1: Enable noise rejection (default). But in Low Crystal 2 Oscillator (LXT2) mode, Green mode and Idle mode, the noise rejection circuits are always disabled.

Bit 0 (CP2NRDT): Comparator 2 Noise Rejection Delay Time. In Low XTAL1 oscillator (LXT1) mode the noise rejection high/low pulses always 4/Fm.

0: Comparator1 output H/L pulses equal to 4/Fm (0.5us at 8MHz) is regarded as signal.

1: Comparator1 output H/L pulses equal to 8/Fm (1us at 8MHz) is regarded as signal.

6.1.50 Bank0 R3D~R42: unused

6.1.51 Bank0 R43: CPIRLCON (Comparator Internal Reference level Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0

Bit 7(BG2OUT): when this bit set to 1, P83 pin will output bandgap reference voltage

Bits 6~4(C2IRL2~C2IRL0) : Comparator 2 internal reference level

Bit 3(BG1OUT): when this bit set to 1, P73 pin will output bandgap reference voltage

Bits 2~0(C1IRL2~C1IRL0) : Comparator 1 internal reference level

CxIRL2	CxIRL1	CxIRL0	voltage Level(V)
0	0	0	0.5
0	0	1	0.8
0	1	0	1.0
0	1	1	1.5
1	0	0	2.0
1	0	1	2.2
1	1	0	2.5
1	1	1	3.0

6.1.52 Bank0 R44~R47: unused

6.1.53 Bank0 R48: TC1CR(Timer 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0

Bit 7(TC1CAP): software capture control

0: software capture control disable

1: software capture control enable

Bit 6(TC1S): Timer/Counter 1 start control

0: stop and counter clear

1: start

Bits 5~4(TC1CK1~TC1CK0): Timer/Counter 1 clock source select bits

TC1CK1	TC1CK0	CLOCK SOURCE	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
		Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	$F_C/2^{12}$	512μS	131072μS	256ms	65536ms
0	1	$F_C/2^{10}$	128μS	32768μS	64ms	16384ms
1	0	$F_C/2^7$	16μS	4096μS	8ms	2048ms
1	1	External clock (TC1 pin)	-	-	-	-

Bit 3(TC1M): Timer/Counter 1 mode select

0: Timer/Counter 1 mode

1: Capture mode

Bit 2(TC1ES): Timer/Counter 1 signal edge

0: increment if the transition from low to high (rising edge) take place on TC1 pin.

1: increment if the transition from high to low (falling edge) take place on TC1 pin.

Bits 1~0: no used, set to 0 all the time.

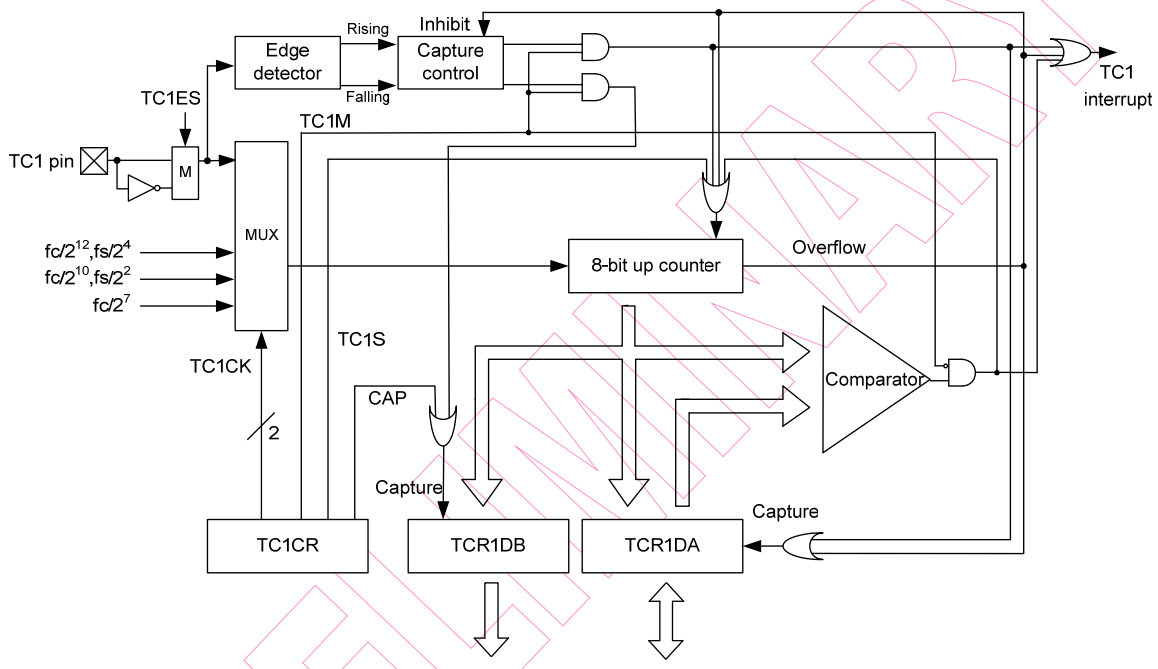


Fig.6 Configuration of Timer/Counter1

In Timer mode, counting up is performed using internal clock. When the contents of up-counter are matched the TCR1DA, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TCR1DB by setting TC1CAP to “1” and the TC1CAP is cleared to “0” after capture automatically.

In Counter mode, counting up is performed using external clock input pin (TC1 pin) and either rising or falling edge can be select by TC1ES but **both edges can not be used**. When the contents of up-counter are matched the TCR1DA, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared. The current contents of up-counter are loaded into TCR1DB by setting TC1CAP to “1” and the TC1CAP is cleared to “0” after capture automatically.

In Capture mode, the pulse width, period and duty of the TC1 input pin are measured in this mode, which can be used to decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TC1 pin input, the contents of counter is loaded into TCR1DA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TC1 pin input, the contents of counter are loaded into TCR1DB. The counter is still countering, on the next rising edge of TC1 pin input, the contents of counter are loaded into TCR1DA, counter is cleared and interrupt is generated again. If the overflows before the edge is detected, the FFH is loaded into TCR1DA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detection) is generated, capture and overflow detection are halted until TCR1DA is read out.

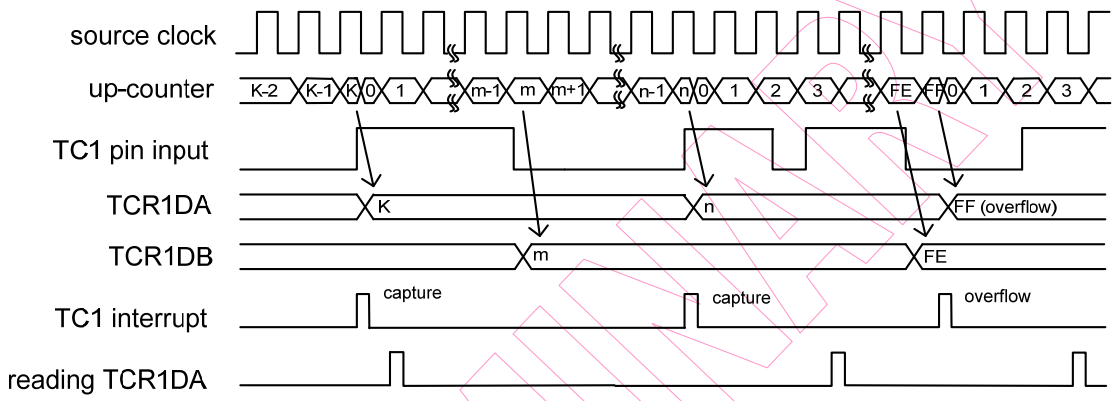


Fig. 7 Timing chart of capture mode

6.1.54 Bank0 R49: TCR1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0

Bits 7~0(TCR1DA7~TCR1DA0): Data buffer of 8 bit timer/counter 1

6.1.55 Bank0 R4A: TCR1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0

Bits 7~0(TCR1DB7~TCR1DB0): Data buffer of 8 bit timer/counter 1

6.1.56 Bank0 R4B: TC2CR (Timer 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7~6: unused bits, set to 0 all the time

Bit 5 (TC2ES): TC2 signal edge

0: increment if the transition from low to high (rising edge) takes place on TC2 pin

1: increment if the transition from high to low (falling edge) takes place on TC2 pin

Bit 4 (TC2M): Timer/Counter2 mode select.

0: Timer/Counter 2 mode

1: Window mode

Bit 3(TC2S): Timer/Counter2 start control

0: Stop and counter clear

1: start

Bits 2~0(TC2CK2~TC2CK0): Timer/Counter 2 clock source select.

TC2CK2	TC2CK1	TC1CK0	CLOCK SOURCE	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{23}$	1.05s	19.1hr	145hr	9544hr
0	0	1	$F_C/2^{13}$	1.024ms	67.11s	512ms	33554.432s
0	1	0	$F_C/2^8$	32μs	2.097s	16ms	1048.576s
0	1	1	$F_C/2^3$	1μs	65.536ms	0.5ms	32768ms
1	0	0	F_C	125ns	8.192ms	0.0625ms	4096ms
1	0	1	-	-	-	-	-
1	1	0	-	-	-	-	-
1	1	1	External clock (TC2 pin)	-	-	-	-

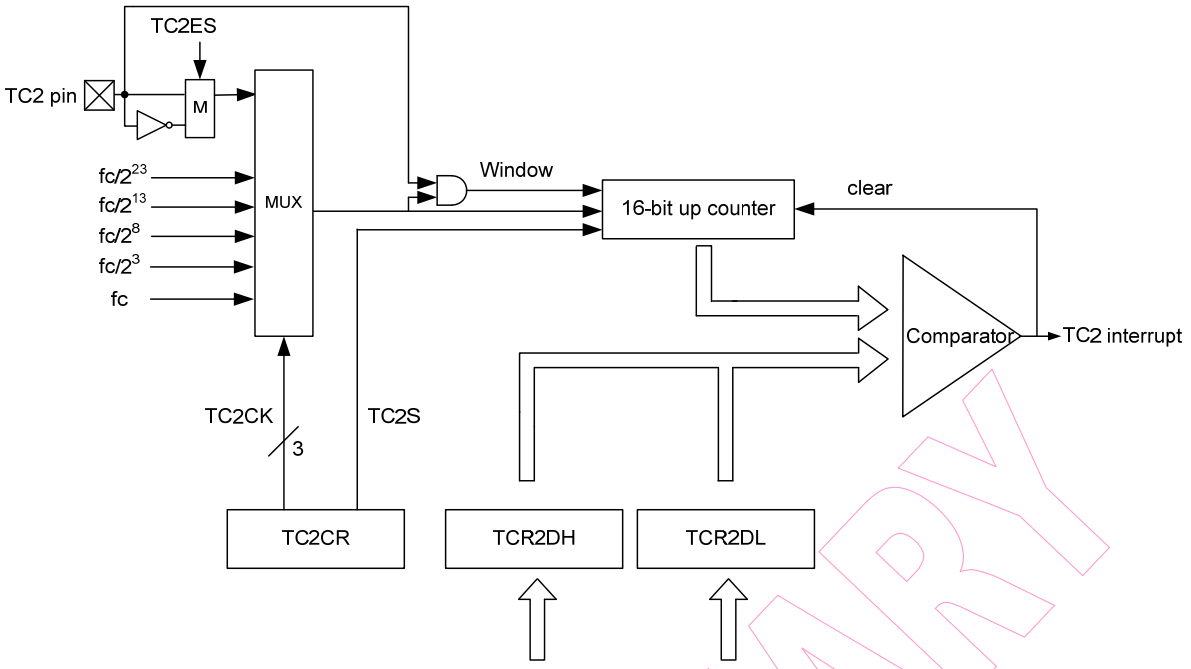


Fig. 8 Configuration of Timer/Counter2

In Timer mode, counting up is performed using internal clock. When the contents of up-counter are matched the TCR2 (TCR2H+TCR2L), then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

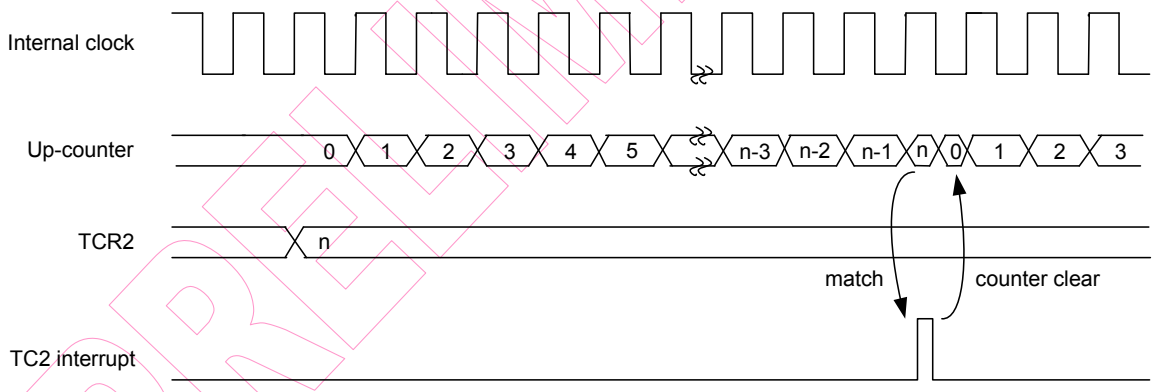


Fig. 9 Timer mode timing chart

In Counter mode, counting up is performed using external clock input pin (TC2 pin) and either rising or falling can be select by setting TC2ES . When the contents of up-counter are matched the TCR2 (TCR2H+TCR2L), then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

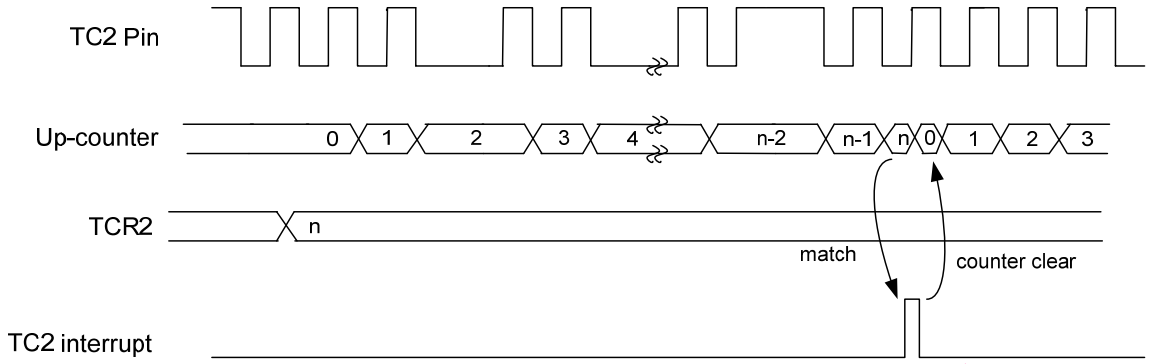


Fig. 10 Counter mode timing chart (INT2ES = 1)

In Window mode, countering up is performed on rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of up-counter are matched the TCR2 (TCR2H+TCR2L), then interrupt is generated and counter is cleared. **The frequency (window pulse) must be slower than the selected internal clock.**

Writing to the TCR2L, the comparison is inhibited until TCR2H is written.

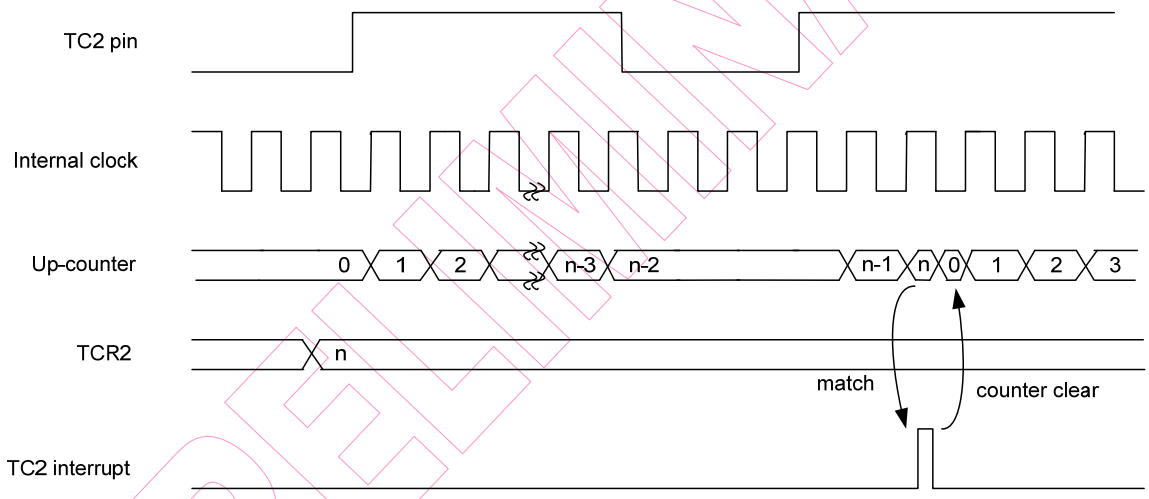


Fig. 11 Window mode timing chart

6.1.57 Bank0 R4C: TCR2DH (Timer 2 High Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8

Bits 7~0(TCR2D15~ TCR2D8): High byte data buffer of 16-bit timer/couter2

6.1.58 Bank0 R4D: TCR2DL (Timer 2 Low Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0

Bits 7~0(TCR2D7~ TCR2D0): Low byte data buffer of 16-bit timer/couter2

6.1.59 Bank0 R4E: TC3CR (Timer 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7~6(TC3FF1~TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5(TC3S): Timer/Counter 3 start control

0: Stop and clear counter

1: start

Bits 4~2(TC3CK2~TC3CK0): Timer/Counter 3 clock source select.

TC3CK2	TC3CK1	TC3CK0	CLOCK SOURCE	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{11}$	256μs	65536μs	128ms	32768ms
0	0	1	$F_C/2^7$	16μs	4096μs	8ms	2048ms
0	1	0	$F_C/2^5$	4μs	1024μs	2ms	512ms
0	1	1	$F_C/2^3$	1μs	256μs	500μs	128ms
1	0	0	$F_C/2^2$	500ns	128μs	250μs	64ms
1	0	1	$F_C/2$	250ns	64μs	125μs	32ms
1	1	0	F_C	125ns	32μs	62.5μs	16ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1~0(TC3M1~TC3M0): Timer/Counter 3 operation mode select.

TC3M1	TC3M0	Operating mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

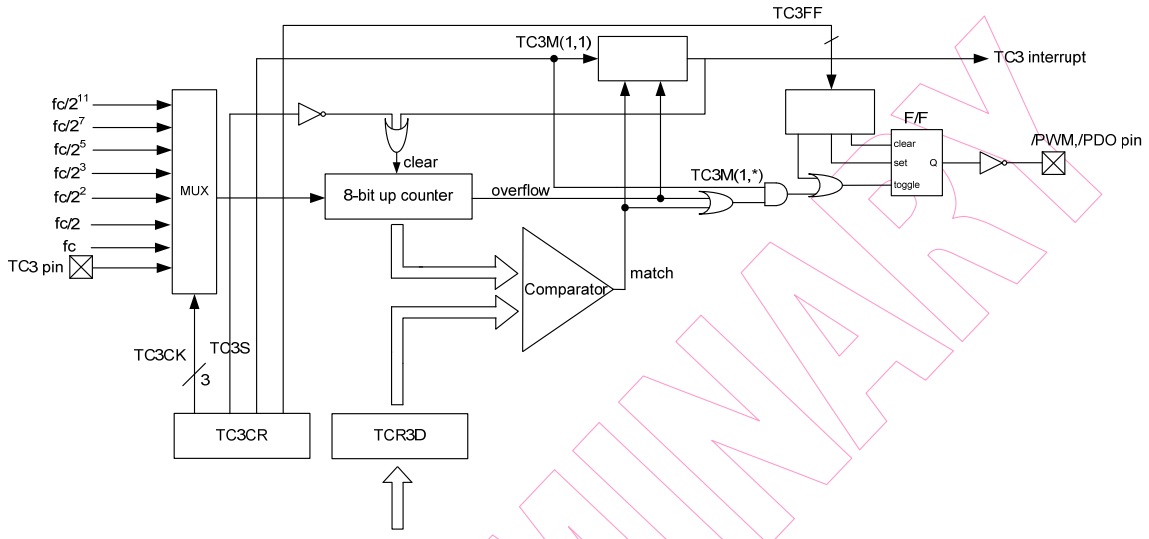


Fig. 12 Timer/Counter3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of up-counter are matched the TCR3D, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using external clock input pin (TC3 pin). When the contents of up-counter are matched the TCR3D, then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using internal clock. The contents of TCR3D are compared with the contents of up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time the /PDO output is toggled.

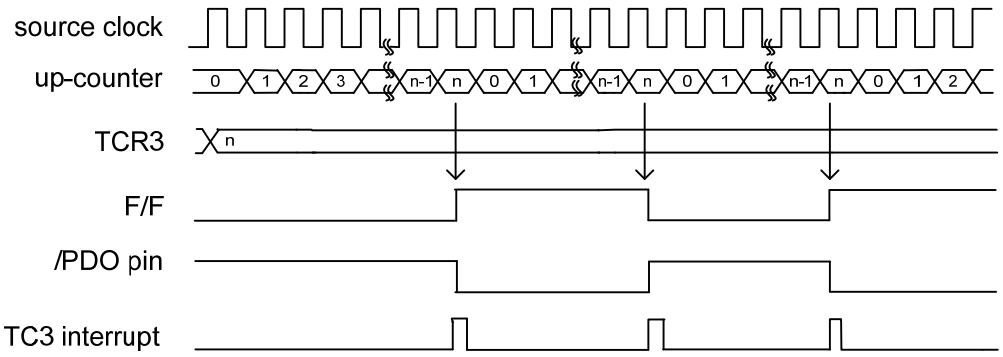


Fig. 13 Timing chart for PDO mode

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of up-counter. The F/F is toggled when match is found. The counter is still countering, the F/F is toggled again when counter is overflow, then the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time the overflow occurs. **TCR3 is configured a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the first time, TRC3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

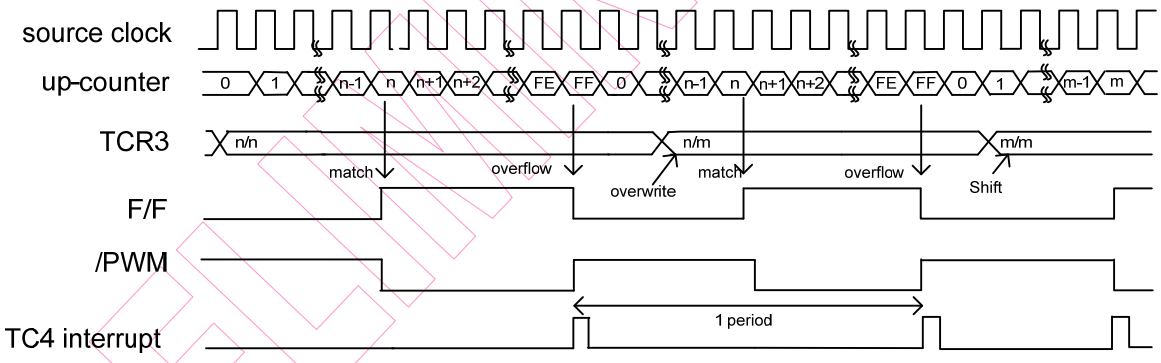


Fig. 14 Timing chart for PWM mode

6.1.60 Bank0 R4F: TCR3D (Timer 3 Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0

Bits 7~0(TCR3DB7~TCR13DB0): Data buffer of 8 bit timer/counter 3

6.1.61 Bank1 R5: P5PHCR (Port 5 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

Bit 7(/PH57): control bit used to enable the pull high of P57 pin

0: enable internal pull-high

1: disable internal pull-high

Bit 6(/PH56): control bit used to enable the pull high of P56 pin

Bit 5(/PH55): control bit used to enable the pull high of P55 pin

Bit 4(/PH54): control bit used to enable the pull high of P54 pin

Bit 3(/PH53): control bit used to enable the pull high of P53 pin

Bit 2(/PH52): control bit used to enable the pull high of P52 pin

Bit 1(/PH51): control bit used to enable the pull high of P51 pin

Bit 0(/PH50): control bit used to enable the pull high of P50 pin

6.1.62 Bank1 R6: P6PHCR (Port 6 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7(/PH67): control bit used to enable the pull high of P67 pin

Bit 6(/PH66): control bit used to enable the pull high of P66 pin

Bit 5(/PH65): control bit used to enable the pull high of P65 pin

Bit 4(/PH64): control bit used to enable the pull high of P64 pin

Bit 3(/PH63): control bit used to enable the pull high of P63 pin

Bit 2(/PH62): control bit used to enable the pull high of P62 pin

Bit 1(/PH61): control bit used to enable the pull high of P61 pin

Bit 0(/PH60): control bit used to enable the pull high of P60 pin

6.1.63 Bank1 R7: P7PHCR (Port 7 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70

Bit 7(/PH77): control bit used to enable the pull high of P77 pin

Bit 6(/PH76): control bit used to enable the pull high of P76 pin

Bit 5(/PH75): control bit used to enable the pull high of P75 pin

Bit 4(/PH74): control bit used to enable the pull high of P74 pin

Bit 3(/PH73): control bit used to enable the pull high of P73 pin

Bit 2(/PH72): control bit used to enable the pull high of P72 pin

Bit 1(/PH71): control bit used to enable the pull high of P71 pin

Bit 0(/PH70): control bit used to enable the pull high of P70 pin

6.1.64 Bank1 R8: P8PHCR (Port 8 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80

Bit 7(/PH87): control bit used to enable the pull high of P87 pin

Bit 6(/PH86): control bit used to enable the pull high of P86 pin

Bit 5(/PH85): control bit used to enable the pull high of P85 pin

Bit 4(/PH84): control bit used to enable the pull high of P84 pin

Bit 3(/PH83): control bit used to enable the pull high of P83 pin

Bit 2(/PH82): control bit used to enable the pull high of P82 pin

Bit 1(/PH81): control bit used to enable the pull high of P81 pin

Bit 0(/PH80): control bit used to enable the pull high of P80 pin

6.1.65 Bank1 R9: P9PHCR (Port 9 Pull High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90

Bit 7(/PH97): control bit used to enable the pull high of P97 pin

Bit 6(/PH96): control bit used to enable the pull high of P96 pin

Bit 5(/PH95): control bit used to enable the pull high of P95 pin

Bit 4(/PH94): control bit used to enable the pull high of P94 pin

Bit 3(/PH93): control bit used to enable the pull high of P93 pin

Bit 2(/PH92): control bit used to enable the pull high of P92 pin

Bit 1(/PH91): control bit used to enable the pull high of P91 pin

Bit 0(/PH90): control bit used to enable the pull high of P90 pin

6.1.66 Bank1 RA (Unused)

6.1.67 Bank1 RB: P5PLCR (Port 5 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50

Bit 7(/PL57): control bit used to enable the pull low of P57 pin

0: enable internal pull-low

1: disable internal pull-low

Bit 6(/PL56): control bit used to enable the pull low of P56 pin

Bit 5(/PL55): control bit used to enable the pull low of P55 pin

Bit 4(/PL54): control bit used to enable the pull low of P54 pin

Bit 3(/PL53): control bit used to enable the pull low of P53 pin

Bit 2(/PL52): control bit used to enable the pull low of P52 pin

Bit 1(/PL51): control bit used to enable the pull low of P51 pin

Bit 0(/PL50): control bit used to enable the pull low of P50 pin

6.1.68 Bank1 RC: P6PLCR (Port 6 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60

Bit 7(/PL67): control bit used to enable the pull low of P67 pin

Bit 6(/PL66): control bit used to enable the pull low of P66 pin

Bit 5(/PL65): control bit used to enable the pull low of P65 pin

Bit 4(/PL64): control bit used to enable the pull low of P64 pin

Bit 3(/PL63): control bit used to enable the pull low of P63 pin

Bit 2(/PL62): control bit used to enable the pull low of P62 pin

Bit 1(/PL61): control bit used to enable the pull low of P61 pin

Bit 0(/PL60): control bit used to enable the pull low of P60 pin

6.1.69 Bank1 RD: P7PLCR (Port 7 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70

Bit 7(/PL77): control bit used to enable the pull low of P77 pin

Bit 6(/PL76): control bit used to enable the pull low of P76 pin

Bit 5(/PL75): control bit used to enable the pull low of P75 pin

Bit 4(/PL74): control bit used to enable the pull low of P74 pin

Bit 3(/PL73): control bit used to enable the pull low of P73 pin

Bit 2(/PL72): control bit used to enable the pull low of P72 pin

Bit 1(/PL71): control bit used to enable the pull low of P71 pin

Bit 0(/PL70): control bit used to enable the pull low of P70 pin

6.1.70 Bank1 RE: P8PLCR (Port 8 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80

Bit 7(/PL87): control bit used to enable the pull low of P87 pin

Bit 6(/PL86): control bit used to enable the pull low of P86 pin

Bit 5(/PL85): control bit used to enable the pull low of P85 pin

Bit 4(/PL84): control bit used to enable the pull low of P84 pin

Bit 3(/PL83): control bit used to enable the pull low of P83 pin

Bit 2(/PL82): control bit used to enable the pull low of P82 pin

Bit 1(/PL81): control bit used to enable the pull low of P81 pin

Bit 0(/PL80): control bit used to enable the pull low of P80 pin

6.1.71 Bank1 RF: P9PLCR (Port 9 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90

Bit 7(/PL97): control bit used to enable the pull low of P97 pin

Bit 6(/PL96): control bit used to enable the pull low of P96 pin

Bit 5(/PL95): control bit used to enable the pull low of P95 pin

Bit 4(/PL94): control bit used to enable the pull low of P94 pin

Bit 3(/PL93): control bit used to enable the pull low of P93 pin

Bit 2(/PL92): control bit used to enable the pull low of P92 pin

Bit 1(/PL91): control bit used to enable the pull low of P91 pin

Bit 0(/PL90): control bit used to enable the pull low of P90 pin

6.1.72 Bank1 R10 (Unused)

6.1.73 Bank1 R11: P5HD/SCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50

Bits 7~0(H57~H50): P57~P50 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.74 Bank1 R12: P6HD/SCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60

Bits 7~0(H67~H60): P67~P60 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.75 Bank1 R13: P7HD/SCR (Port 7 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70

Bits 7~0(H77~H70): P77~P70 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.76 Bank1 R14: P8HD/SCR (Port 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80

Bits 7~0(H87~H80): P87~P80 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.77 Bank1 R15: P9HD/SCR (Port 9 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90

Bits 7~0(H97~H90): P97~P90 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.78 Bank1 R16 (Unused)

6.1.79 Bank1 R17: P5ODCR (Port 5 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50

Bits 7~0(OD57~OD50): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.80 Bank1 R18: P6ODCR (Port 6 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bits 7~0(OD67~OD60): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.81 Bank1 R19: P7ODCR (Port 7 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70

Bits 7~0(OD77~OD70): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.82 Bank1 R1A: P8ODCR (Port 8 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80

Bits 7~0(OD87~OD80): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.83 Bank1 R1B: P9ODCR (Port 9 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90

Bits 7~0(OD97~OD90): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.84 Bank1 R1C (Unused)

6.1.85 Bank1 R1D: IRCS (IRC Frequency Selection Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RCM1	RCM0	0	0	0	0

Bits 7~6: unused bits, set to 0 all the time.

Bits 5~4 (RCM1 ~ RCM0): IRC Mode Frequency Selection Bits

RCM 1	RCM 0	Frequency(MHz)
0	0	4
0	1	16
1	0	8
1	1	455kHz

WORD1 COBS0=0 :

The R1D<5,4> of the initialized values will keep same the WORD1<6,5>.

The R1D<5,4> can't change.

WORD1 COBS0=1 :

The R1D<5,4> of the initialized values will keep same the WORD1<6,5>.

The R1D<5,4> can change, When user want to work on other IRC frequency.

ex. 4M -> 16M

Bits 3~0: unused bits, set to 0 all the time.

6.1.86 Bank1 R1E~R22 (Unused)

6.1.87 Bank1 R23: I2CCR1 (I2C Status and Control Register1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY

Bit 7(Strobe/Pend): In master mode, it is used as strobe signal to control I2C circuit to send SCL clock. Reset automatically after receiving or transmitting handshake signal (ACK or NACK). In slave mode, it is used as pending signal, user should clear it after fill data into Tx buffer or get data from Rx buffer to inform slave I2C circuit to release SCL signal.

Bit 6(IMS): I2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I2C Fast/Standard mode select bit. (If Fm is 4MHz and I2CTS1~0<0,0>)

0: Standard mode (100K bit/s)

1: Fast mode (400K bit/s)

Bit 4(SOTP): In Master mode, if STOP=1 and R/nW=1 then EM78F568N must return nACK signal to slave device before send STOP signal. If STOP=1 and R/nW=0 then EM78F568N send STOP signal after receive an ACK signal. Reset when EM78F568N send STOP signal to Slave device. In slave mode, if STOP=1 and R/nW=0 then EM78F568N must return nACK signal to master device.

Bit 3(SAR_EMPTY): Set when EM78F568N transmit 1 byte data from I2C Slave Address Register and receive ACK (or nACK) signal. Reset when MCU write 1 byte data to I2C Slave Address Register.

Bit 2(ARK): The Ack condition bit is set to 1 by hardware when the device responds acknowledge (ACK). Reset when the device responds not-acknowledge (nACK) signal

Bit 1(FULL): Set by hardware when I2C receive buffer register is full. Reset by hardware when MCU read data from I2C receive buffer register.

Bit 0(EMPTY): Set by hardware when I2C transmit buffer register is empty and receive ACK (or nACK) signal. Reset by hardware when MCU write new data to I2C transmit buffer register.

6.1.88 Bank1 R24: I2CCR2 (I2C Status and Control Register2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN

Bit 7 (I2CBF): I2C Busy Flag Bit

0:clear to “0”, in Slave mode, if receive STOP signal or I2C slave address not math.

1: set when I2C communicate with master in slave mode.

Bit 6 (GCEN): I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bits 5~4: No used bits, set to 0 all the time.

Bits 3~2 (I2CTS1~I2CTS0): I2C Transmit Clock Source Select Bits (When I2CCS=0). When operating different Fm, these bits must set to correct value to let SCL clock match standard/fast mode.

I2CCR1 bit5=1, fast mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm(MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

I2CCR1 bit5=0, standard mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm(MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

Bit 1: No used bit, set to 0 all the time.

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode

1: Enable I2C mode

6.1.89 Bank1 R25: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW

Bits 7~1 (SA6~SA0): When EM78F568N used as master device for I2C application. This is the slave device address register.

Bit 0 (IRW): When EM78F568N used as master device for I2C application. This bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.90 Bank1 R26: I2CDA (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bits 7~0 (DA7~DA0): When EM78F568N used as slave device for I2C application, this register store the address of EM78F568N. It is used to identify the data on the I2C bus to extract the message delivered to the EM78F568N.

6.1.91 Bank1 R27: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Bits 7~0 (DB7~DB0): I2C Receive/Transmit Data Buffer.

6.1.92 Bank1 R28: I2CA (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DA9	DA8

Bits 7~2: unused

Bits 1~0 (DA9~DA8): high bits of device address.

6.1.93 Bank1 R29 (Unused)

6.1.94 Bank1 R2A: PWMER (PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PWMBE	PWMAE

Bits 7~2: unused bits, set to 0 all the time.

Bit 1 (PWMBE): PWM B Enable bit

0: PWM B is off (default value), and its related pin P52 carries out I/O pin function.

1: PWM B is on, and its related pin is automatically set to output.

Bit 0 (PWMAE): PWM A Enable bit.

0: PWM A is off (default value), and its related pin carries out I/O pin function

1: PWM A is on, and its related pin is automatically set to output

6.1.95 Bank1 R2B: TIMEN (Timer/PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	TBEN	TAEN

Bits 7~2: unused bits, set to 0 all the time.

Bit 1 (TBEN): Timer B enable bit

0: Timer B is off (Default)

1: Timer B is on

Bit 0 (TAEN): Timer A enable bit

0: Timer A is off (Default)

1: Timer A is on

6.1.96 Bank1 R2C~R2E: Unused

6.1.97 Bank1 R2F: PWMACR (PWM A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBA	0	0	0

Bits 7~4: unused bits, set 0 all the time

Bit 3(TRCBA): Timer A Read Control Bit

0: When this bit set to 0, the values of PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA period data

1: When this bit set to 1, READ values FROM PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA timer data

Bits 2~0: unused bits, set 0 all the time

6.1.98 Bank1 R30: PWMBCR (PWM B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBB	0	0	0

Bits 7~4: unused bits, set 0 all the time

Bit 3(TRCBB): Timer B Read Control Bit

0: When this bit set to 0, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB period data

1: When this bit set to 1, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB timer data

Bits 2~0: unused bits, set 0 all the time

6.1.99 Bank1 R31: unused

6.1.100 Bank1 R32: TACR (Timer A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TAP2	TAP1	TAP0

Bits 7~3: unused bit, set 0 all the time.

TAP2	TAP1	T1AP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1 : 4
0	1	0	1 : 8
0	1	1	1 : 16
1	0	0	1 : 32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

6.1.101 Bank1 R33: TBCR (Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TBP2	TBP1	TBP0

Bits 7~3: unused bits, set 0 all the time.

Bits 2~0 (TBP2~TBP0): Timer B Prescaler Bits

TBP2	TBP1	TBP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1 : 4
0	1	0	1 : 8
0	1	1	1 : 16
1	0	0	1 : 32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

6.1.102 Bank1 R34: unused

6.1.103 Bank1 R35: TAPRDH (Timer A Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA[9]	PRDA[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7~0(PRDA[9]~PRDA[2]): The contents of this register is a period of Timer A.

6.1.104 Bank1 R36: TBPRDH (Timer B Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7~0(PRDB[9]~PRDB[2]): The contents of this register is a period of Timer B.

6.1.105 Bank1 R37: unused

6.1.106 Bank1 R38: TADTH (Timer A Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

Bits 7~0 (DTA[9]~ DTA[2]): The contents of this register is a duty of Timer A.

6.1.107 Bank1 R39: TBDTH (Timer B Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

Bits 7~0(DTB[7]~DTB[0]): The contents of this register is a duty of Timer B.

6.1.108 Bank1 R3A: unused.

6.1.109 Bank1 R3B: PRDxL (PWM A/B/C Period Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]

Bits 7~4: unused bits, set to 0 all the time.

Bits 3~2(PRDB[1]~PRDB[0]): PWM B period buffer low bits

Bits 1~0(PRDA[1]~PRDA[0]): PWM A period buffer low bits

6.1.110 Bank1 R3C: DTxL (PWM1/2 Duty Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]

Bits 7~4: unused bits, set to 0 all the time.

Bits 3~2(DTB[1]~DTB[0]): PWM B duty buffer high bits

Bits 1~0(DTA[1]~DTA[0]): PWM A duty buffer high bits

6.1.111 Bank1 R3D~R4F(Unused)

6.1.112 Bank0 R50~R7F, Bank0~1 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 TCC/WDT & Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the TCCCR register (Bank0 R13) are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the WDTCR register (Bank0 R11) are used to determine the prescaler of WDT. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Fig. 15 depicts the circuit diagram of TCC/WDT.

Bank0 R14 (TCCDATA) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external singal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). As illustrated in Fig. 15. If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (keep in High or low level) must greater than 1CLK. **The TCC will stop running when sleep mode occurs.**

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

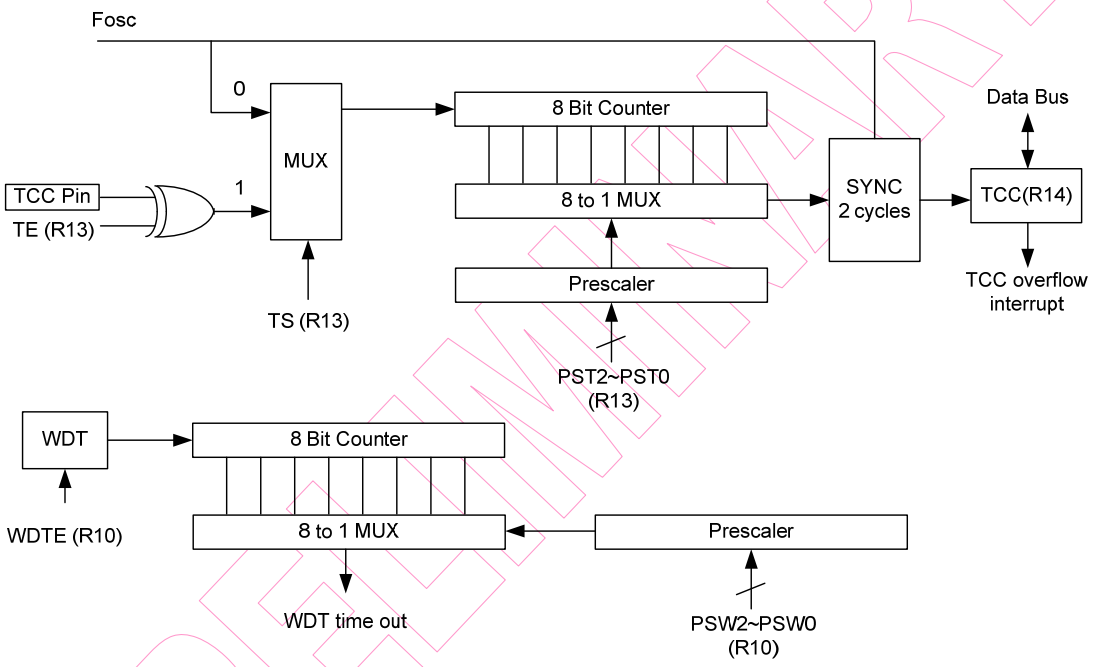


Fig. 15 Block Diagram of TCC and WDT

6.3 I/O Ports

The I/O registers, Port 5~Port 9 are bi-directional tri-state I/O ports. All have high sink/drive setting by software. Port 5, Port 6 and Port 7 also have wake up function. Further, Port 6 have input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC9).

[1] NOTE:VDD=5V, WDT time-out period = 16.5ms ± 8%. VDD=3V, WDT time-out period = 18ms ± 8%.

The I/O registers and I/O control registers are both readable and writable.

Table 3 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 input status changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before SLEEP 1. Disable WDT[2] (using very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3.1 Enable interrupt, after wake-up if “ENI” switch to interrupt vector(006H), if “DISI” execute next instruction 3.2 Disable interrupt, always execute next instruction 4. Enable wake-up enable bit 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt 4. IF Port 6 change (interrupt) → Interrupt vector (006H)

6.4 UART (Universal Asynchronous Receiver/ Transmitter)

Registers for UART Circuit

R_BANK	Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X32	**URCR1**	**URTD8**	**UMODE1**	**UMODE0**	**BRATE2**	**BRATE1**	**BRATE0**	**UTBE**	**TXE**
			R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 0	0X33	**URCR2**	0	0	**SBIM1**	**SBIM0**	**UINVEN**	0	0	0
					R/W	R/W	R/W			
Bank 0	0X34	**URS**	**URRD8**	**EVEN**	**PRE**	**PRERR**	**OVERR**	**FMERR**	**URBF**	**RXE**
			R	R/W	R/W	R	R	R	R	R/W
Bank 0	0X35	**URRD**	**URRD7**	**URRD6**	**URRD5**	**URRD4**	**URRD3**	**URRD2**	**URRD1**	**URRD0**
			R	R	R	R	R	R	R	R
Bank 0	0x36	**URTD**	**URTD7**	**URTD6**	**URTD5**	**URTD4**	**URTD3**	**URTD2**	**URTD1**	**URTD0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0D	**ISR2**	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	**UERRIF**	**RBFF**	**TBEF**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x1D	**IMR2**	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	**UERRIE**	**URIE**	**UTIE**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[2] NOTE: Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-Up function. (CODE Option Register and Bit 11 (ENWDTB-) set to “1”).

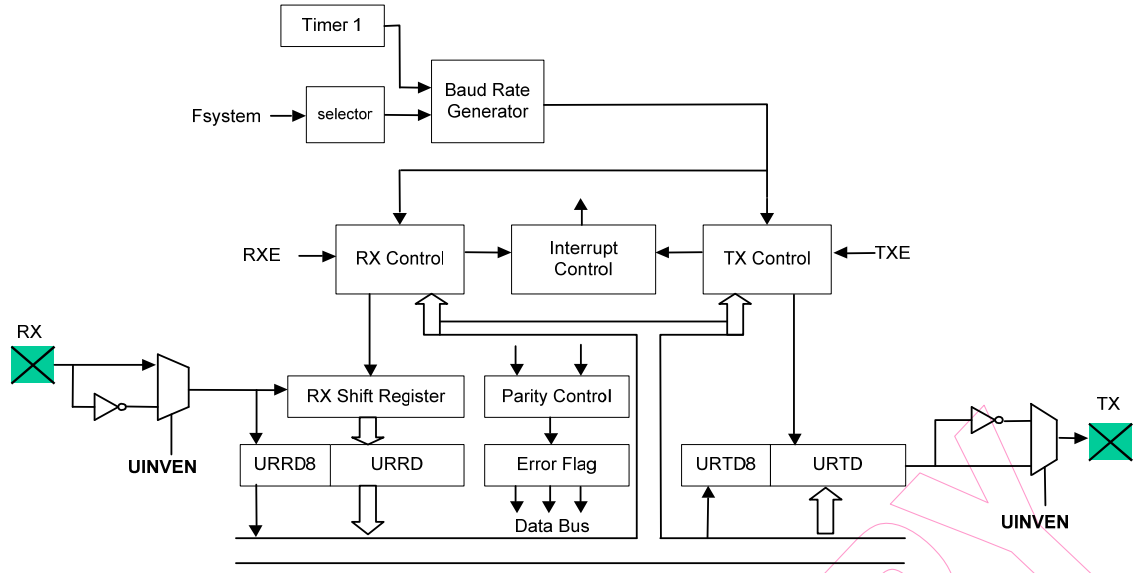


Fig. 16 Function Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three “0” are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

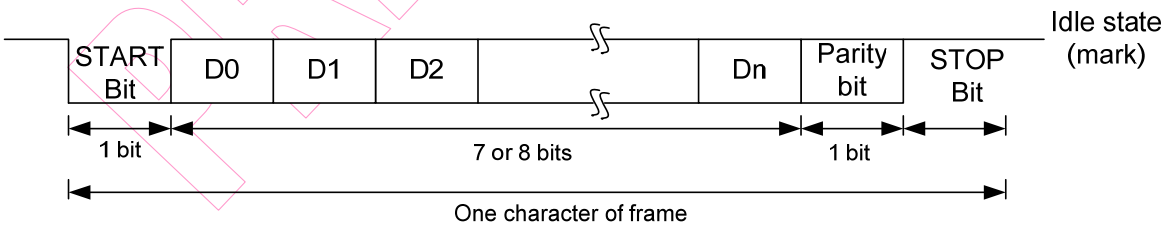


Fig. 17 Data Format in UART

6.4.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 7-18 below shows the data format in each mode.

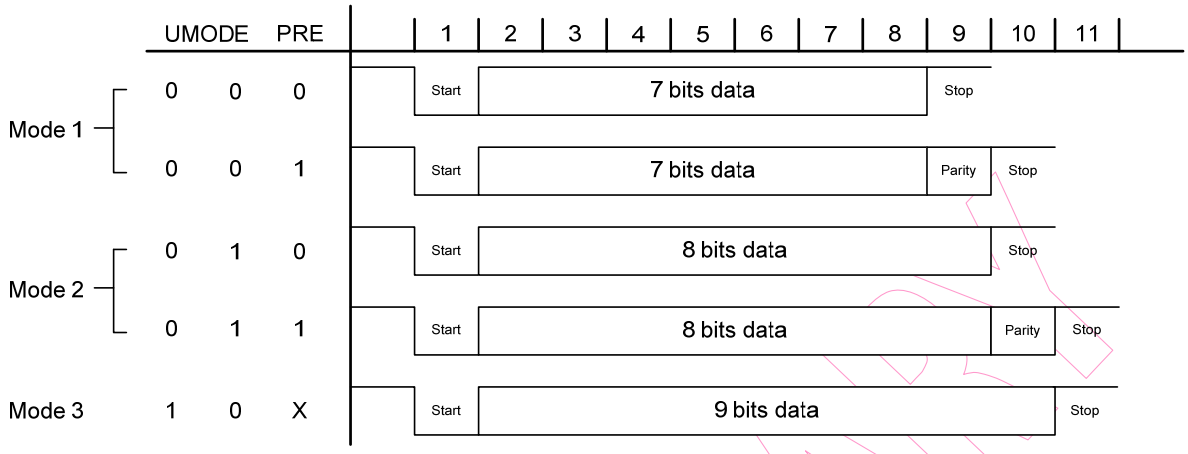


Fig. 18 UART Model

6.4.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URCR1 register will be set by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one “0” bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one “1” bit (stop bit) is output.

Mark state: output “1” continues until the start bit of the next transmitted data.
After transmitting the stop bit, the UART generates a TBEF interrupt (if enabled).

6.4.3 Receiving

In receiving, the UART operates as follows:

1. Set RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to 1. This means UART interrupt will occur.
4. The UART makes the following checks:
   (a) Parity check: The number of 1 of the received data must match the even or odd parity setting of the EVEN bit in the URS register.

(b)Frame check: The start bit must be 0 and the stop bit must be 1.

(c)Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

If any checks failed, the UERRIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software otherwise, UERRIF interrupt will occur when the next byte is received.

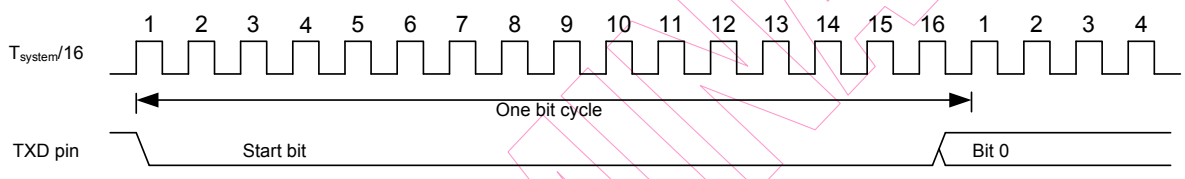
5. Read received data from URRD register. And URBF bit will be cleared by hardware.

6.4.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.
The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.4.5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

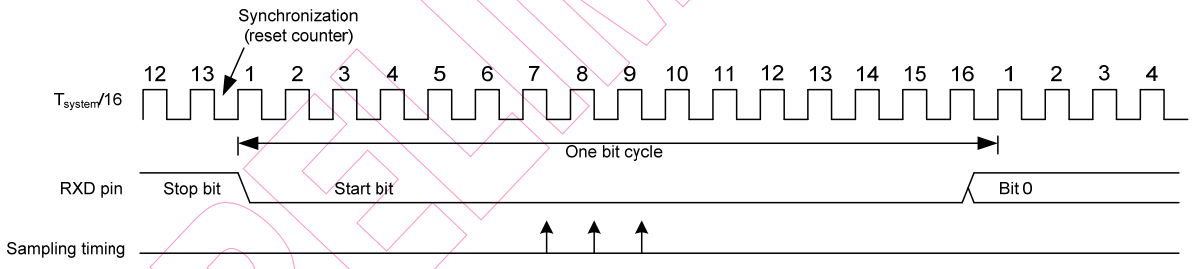


Fig. 19 UART timing

6.5 SPI function

R_BANK	Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X2B	**SPICR**	**CES**	**SPIE**	**SRO**	**SSE**	**SDOC**	**SBRS2**	**SBRS1**	**SBRS0**
			R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0X2C	**SPIS**	**DORD**	**TD1**	**TD0**	**0**	**OD3**	**OD4**	**0**	**RBF**
			R/W	R/W	R	R	R/W	R/W	R	R/W
Bank 0	0X2D	**SPIR**	**SRB7**	**SRB6**	**SRB5**	**SRB4**	**SRB3**	**SRB2**	**SRB1**	**SRB0**
			R	R	R	R	R	R	R	R
Bank 0	0X2E	**SPIW**	**SWB7**	**SWB6**	**SWB5**	**SWB4**	**SWB3**	**SWB2**	**SWB1**	**SWB0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0C	**ISR1**	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x1C	**IMR1**	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.5.1 Overview & Features

Overview:

Figures 20, 21, and 22 shows how the EM78F568N communicates with other devices through SPI module. If EM78F568N is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if EM78F568N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. You can also set SPIS bit 7(DORD) to decide the SPI transmission order, SPICR bit3 (SDOC) to control SDO pin after serial data output status and SPIS bit 6 (TD1), bit 5 (TD0) decides the SDO status output delay times.

Features:

Operation in either Master mode or Slave mode,

Three-wire or four-wire full duplex synchronous communication

Programmable baud rates of communication,

Programming clock polarity, (R2B bit7)

Interrupt flag available for the read buffer full,

SPI transmission order

After serial data output SDO status select,

SDO status output delay times,

SPI handshake pin,

Up to 8 MHz (maximum) bit frequency,

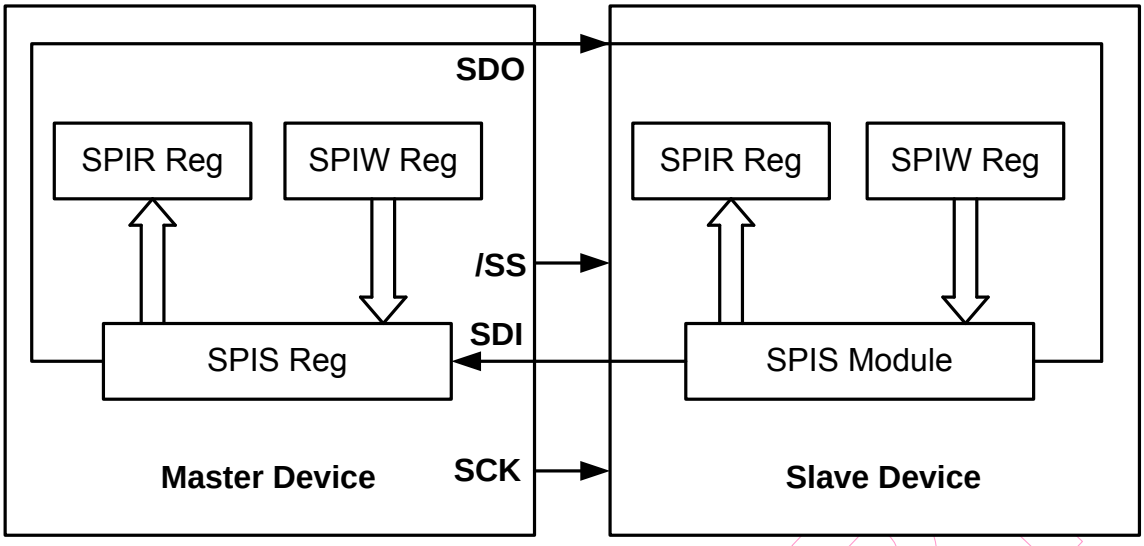


Fig. 20 SPI Master/Slave Communication

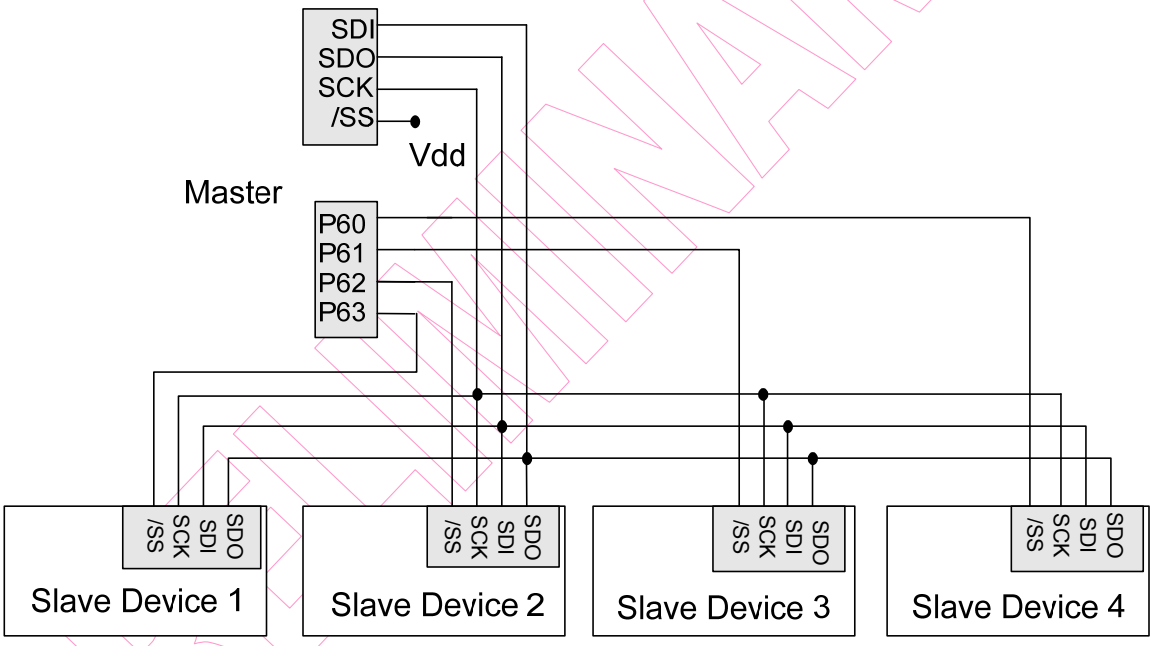


Fig. 21 The SPI Configuration of Single-Master and Multi-Slave

6.5.2 SPI Function Description

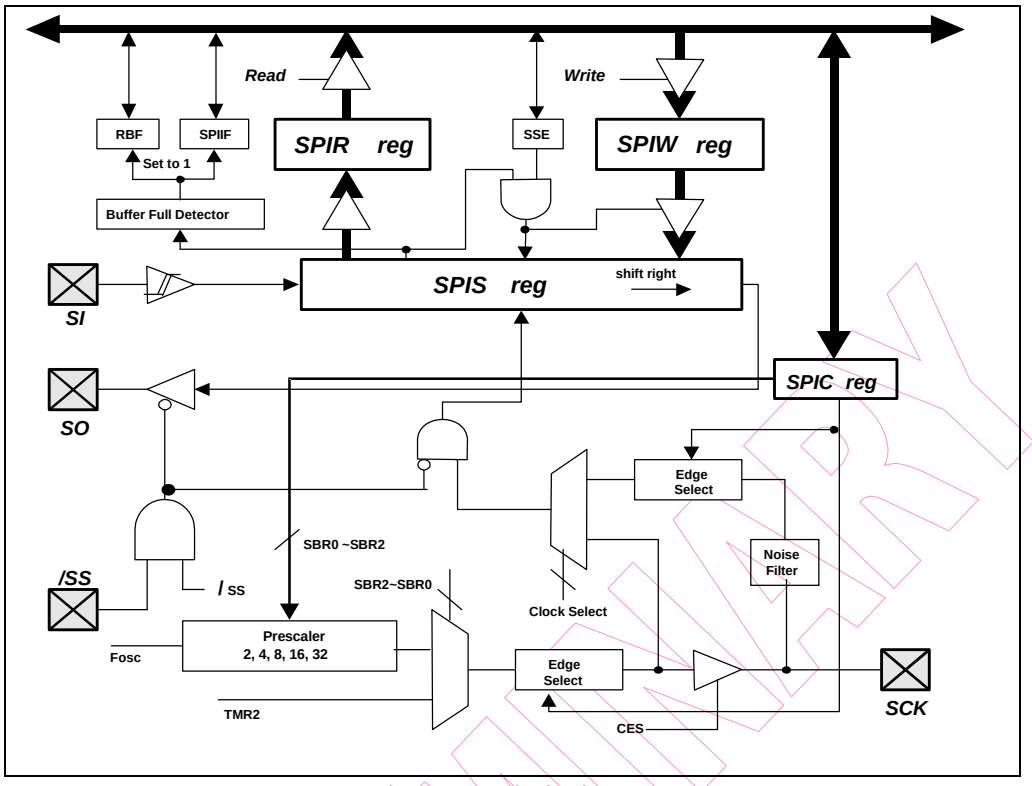


Fig. 22 SPI Block Diagram

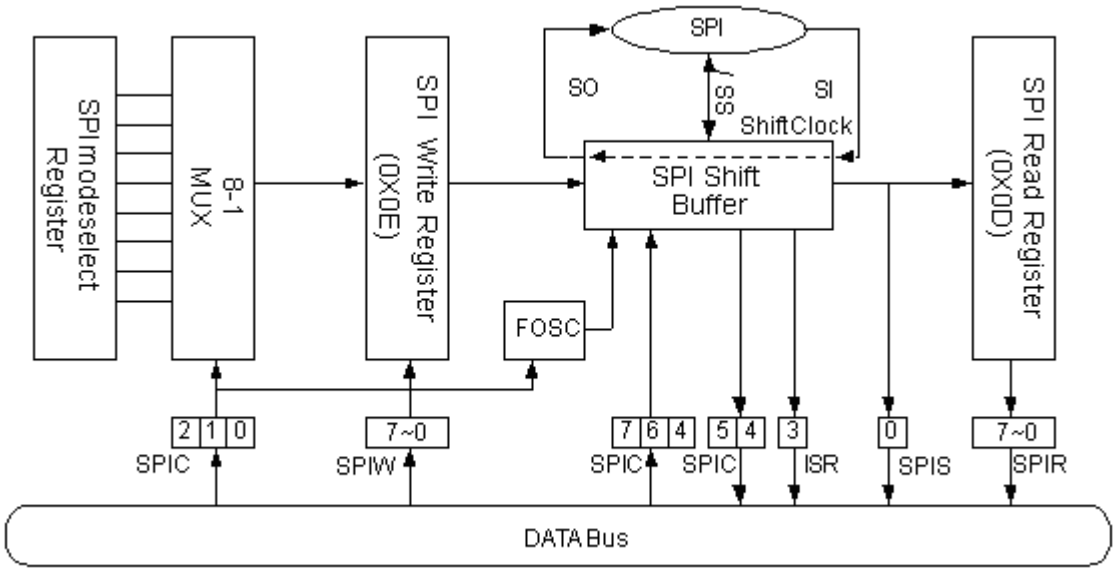


Fig. 23 The Function Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Fig. 22 and 23

- P52/RX/SI: Serial Data In
- P51/SDA/TX/SO: Serial Data Out
- P53/SCL/SCK: Serial Clock
- P50/VREF//SS: /Slave Select (Option). This pin (/SS) may be required during a slave mode
- RBF: Set by Buffer Full Detector
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed.
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shift at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIIF (SPI Interrupt) flag are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“ if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal or the external clock as the shifting clock.
- Edge Select: Selecting the appropriate clock edges by programming the CES bit

6.5.3 SPI Signal & Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

P52/RX/SI:

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected

- Program the same clock rate and clock edge to latch on both the master and slave devices
- The byte received will update the transmitted byte
- The RBF will be set as the SPI operation is completed
- Timing is shown in Figures Fig. 24 and 25.

P51/SDA/TX/SO:

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- The CES bit will be reset, as the SPI operation is completed
- Timing is shown in Fig. 24 and 25

P53/SCL/SCK:

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SI and SO pins
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode
- Timing is show in Fig. 24 and 25

P50/VREF//SS:

- Slave Select; negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignores the data on the SI and SO pins while /SS is high, because the SO is no longer driven
- Timing is shown in Fig. 24 and 25

6.5.4 SPI Mode Timing

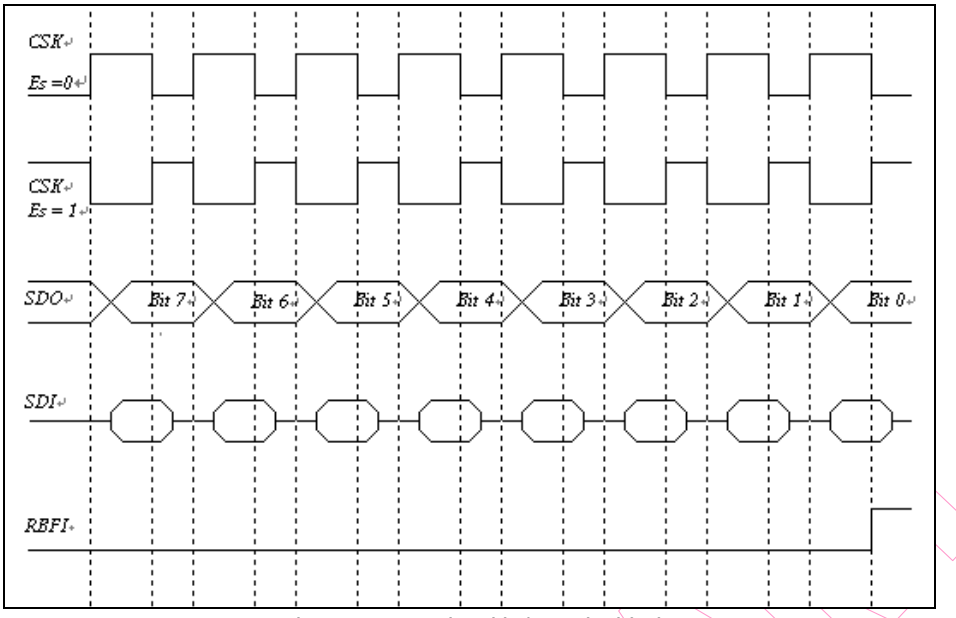


Fig. 24 SPI Mode with /SS Disabled

The SCK edge is selected by programming bit CES. The waveform shown in Fig. 24 is applicable regardless of whether the EM78F568N is in master or slave mode with /SS disabled. However, the waveform in Fig. 25 can only be implemented in slave mode with /SS enabled.

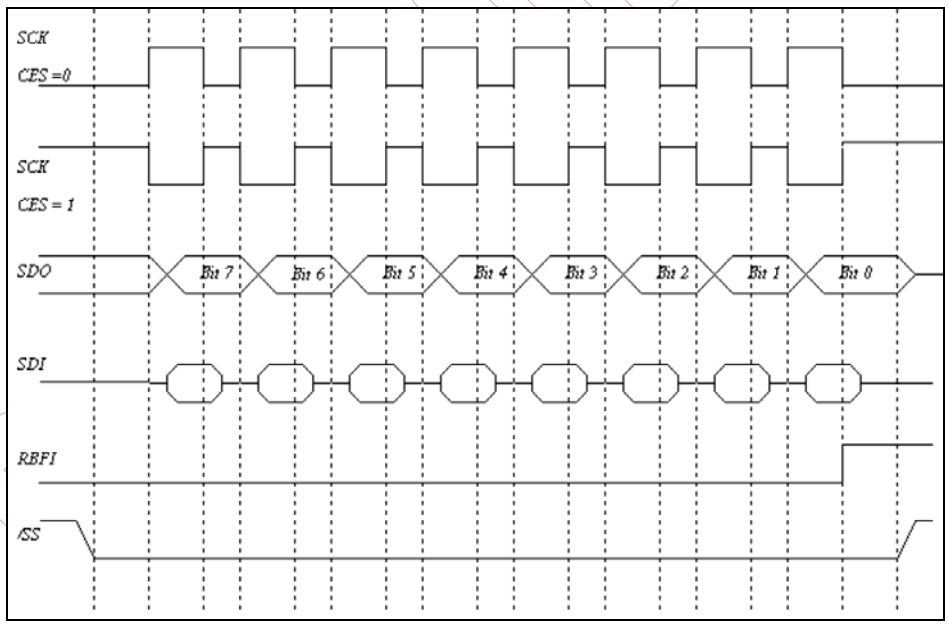


Fig. 25 SPI Mode with /SS Enabled

6.6 I2C function

Registers for I2C Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X23	**I2CCR1**	**Strobe/Pend**	**IMS**	**ISS**	**STOP**	**SAR_EMPTY**	**ACK**	**FULL**	**EMPTY**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X24	**I2CCR2**	0	0	0	0	**I2CTS1**	**I2CTS0**	**I2CCS**	**I2CEN**
			R	R	R	R	R/W	R/W	R/W	R/W
Bank 1	0X25	**I2CSA**	**SA6**	**SA5**	**SA4**	**SA3**	**SA2**	**SA1**	**SA0**	**IRW**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X26	**I2CDA**	**DA7**	**DA6**	**DA5**	**DA4**	**DA3**	**DA2**	**DA1**	**DA0**
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X27	**I2CDB**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X28	**I2CA**	**0**	**0**	**0**	**0**	**0**	**0**	**DA9**	**DA8**
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISR3**	0	0	0	0	0	PWMCIF	**I2CRIF**	**I2CTIF**
			R	R	R	R	R	R/W	R/W	R/W
Bank 0	0x1E	**IMR3**	0	0	0	0	0	PWMCIE	**I2CRIE**	**I2CTIE**
			R	R	R	R	R	R/W	R/W	R/W

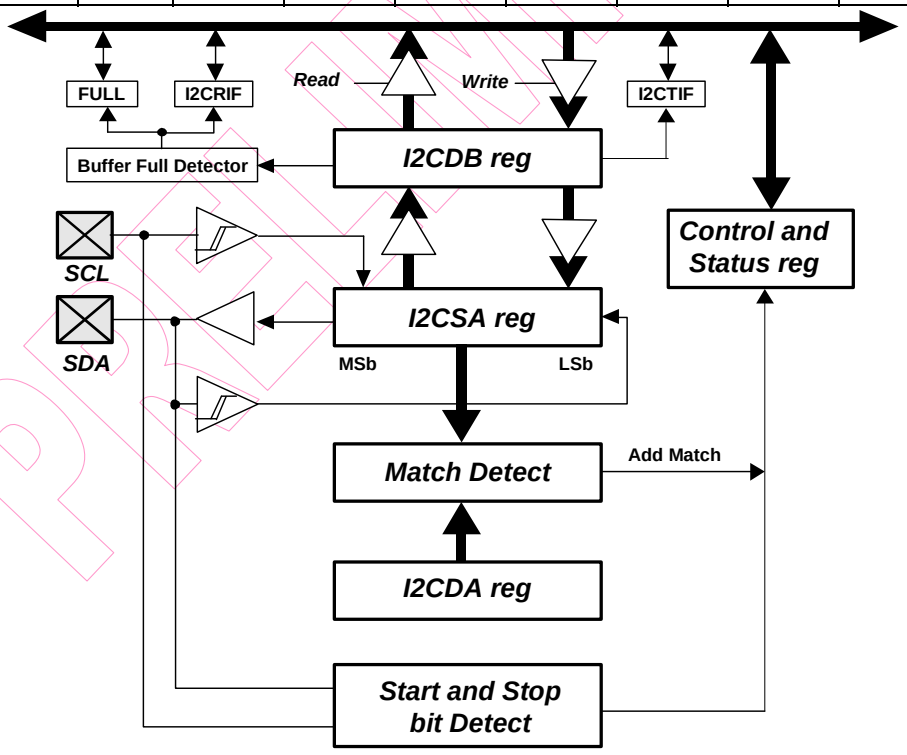


Fig. 26 I2C Block Diagram

The EM78F568N supports a bidirectional, 2-wire bus, 7-bits & 10-bits addressing and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode or up to 400 kbit/s in the Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Within the procedure of the I2C bus, unique situations arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

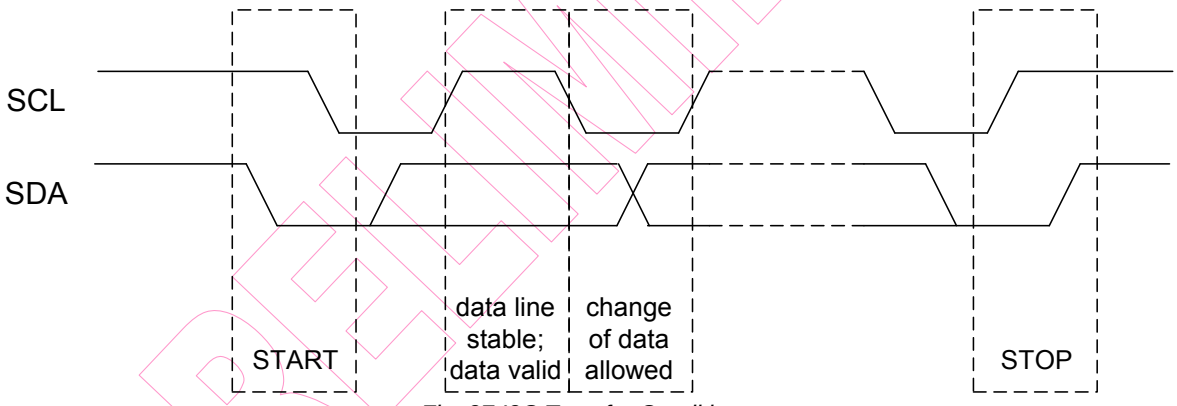


Fig. 27 I2C Transfer Condition

Master-transmitter transmits to slave-receiver. The transfer direction is not changed.

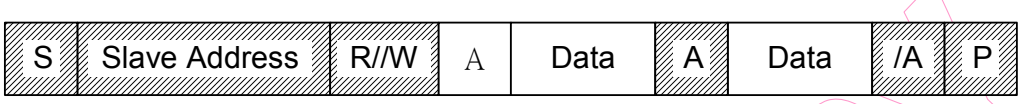
Master reads slave immediately after first byte. At the moment of the first acknowledge, the master- transmitter becomes a master- receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The STOP condition is generated by the master, which has previously sent a not-acknowledge (A).

'0' Write — data transferred (n byte + acknowledge)

Master to Slave

Slave to Master

A = acknowledge (SDA low)
/A = not acknowledge (SDA high)
S = Start
P = Stop



'1' Read — data transferred (n byte + acknowledge)

6.6.1 Master Mode

In transmitting serial data, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable I2C master function.
3. Write slave address into the I2CSA register and IRW bit to select read or write.
4. Set strobe bit will start transmit and then Check SAR_EMPTY bit.
5. Write 1st data into the I2CDB register, set strobe bit and Check EMPTY bit.
6. Write 2nd data into the I2CDB register, set strobe bit, STOP bit and Check EMPTY bit.

6.6.2 Slave Mode

In receiving, the I2C operates as follows:

1. Set I2CTS1~0, I2CCS and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable I2C slave function.
3. Write device address into the I2CDA register.
4. Check FULL bit, read I2CDB register (address) and then clear Pend bit.
5. Check FULL bit, read I2CDB register (1st data) and then clear Pend bit.
6. Check FULL bit, read I2CDB register (2nd data) and then clear Pend bit.

6.7 A/D converter

Registers for AD Converter Circuit

R_BANK	Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X24	**ADCR1**	**VREFS**	**ADRUN**	**ADPD**	**0**	**0**	**ADIS2**	**ADIS1**	**ADIS0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x25	**ADCR2**	**CALI**	**SIGN**	**VOF2**	**VOF1**	**VOF0**	**CKR2**	**CKR1**	**CKR0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X26	**ADICL**	**ADE7**	**ADE6**	**ADE5**	**ADE4**	**ADE3**	**ADE2**	**ADE1**	**ADE0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X29	**ADDH**	**ADD11**	**ADD10**	**ADD9**	**ADD8**	**ADD7**	**ADD6**	**ADD5**	**ADD4**
			R	R	R	R	R	R	R	R
Bank 0	0X2A	**ADDL**	**0**	**0**	**0**	**0**	**ADD3**	**ADD2**	**ADD1**	**ADD0**
			-	-	-	-	R	R	R	R
Bank 0	0X1C	**IMR1**	**LVDIE**	**ADIE**	**SPIE**	**PWMBIE**	**PWMAIE**	**EXIE**	**ICIE**	**TCIE**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0C	**ISR1**	**LVDIF**	**ADIF**	**SPIF**	**PWMBIF**	**PWMAIF**	**EXIF**	**ICIF**	**TCIF**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x2F	**WUCR1**	**0**	**0**	**LVDWE**	**ICWE**	**ADWE**	**CMP2WE**	**CMP1WE**	**EXWE**
			R	R	R/W	R/W	R/W	R/W	R/W	R/W

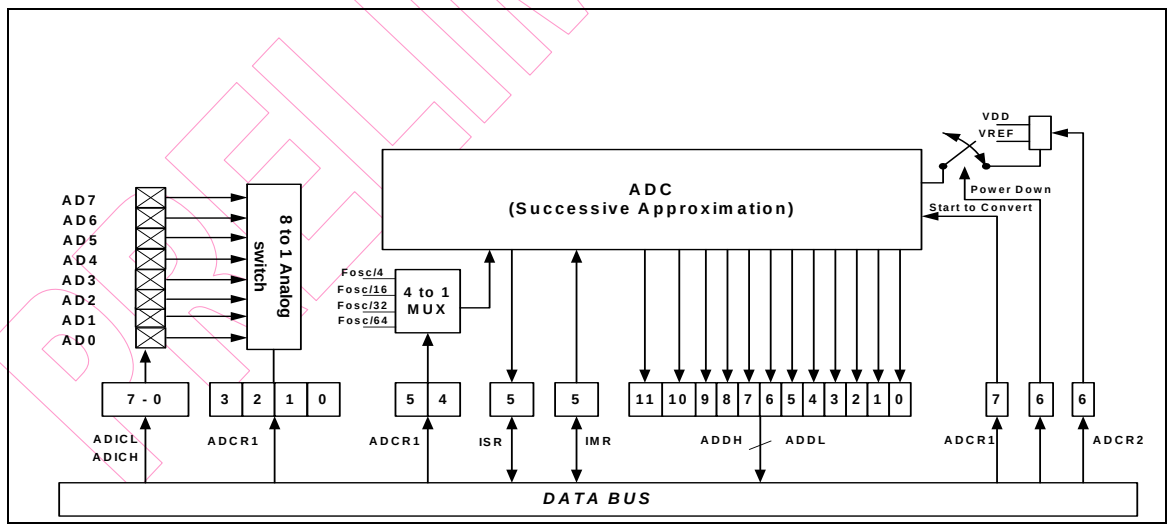


Fig. 28 AD Converter

This is a 12-bit successive approximation type AD converter. The upper side of analog reference voltage can select either internal VDD or external input pin P50 (VREF) by

setting the VREFS bit in ADCR1. Connecting to external VREF is more accuracy than internal VDD.

6.7.1 ADC Data Register

When the A/D conversion is completed, the result is loaded to the ADDH (8-bit) and ADDL (4-bit). The START/END bit is cleared, and the ADIF is set.

6.7.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at VDD =5V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

6.7.3 A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of A/D conversion. For the eKTR8750, the conversion time per bit is about 4μs. Table 5 shows the relationship between Tct and the maximum operating frequencies.

Table 5

CKR2~CKR0	Operation Mode	Max. Frequency (Fc)	Max. Conversion Rate per Bit	Max. Conversion Rate
000	Fosc/4	4MHz	1MHz (1μs)	15us(66.66kHz)
001	Fosc/1	1MHz	1MHz (1μs)	15us(66.66kHz)
010	Fosc/2	2MHz	1MHz (1μs)	15us(66.66kHz)
011	Fosc/8	8MHz	1MHz (1μs)	15us(66.66kHz)
100	Fosc/16	16MHz	1MHz (1μs)	15us(66.66kHz)
101	Fosc/32	32MHz	1MHz (1μs)	15us(66.66kHz)
110	Fosc/64	64MHz	1MHz (1μs)	15us(66.66kHz)
111	Internal RC		1MHz (1μs)	15us(66.66kHz)

6.8 PWM

6.8.1 Overview

In PWM mode, PWMA, PWMB pins produce up to a 10-bit resolution PWM output (see Fig.29 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Fig. 29 depicts the relationships between a period and a duty cycle.

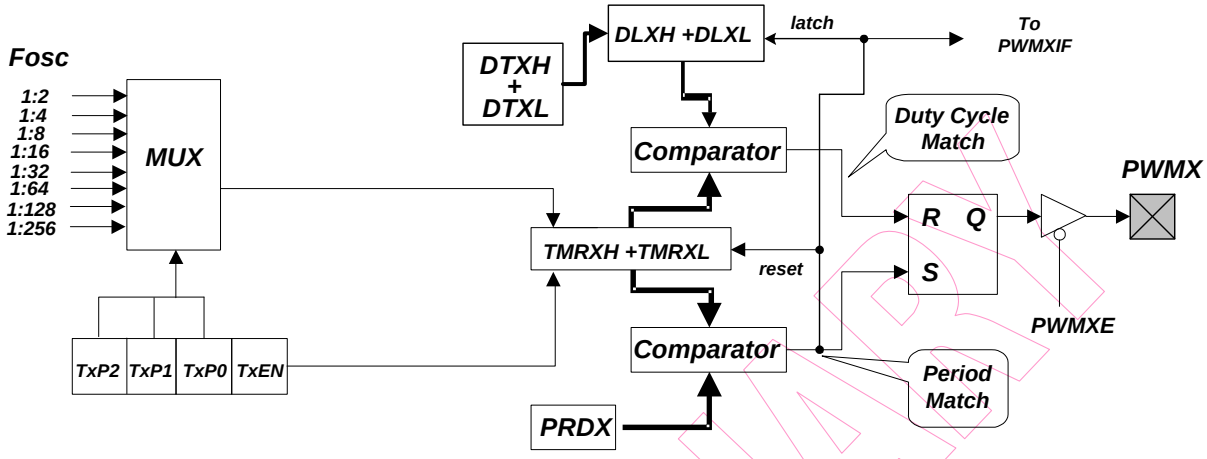


Fig. 29 The Functional Block Diagram of the Three PWMs

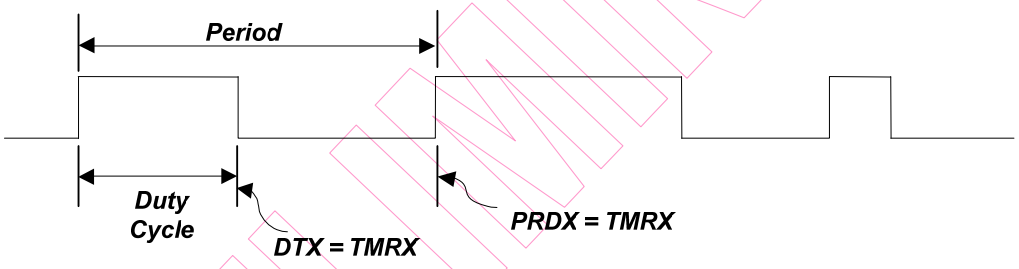


Fig. 30 The Output Timing of the PWM

6.8.2 Increment Timer Counter (TMRX: TMRAH/TWRAL or TMRBH/TWRBL)

TMRX are 10-bits clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX just can be read only. If employed, they can be turned down for power saving by setting TXEN bits to 0.

6.8.3 PWM Period (PRDX: PRDA, PRDB)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

• TMRX is cleared.

• The PWMX pin is set to 1.

• The PWM duty cycle is latched from DTXL/DTXH to DLXL/DLXH.

< Note > The PWM output will not be set, if the duty cycle is 0;

• The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM period:

PERIOD = (PRDX + 1) * (1/Fosc) * (TMRX prescale value)

Ex. PRDX=49; Fosc=4MHz; TMRX(0,0,0)=1:2,

then PERIOD=(49 + 1) * (1/4M) * 2/2 * 2 =25us

6.8.4 PWM Duty Cycle (DTX: DTXH/ DTXL; DLX: DLXH/DLXL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX) * (1/Fosc) * (TMRX prescale value)

Ex. DTX=10; Fosc=4MHz; TMRX(0,0,0)=1:2, then Duty Cycle=10 * (1/4M) * 2/2 * 2 =5us

6.9 RESET and Wake-up

6.9.1. RESET

A RESET is initiated by one of the following events-

(1) Power on reset.

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approx. 18ms[3] (one oscillator start-up timer period) after the reset is detected. And if the /Reset pin goes “low” or WDT time-out is active, a reset is generated, in RC mode the reset time is 34clocks, High XTAL mode reset time is 2ms and 32clocks. In low XTAL mode, the reset time is 500ms. Once the RESET occurs, the following functions are performed. Refer to Fig.18.

• The oscillator is running, or will be started.

• The Program Counter (R2) is set to all "0".

• All I/O port pins are configured as input mode (high-impedance state).

• The Watchdog timer and prescaler are cleared.

• The bits of the control register are set as Table 4.

[3] NOTE: Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up generated, in RC mode the wake-up time is 34clocks, High XTAL mode wake-up time is 2ms and 32clocks. In low XTAL mode, the wake-up time is 500 ms.The controller can be awakened by-

(1) External reset input on /RESET pin,

(2) WDT time-out (if enabled), or

(3) External (P60,/INT) pin changes (if EXWE is enabled).

(4) Port 6 input status changes (if ICWE is enabled).

(5) Comparator 1/2 output status change (if CMP1WE/CMP2WE is enabled).

(6) A/D conversion completed (if ADWE is enabled).

(7) SPI received data, When SPI act as slave device (if SPIWE is enabled).

(8) Port 5 / Port 7 input status changes(if corresponding control bits is enabled)

The first two cases will cause the EM78F568N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3,4,5,6,7 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 0x3, 0x6, 0X15,0X30 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Case 8 has no interrupt. All of the sleep mode, wake up time is 150us, no matter what’s oscillation mode (except low XTAL mode). In low XATL mode, wake up time is 500ms.

Only one of the Cases 2 to 6 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM78F568N can be wake-up only by Case 1 or 2. Refer to the section on Interrupt for further details.

[b] If External (P60,/INT) pin change is used to wake-up EM78F568N and EXWE bit is enabled before SLEP, WDT must be disabled. Hence, the EM78F568N can be wake-up only by Case 3.

[c] If Port 6 Input Status Change is used to wake-up EM78F568N and corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM78F568N can be wake-up only by Case 4.

[d] If Comparator 1/2 output status change is used to wake-up EM78F568N and CMP1WE/CMP2WE bit of Bank0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N can be wake-up only by Case 5

[e] If AD conversion completed is used to wake-up EM78F568N and ADWE bit of Bank0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N can be wake-up only by Case 6.

[f] When SPI act as slave device, after received data will wake-up EM78F568N and SPIWE bit of Bank0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N can be wake-up only by Case 7.

All kind of the wake-up mode and interrupted mode showed as below:

Wakeup signal	*Sleep mode*	*Idle mode*	*Green mode*	*Normal mode*
External interrupt	If enable EXWE bit : Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable EXWE bit Wake-up+ interrupt (if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
Port 6 pin change	If enable ICWE bit : Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable ICWE bit Wake-up+ interrupt (if interrupt enable)+ next instruction	Interrupt(if interrupt enable) or next instruction	Interrupt(if interrupt enable) or next instruction
TCC overflow interrupt	X	Wake-up+ interrupt(if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
SPI interrupt	If enable SPIWE bit : Wake-up+ interrupt (if interrupt enable)+ next instruction **SPI must be slave mode**	If enable SPIWE bit Wake-up+ interrupt(if interrupt enable)+ next instruction **SPI must be slave mode**	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
Comparator 1/2 (Comparator Output Status Change)	If enable CMP1WE/ CMP2WE bit : Wake-up+ interrupt (if interrupt enable)+ next instruction	If enable CMP1WE/ CMP2WE bit: Wake-up+ interrupt (if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
TC1 interrupt	X	Wake-up+ interrupt(if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
UART Transmit complete interrupt	X	X	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
UART Receive data buffer full interrupt	X	X	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
UART Receive error interrupt	X	X	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
TC2 interrupt	X	Wake-up+ interrupt(if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
TC3 interrupt	X	Wake-up+ interrupt(if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
PWMA / B (When TimerA/B Match PRDA/B)	X	Wake-up+ interrupt(if interrupt enable)+ next instruction	interrupt(if interrupt enable) or next instruction	interrupt(if interrupt enable) or next instruction
AD conversion complete interrupt	If enable ADWE bit : Wake-up+ interrupt(if interrupt enable)+ next instruction **Fs and Fm don't stop**	If enable ADWE bit Wake-up+ interrupt(if interrupt enable)+ next instruction **Fs and Fm don't stop**	interrupt(if interrupt enable) or next instruction **Fs and Fm don't stop**	interrupt(if interrupt enable) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

After wake up:
1. If interrupt enable → interrupt+ next instruction
2. If interrupt disable → next instruction

Table 4 The Summary of the Initialized Values for Registers

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	0	SBS0	0	0	0	GBS0
		Power-On	0	0	0	U	0	0	0	U
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	P	0	0	0	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	0	0	0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	0	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X05	BANK 0, R5 (PORT 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	BANK 0, R6 (PORT 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	BANK 0, R7 (PORT 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x08	BANK 0, R8	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	(PORT 8)	/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09	BANK 0, R9 (PORT 9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0B	BANK 0, RB (OMCR)	Bit Name	CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	TCSS
		Power-On	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	BANK 0, RC (ISR1)	Bit Name	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0D	BANK 0, RD (ISR2)	Bit Name	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	BANK 0, RE (ISR3)	Bit Name	0	0	0	0	I2CDTPIF	0	I2CRIF	I2CTIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x10	BANK 0, R10 EIESCR	Bit Name	0	0	0	0	0	0	0	EIES
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	0	0	P
0x11	BANK 0, R11 WDTCR	Bit Name	WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	0	P	P	P	P
0x12	BANK 0, R12	Bit Name	0	0	0	0	LVDEN	/LVD	LVD1	LVD0
		Power-On	0	0	0	0	0	R	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	LVDCR	/RESET and WDT	0	0	0	0	0	R	0	0
		Wake-Up from Pin Change	0	0	0	0	P	R	P	P
0X13	BANK 0, R13 TCCCR	Bit Name	0	TCCS	TS	TE	PSTE	PST2	PST1	PST0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P
0X14	BANK 0, R14 TCCDATA	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X15	BANK 0, R15 IOCR5	-	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X16	BANK 0, R16 IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X17	BANK 0, R17 IOCR7	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X18	BANK 0, R18 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X19	BANK 0, R19 IOCR9	Bit Name	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1C	BANK 0, R1C IMR1	Bit Name	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1D	BANK 0, R1D IMR2	Bit Name	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1E	BANK 0, R1E IMR3	Bit Name	0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X20	BANK 0, R20 P5WUCR	Bit Name	WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X21	BANK 0, R21 P5WUECR	Bit Name	WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X22	BANK 0, R22 P7WUCR	Bit Name	WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X23	BANK 0, R23 P7WUECR	Bit Name	WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X24	BANK 0, R24 ADCR1	Bit Name	VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X25	BANK 0, R25 ADCR2	Bit Name	CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X26	BANK 0, R26 ADICL	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X29	BANK 0, R29 ADDH	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2A	BANK 0, R2A ADDL	Bit Name	0	0	0	0	AD3	AD2	AD1	AD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P
0X2B	BANK 0, R2B SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2C	BANK 0, R2C SPIS	Bit Name	DORD	TD1	TD0	0	OD3	OD4	0	RBF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	0	P	P	0	P
0X2D	BANK 0, R2D SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2E	BANK 0, R2E SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2F	BANK 0, R2F WUCR1	Bit Name	0	SPIWE	LVDWE	ICWE	ADWE	CMP2WE	CMP1WE	EXWE
		Power-On	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P
0X32	BANK 0, R32 URCR1	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-On	U	0	0	0	0	0	1	0
		/RESET and WDT	P	0	0	0	0	0	1	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X33	BANK 0, R33 URCR2	Bit Name	0	0	SBIM1	SBIM0	UINVEN	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	0	0	0
0X34	BANK 0, R34 URS	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-On	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X35	BANK 0, R35 URRD	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X36	BANK 0, R36 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X37	BANK 0, R37 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X38	BANK 0, R38 TBPTH	Bit Name	HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X39	BANK 0, R39	Bit Name	C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CMP1CR	Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X3C	BANK 0, R3C CMP2CR	Bit Name	C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	0	0	P	P	0	0
0X43	BANK 0, R43 CPIRLCON	Bit Name	BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X48	BANK 0, R48 TC1CR	Bit Name	TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	0	0
0X49	BANK 0, R49 TCR1DA	Bit Name	TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4A	BANK 0, R4A TCR1DB	Bit Name	TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4B	BANK 0, R4B T2CR	Bit Name	0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P
0X4C	BANK 0, R4C TCR2DH	Bit Name	TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4D	BANK 0, R4D TCR2DL	Bit Name	TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4E	BANK 0, R4E TC3CR	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X4F	BANK 0, R4F TC3RD	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X05	BANK 1, R5 P5PHCR	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X06	BANK 1, R6 P6PHCR	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X07	BANK 1, R7 P7PHCR	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X08	BANK 1, R8 P8PHCR	Bit Name	/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X09	BANK 1,	Bit Name	/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	R9 P9PHCR	Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0B	BANK 1, RB P5PLCR	Bit Name	/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0C	BANK 1, RC P6PLCR	Bit Name	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0D	BANK 1, RD P7PLCR	Bit Name	/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0E	BANK 1, RE P8PLCR	Bit Name	/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X0F	BANK 1, RF P9PLCR	Bit Name	/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X11	BANK 1, R11 P5HD/SCR	Bit Name	/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X12	BANK 1, R12 P6HD/SCR	Bit Name	/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X13	BANK 1, R13 P5HD/SCR	Bit Name	/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X14	BANK 1, R14 P5HD/SCR	Bit Name	/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X15	BANK 1, R15 P5HD/SCR	Bit Name	/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X17	BANK 1, R17 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X18	BANK 1, R18 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X19	BANK 1, R19 P7ODCR	Bit Name	OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1A	BANK 1, R1A P8ODCR	Bit Name	OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1B	BANK 1, R1B P9ODCR	Bit Name	OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X1D	BANK 1, R1D IRCS	Bit Name	0	0	RCM1	RCM0	0	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X23	BANK 1, R23 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
		Power-On	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X24	BANK 1, R24 I2CCR2	Bit Name	I2CBF	GCEN	0	0	I2CTS1	I2CTS0	I2CCS	I2CEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P
0X25	BANK 1, R25 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X26	BANK 1, R26 I2CDA	Bit Name	0	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X27	BANK 1, R27 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X28	BANK 1, R28 I2CA	Bit Name	0	0	0	0	0	0	DA9	DA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X2A	BANK 1, R2A PWMER	Bit Name	0	0	0	0	0	0	PWMBE	PWMAE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X2B	BANK 1, R2B TIMEN	Bit Name	0	0	0	0	0	0	TBEN	TAEN
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X2F	BANK 1, R2F PWMACR	Bit Name	0	0	0	0	TRCBA	0	0	0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	P	0	0	0
0X32	BANK 1, R32 TACR	Bit Name	0	0	0	0	0	TAP2	TAP1	TAP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X33	BANK 1, R33 TBCR	Bit Name	0	0	0	0	0	TBP2	TBP1	TBP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	P	P	P
0X35	BANK 1, R35 TAPRDL	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X36	BANK 1, R36 TBPRDL	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X38	BANK 1, R38 TADT	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X39	BANK 1, R38 TBDT	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0X3B	BANK 1, R3B PRDxL	Bit Name	0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P
0X3C	BANK 1, R3C DTxL	Bit Name	0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	P	P	P	P	P	P

U: Unknown or don't care. P: Previous value before reset. t: Check Table 5

6.9.2. The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1. A power-on condition,
2. A high-low-high pulse on /RESET pin, and
3. Watchdog timer time-out.

The values of T and P, listed in Table 5 are used to check how the processor wakes up. Table 5 shows the events that may affect the status of T and P.

Table 5 The Values of RST, T and P after RESET

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous status before reset

Table 6 The Status of T and P Being Affected by Events.

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous value before reset

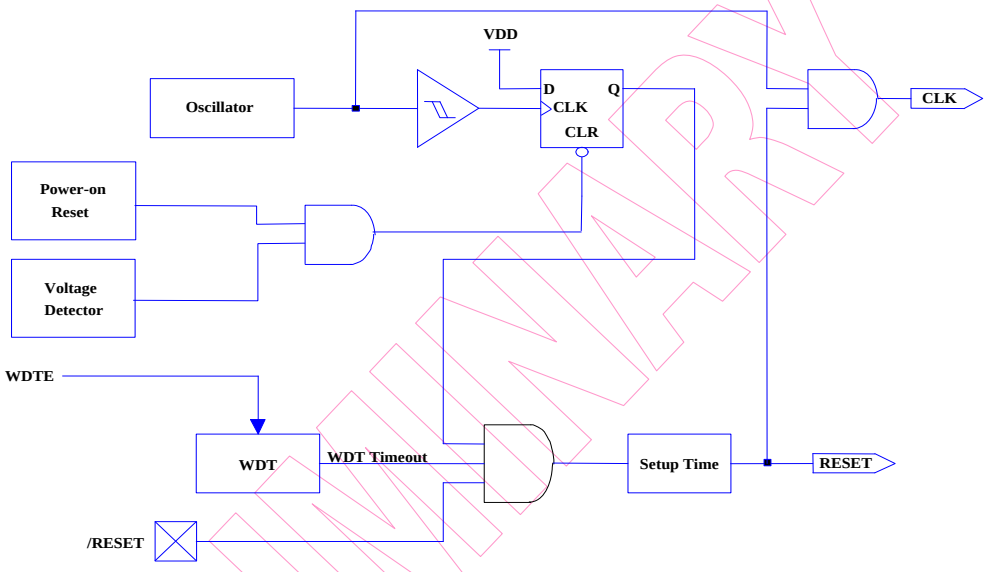


Fig. 31 Block Diagram of Controller Reset

6.10 Interrupt

The EM78F568N has 14 interrupts (3 external, 11 internal) listed below:

Interrupt Source		Enable Condition	Int. flag	Int. vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDIF	000C	4
External	Comparator1	ENI+CMP1IE=1	CMP1IF	000F	5
Internal	SPI	ENI + SPIIE=1	SPIIF	0012	6
External	Comparator2	ENI+CMP2IE=1	CMP2IF	0015	7
Internal	TC1	ENI + TC1IE=1	TC1IF	0018	8
Internal	UART Transmit	ENI + UTIE=1	TBEF	001B	9
Internal	UART Receive	ENI + URIE=1	RBFF	001E	10
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	0021	11
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	12
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	13
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	14
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	15
Internal	AD	ENI + ADIE=1	ADIF	0030	16
Internal	I2C Transmit	ENI+ I2CTIE	I2CTIF	0036	17
Internal	I2C Receive	ENI+ I2CRIE	I2CRIF	0039	18
Internal	I2C Stop	ENI+ I2CSTPIE	I2CSTPIF	003F	19

Bank0 RC~RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank0 R1C~R1F is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt equipped with digital noise rejection circuit (input pulse less than **8 system clocks time** is eliminated as noise), **but in Low XTAL oscillator (LXT) mode the noise rejection circuit will be disable.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC,R3 and R4 will be pushed back.

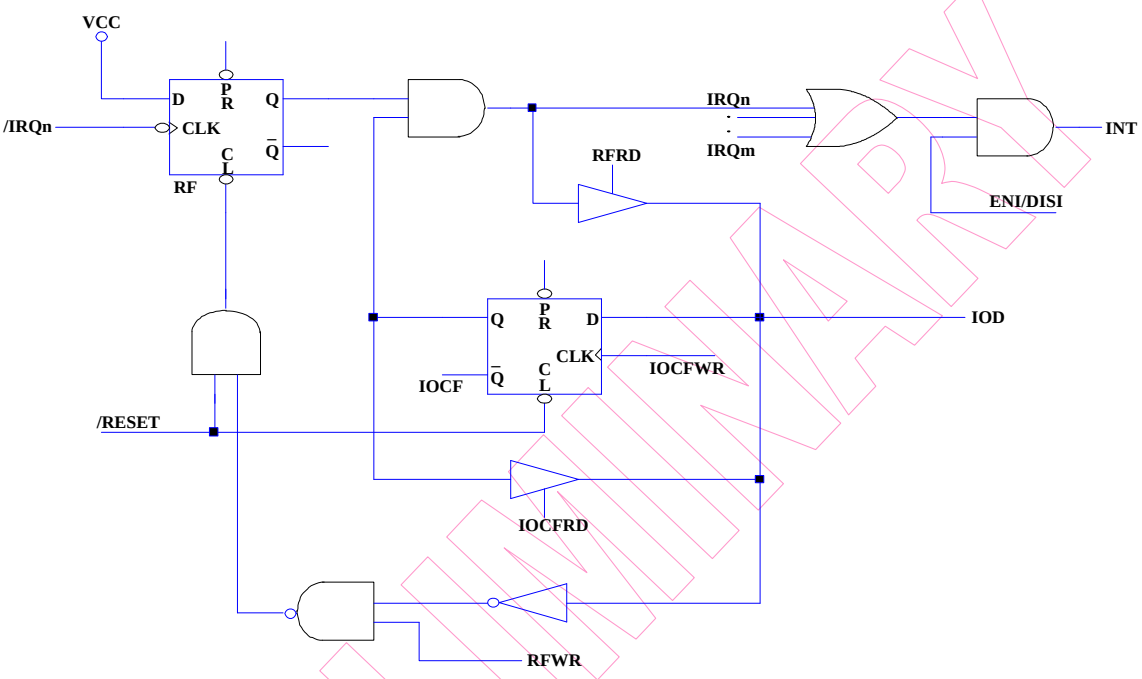


Fig. 32 Interrupt Input Circuit

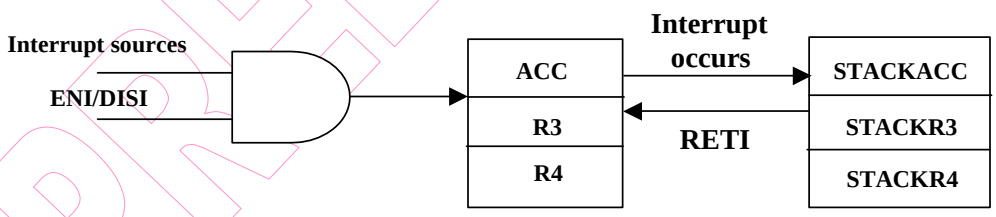


Fig. 33 Interrupt backup diagram

6.11 LVD (Low Voltage Detector)

During the power source unstable situation, such like external power noise interference or EMS test condition, it will cause the power vibrate fierce. At the time the Vdd is unsettled, it maybe below working voltage. When system voltage, Vdd, below the working voltage, the IC kernel must keep all register status automatically.

LVD property is setting at Bank0 R12, Bit 1,0 detail operation mode as following :

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bits 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level control Bits.

The LVD status and interrupt flag is refer to Bank0 RC

"1" means interrupt request, and "0" means no interrupt occurs.

Bit 7 (LVDIF): Low voltage Detector interrupt flag.

When LVD1, LVD0 = "0,0", Vdd > 2.2V, LVDIF is "0", Vdd<= 2.2V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "0,1", Vdd > 3.3V, LVDIF is "0", Vdd<= 3.3V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1,0", Vdd > 4.0V, LVDIF is "0", Vdd<= 4.0V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1,1", Vdd > 4.5V, LVDIF is "0", Vdd<= 4.5V, set LVDIF to "1". LVDIF reset to "0" by software.

The following steps are needed to setup the LVD function:

1. Set the LVDEN to "1", then use Bit 1,0 (LVD1, LVD0) of Register RB to set LVD interrupt level

2. Waiting for LVD occur interrupt.

3. Clear LVD interrupt flag

The internal LVD module is using internal circuit to fit. When you set the LVDEN to enable the LVD module. The current consumption will increase about 10uA.

During the sleep mode, the LVD module continues to operate. If the device voltage drop slowly and crosses the detect point. The LVDIF bit will be set and the device won't wake-up from Sleep mode. Until the others wake-up source to wake-up EM78F568N, the LVD interrupt flag still set as the prior status.

When system reset, the LVD flag will be clear.

The Figure 20 shows the LVD module to detect the external voltage situation.

When Vdd drop not below V_{LVD}, LVDIF keep at "0".

When Vdd drop below V_{LVD}, LVDIF set to “1”. If global ENI enable, LVDIF will be set to “1”, the next instruction will branched to interrupt vector. The LVD interrupt flag clear to “0” by software.

When Vdd drop below V_{RESET} and less than 80us, system will keep all the register status and system halt but oscillation active. When Vdd drop below V_{RESET} and more than 80us, system will occur RESET, and the following actions refer the section 6.5.1 RESET description.

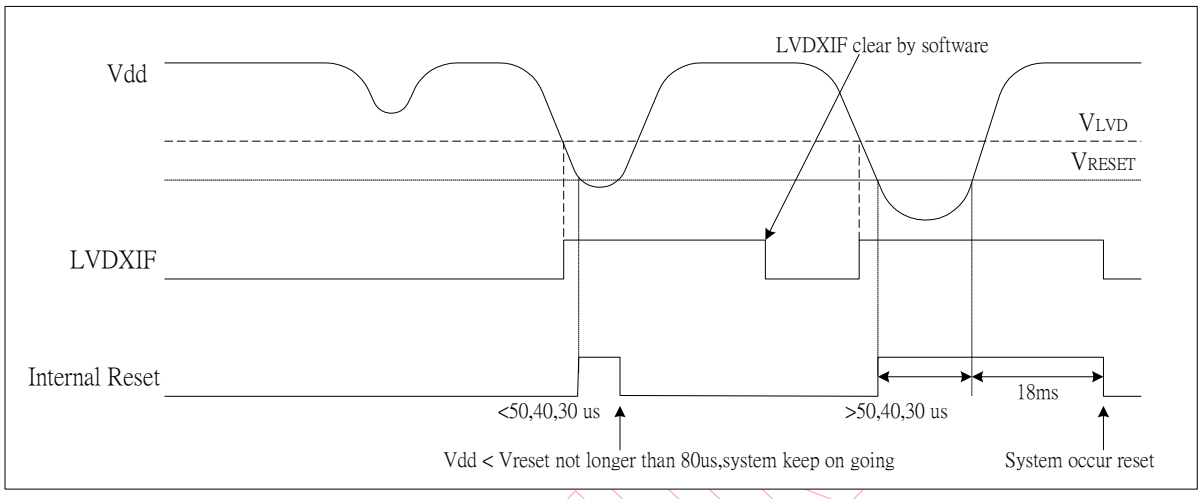


Fig. 34 LVD waveform situation

6.12 Oscillator

6.12.1 Oscillator Modes

The EM78F568N can be operated in the four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High XTAL oscillator mode (HXT), and Low XTAL oscillator mode(LXT). User can select one of them by programming OSC2, OCS1 and OSC0 in the CODE Option register. Table10 depicts how these four modes are defined.

The up-limited operation frequency of crystal/resonator on the different VDD is listed in Table 11

Table 10 Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (XTAL oscillator mode)	0	0	0
HXT (High XTAL oscillator mode)	0	0	1
LXT1 (Low XTAL1 oscillator mode)	0	1	0
LXT2 (Low XTAL2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

In LXT1, LXT2, XT, HXT and ERC mode OSCI and OSCO are used, can't used as normal I/O pin.

In IRC mode, P55 is normal I/O pin

<Note>: 1. Frequency range of HXT mode is 20MHz ~ 6MHz.

2. Frequency range of XT mode is 6MHz ~ 1MHz.

3. Frequency range of LXT1 mode is 1MHz ~ 100kHz.

4. Frequency range of XT mode is 32kHz.

Table 11 The Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max.(MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	5.0	20.0

6.12.2 Crystal Oscillator/Ceramic Resonators (XTAL)

EM78F568N can be driven by an external clock signal through the OSCI pin as shown in Fig. 35 below.

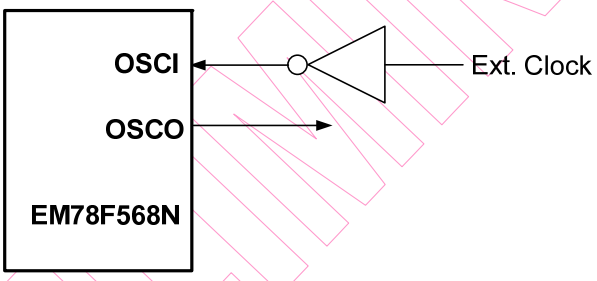


Fig. 35 Circuit for External Clock Input

In the most applications, pin OSCI and pin OSCO can connected with a crystal or ceramic resonator to generate oscillation. Fig. 36 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 12 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

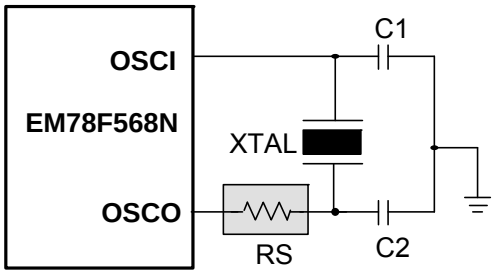


Fig. 36 Circuit for Crystal/Resonator

Table 12 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

6.12.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig. 37) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 M ohm. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

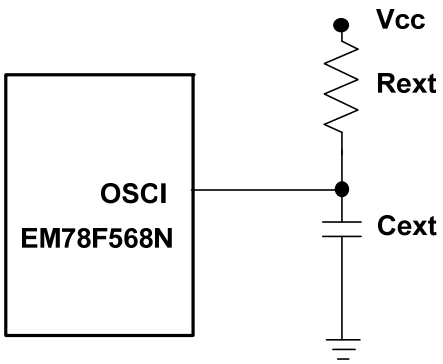


Fig. 37 Circuit for External RC Oscillator Mode

Table 13 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140 KHz	140 KHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850 KHz	820 KHz
	10k	450 KHz	450 KHz
	100k	48 KHz	50 KHz
300 pF	3.3k	560 KHz	540 KHz
	5.1k	370 KHz	360 KHz
	10k	196 KHz	192 KHz
	100k	20 KHz	20 KHz

<Note> 1. Measured on DIP packages.
2. For design reference only.

6.12.4 Internal RC Oscillator Mode

EM78F568N offer a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (16MHz, 8MHz and 455KHz) that can be set by CODE OPTION: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the CODE OPTION bits: C4~C0. Table 14 describes a typical instance of the calibration.

Table 15 Internal RC Drift Rate (Ta=25°C , VDD=5 V± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.2V~5.5V)	Process	Total
455kHz	±5%	±5%	±4%	±14%
4MHz	±5%	±5%	±4%	±14%
8MHz	±5%	±5%	±4%	±14%
16MHz	±5%	±5%	±4%	±14%

Table 16 Calibration Selections for Internal RC Mode

Trimming code					CLK Period	Frequency
C4	C3	C2	C1	C0		
1	1	1	1	1	Period*(1+32%)	F*(1-24.2%)
1	1	1	1	0	Period*(1+30%)	F*(1-23.1%)
1	1	1	0	1	Period*(1+28%)	F*(1-21.9%)
1	1	1	0	0	Period*(1+26%)	F*(1-20.6%)
1	1	0	1	1	Period*(1+24%)	F*(1-19.4%)
1	1	0	1	0	Period*(1+22%)	F*(1-18%)
1	1	0	0	1	Period*(1+20%)	F*(1-16.7%)
1	1	0	0	0	Period*(1+18%)	F*(1-15.3%)
1	0	1	1	1	Period*(1+16%)	F*(1-13.8%)
1	0	1	1	0	Period*(1+14%)	F*(1-12.3%)
1	0	1	0	1	Period*(1+12%)	F*(1-10.7%)
1	0	1	0	0	Period*(1+10%)	F*(1-9.1%)
1	0	0	1	1	Period*(1+8%)	F*(1-7.4%)
1	0	0	1	0	Period*(1+6%)	F*(1-5.7%)
1	0	0	0	1	Period*(1+4%)	F*(1-3.8%)
1	0	0	0	0	Period*(1+2%)	F*(1-2%)
0	0	0	0	0	Period (default)	F (default)
0	0	0	0	1	Period*(1-2%)	F*(1+2%)
0	0	0	1	0	Period*(1-4%)	F*(1+4.2%)
0	0	0	1	1	Period*(1-6%)	F*(1+6.4%)
0	0	1	0	0	Period*(1-8%)	F*(1+8.7%)
0	0	1	0	1	Period*(1-10%)	F*(1+11.1%)
0	0	1	1	0	Period*(1-12%)	F*(1+13.6%)
0	0	1	1	1	Period*(1-14%)	F*(1+16.3%)
0	1	0	0	0	Period*(1-16%)	F*(1+19%)
0	1	0	0	1	Period*(1-18%)	F*(1+22%)
0	1	0	1	0	Period*(1-20%)	F*(1+25%)
0	1	0	1	1	Period*(1-22%)	F*(1+28.2%)
0	1	1	0	0	Period*(1-24%)	F*(1+31.6%)
0	1	1	0	1	Period*(1-26%)	F*(1+35.1%)
0	1	1	1	0	Period*(1-28%)	F*(1+38.9%)
0	1	1	1	1	Period*(1-30%)	F*(1+42.9%)

* 1.Theoretical values, for reference only. It depend on process.

2. Similar way of calculation is also applicable for low frequency mode.

6.13 Power On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays at its steady state. EM78F568N is equipped with Power On Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd is rising quick enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.14 External Power On Reset Circuit

The circuit shown in Fig.38 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

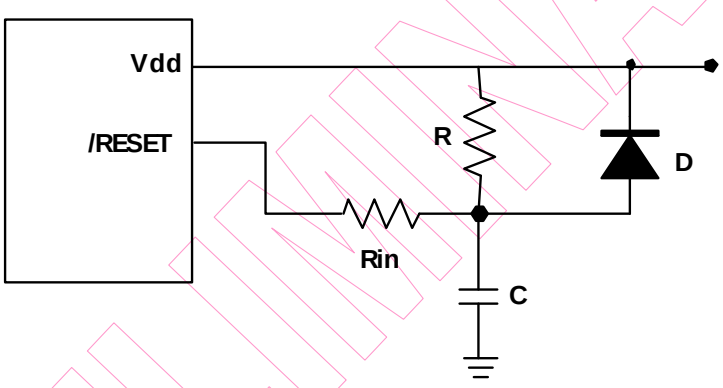


Fig. 38 External Power-Up Reset Circuit

6.15 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig.39 and Fig. 40 show how to build a residue-voltage protection circuit.

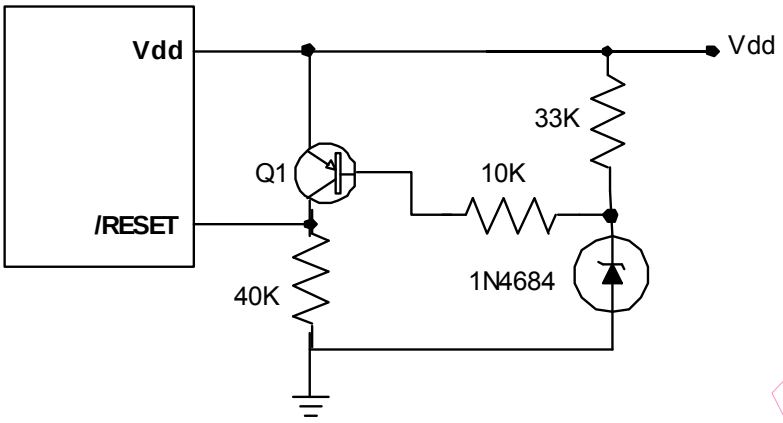


Fig. 39 Circuit 1 for the Residue Voltage Protection

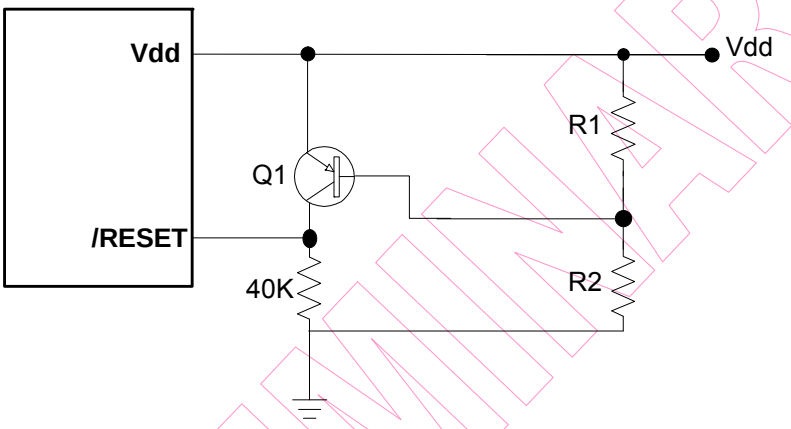


Fig. 40 Circuit 2 for the Residue Voltage Protection

6.16 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two

instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/ 2 as indicated in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
000 0000 0000 0000	0000	NOP	No Operation	None
000 0000 0000 0001	0001	DAA	Decimal Adjust A	C
000 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
000 0000 0000 0100	0004	WDTC	0 → WDT	T,P
000 0000 0001 0000	0010	ENI	Enable Interrupt	None
000 0000 0001 0001	0011	DISI	Disable Interrupt	None
000 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
000 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
000 0001 rrrr rrrr	01rr	MOV R,A	A → R	None
000 0010 0000 0000	0200	CLRA	0 → A	Z
000 0011 rrrr rrrr	03rr	CLR R	0 → R	Z
000 0100 rrrr rrrr	04rr	SUB A,R	R-A → A	Z,C,DC
000 0101 rrrr rrrr	05rr	SUB R,A	R-A → R	Z,C,DC
000 0110 rrrr rrrr	06rr	DECA R	R-1 → A	Z
000 0111 rrrr rrrr	07rr	DEC R	R-1 → R	Z
000 1000 rrrr rrrr	08rr	OR A,R	A ∨ R → A	Z
000 1001 rrrr rrrr	09rr	OR R,A	A ∨ R → R	Z
000 1010 rrrr rrrr	0Arr	AND A,R	A & R → A	Z
000 1011 rrrr rrrr	0Brr	AND R,A	A & R → R	Z
000 1100 rrrr rrrr	0Crr	XOR A,R	A ⊕ R → A	Z
000 1101 rrrr rrrr	0Drr	XOR R,A	A ⊕ R → R	Z
000 1110 rrrr rrrr	0Err	ADD A,R	A + R → A	Z,C,DC
000 1111 rrrr rrrr	0Frr	ADD R,A	A + R → R	Z,C,DC
001 0000 rrrr rrrr	10rr	MOV A,R	R → A	Z
001 0001 rrrr rrrr	11rr	MOV R,R	R → R	Z
001 0010 rrrr rrrr	12rr	COMA R	/R → A	Z
001 0011 rrrr rrrr	13rr	COM R	/R → R	Z
001 0100 rrrr rrrr	14rr	INCA R	R+1 → A	Z

001 0101 rrrr rrrr	15rr	INC R	R+1 → R	Z
001 0110 rrrr rrrr	16rr	DJZA R	R-1 → A, skip if zero	None
001 0111 rrrr rrrr	17rr	DJZ R	R-1 → R, skip if zero	None
001 1000 rrrr rrrr	18rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
001 1001 rrrr rrrr	19rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
001 1010 rrrr rrrr	1Arr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
001 1011 rrrr rrrr	1Brr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
001 1100 rrrr rrrr	1Crr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
001 1101 rrrr rrrr	1Drr	SWAP R	R(0-3) ↔ R(4-7)	None
001 1110 rrrr rrrr	1Err	JZA R	R+1 → A, skip if zero	None
001 1111 rrrr rrrr	1Frr	JZ R	R+1 → R, skip if zero	None
010 0bbb rrrr rrrr	2xrr	BC R,b	0 → R(b)	None <Note2>
010 1bbb rrrr rrrr	2xrr	BS R,b	1 → R(b)	None <Note3>
011 0bbb rrrr rrrr	3xrr	JBC R,b	if R(b)=0, skip	None
011 1bbb rrrr rrrr	3xrr	JBS R,b	if R(b)=1, skip	None
100 kkkk kkkk kkkk	4kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
101 kkkk kkkk kkkk	5kkk	JMP k	(Page, k) → PC	None
110 0000 kkkk kkkk	60kk	MOV A,k	k → A	None
110 0100 kkkk kkkk	64kk	OR A,k	A ∨ k → A	Z
110 1000 kkkk kkkk	68kk	AND A,k	A & k → A	Z
110 1100 kkkk kkkk	6Ckk	XOR A,k	A ⊕ k → A	Z
111 0000 kkkk kkkk	70kk	RETL k	k → A, [Top of Stack] → PC	None
111 0100 kkkk kkkk	74kk	SUB A,k	k-A → A	Z,C,DC
111 1100 kkkk kkkk	7Ckk	ADD A,k	k+A → A	Z,C,DC
111 1010 0000 kkkk	7A0k	SBANK k	K->R1(4)	None
111 1010 0100 kkkk	7A4k	GBANK k	K->R1(0)	None
111 1010 1000 kkkk kkk kkkk kkkk kkkk	7A8k kkkk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
111 1010 1100 kkkk kkk kkkk kkkk kkkk	7ACk kkkk	LJMP k	Next instruction : k kkkk kkkk kkkk K→PC	None
111 1011 rrrr rrrr	7Brr	TBRD R	ROM[(TABPTR)] → R	None

6.17 Code option

Code Option from SRAM/ROM/OTP/FLASH

Word 0														
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
COBS0	-	-	CLKS0	-	-	LVR1	LVR0	RESETEN	ENWDT	NRHL	NREB	PR2	PR1	PR0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 14 (COBS0): IRC mode selection bit

1: IRC frequency selection from register

0: IRC frequency selection from code option

Bits 13~12: unused bit, set to 0 all times.

Bits 11(CLKS0)：instruction period option bits

Instruction Period	CLKS0
4 clocks	0
2 clocks	1

Bits 8~7(LVR1~LVR0)：Low voltage reset enable bit.

LVR1, LVR0	VDD reset level
00	NA
01	2.7V
10	3.7V
11	4.2V

Bit 6 (RESETEN): P83//RST pin selection bit

1: /RST pin

0: P83 pin

Bit 5(ENWDT)：WDT enable bit 0/1: disable/enable

Bit 4(NRHL)：noise rejection high/low pulse define bit.

0: pulses equal to 32/fc [s] is regarded as signal

1: pulses equal to 8/fc [s] is regarded as signal

Bit 3(NREB)：noise rejection enable bit

0: enable

1: disable

Bits 2~0(PR2~PR0): product bits

Word 1														
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HLFS	-	SHE	C4	C3	C2	C1	C0	RCM1	RCM0	-	OSC2	OSC1	OSC0	RCOD
0	**1**	0	0	0	0	0	0	0	0	**1**	0	0	0	0

Bit 14(HLFS)：Initialize CPU mode. (1:green mode,0:normal mode)

Bit 13: unused bit, set to 1 all the time.

Bit 12(SHE)：System halt enable bit. 0:disable 1: enable

Bits 11~7(C4~C0)：IRC trim bits. This parts will auto set by writer.

Bits 6~5(RCM1~RCM0)：IRC frequency selection.

Bit 4: unused bit, set to 1 all the time.

Bits 3~1(OSC2~OSC0)：Oscillator mode selection bits.

Mode	OSC2	OSC1	OSC0
XT (XTAL oscillator mode)	0	0	0
HXT (High XTAL oscillator mode)	0	0	1
LXT1 (Low XTAL1 oscillator mode)	0	1	0
LXT2 (Low XTAL2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

Bit 0(RCOD): A selecting bit of Oscillator output or I/O port.

RCOUT	Pin Function
1	OSCO pin is open drain
0	OSCO output system clock (default)

Word 2														
Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SC3	SC2	SC1	SC0	-	-	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 14~11(SC3~SC0)：WDT clock trim bits. This parts will auto set by writer.

Bits 10~9: unused bit, set to 1 all the time.

Bits 8~0(ID8~ID0)：Customer's ID code.

7 DC Electrical Characteristic

(Ta=25 °C, VDD=5.0V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC	10(-)	14(8)	MHz
	XTAL: VDD to 5V		DC	20(-)	24(20)	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	KHz
	IRC: VDD to 5 V	4MHz, 1MHz, 455KHz, 8MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	2.9	4	5.7	MHz
IRCE	Internal RC oscillator error per stage		±4.3	±4.5	±4.7	%
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	5.8	8	11.4	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	0.725	1	1.425	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	330	455	645	KHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high , VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low , VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	0.7Vdd		Vdd+0.3 V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	-0.3V		0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd		Vdd+0.3 V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V		0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.7Vdd		Vdd+0.3 V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V		0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6,7,8,9)	VOH = VDD-0.5V (IOH =3.7mA)	-4.1	-4.45	-5	mA
IOL1	Output Low Voltage (Ports 5, 6,7,8,9)	VOL = GND+0.5V (IOL =10mA)	11	12	13.5	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-70	-75	-80	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	35	40	45	μA

ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	0.6	2.0	2.5	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	6	7	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	20	22	24	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	25	27	29	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	1.5	1.6	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	2.1	2.2	2.3	mA

* These parameters are characterizes but not tested.
* Data in the Minimum, Typical, Maximum(“Min”,“Typ”,”Max”) column are based on characterization results at 25℃. This data is for design guidance only and is not tested.

(Ta= 85 °C, VDD= 5.0V, VSS= 0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC	10	14	MHz
	XTAL: VDD to 5V		DC	20	24	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	780	F±30%	KHz
	IRC: VDD to 5 V	4MHz, 1MHz, 455KHz, 8MHz	F±30%	F	F±30%	Hz
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	2.83	3.9	5.55	MHz
IRCE	Internal RC oscillator error per stage		±4.3	±4.5	±4.7	%
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	5.52	7.6	10.82	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	0.69	0.95	1.35	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	314	432.2	613	KHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.8	3.9	4.0	V
IERC1	Sink current	VI from low to high , VI=5V	20	21	22	
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.6	1.7	1.7	V
IERC2	Sink current	VI from high to low , VI=2V	15	16	17	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	0.7Vdd		Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	-0.3V		0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd		Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V		0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.7Vdd		Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V		0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.8	2.9	3.0	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.6	1.7	1.8	V
IOH1	Output High Voltage (Ports 5, 6)	VOH = VDD-0.5V (IOH =3.4mA)	-3.7	-4.0	-4.7	mA
IOL1	Output Low Voltage (Ports 5, 6)	VOL = GND+0.5V (IOL =8mA)	9	10	11.5	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-60	-65	-70	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	25	30	35	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating,	0.6	2.0	2.5	μA

		WDT disabled				
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	6	7	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	18	20	22	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	23	25	27	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	1.4	1.5	1.6	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	2.0	2.1	2.2	mA

(Ta= -40 °C, VDD= 5.0V, VSS= 0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycle with two clocks	DC	10	14	MHz
	XTAL: VDD to 5V		DC	20	24	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	880	F±30%	KHz
	IRC: VDD to 5 V	4MHz, 1MHz, 455KHz,8MHz	F±30%	F	F±30%	Hz
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	2.977	4.1	5.83	MHz
IRCE	Internal RC oscillator error per stage		±4.3	±4.5	±4.7	%
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	6.1	8.4	11.96	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	0.76	1.05	1.49	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	346	477	677	KHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	4.0	4.1	4.2	V
IERC1	Sink current	VI from low to high , VI=5V	22	23	24	
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.8	1.9	2.0	V
IERC2	Sink current	VI from high to low , VI=2V	17	18	19	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	0.7Vdd		Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	-0.3V		0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd		Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V		0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.7Vdd		Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V		0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	3.0	3.1	3.2	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.8	1.9	2.0	V
IOH1	Output High Voltage (Ports 5, 6)	VOH = VDD-0.5V (IOH =4.0mA)	-4.4	-4.8	-5.5	mA
IOL1	Output Low Voltage (Ports 5, 6)	VOL = GND+0.5V (IOL =11.5mA)	13	14	16	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-80	-85	-90	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	45	50	55	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	0.6	2.0	2.5	μA
ISB2	Power down current	All input and I/O pins at	6	7	8	μA

		VDD, output pin floating, WDT enabled				
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	22	24	26	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	27	29	31	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	1.6	1.7	1.8	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	2.2	2.3	2.4	mA

8 AC Electrical Characteristic

(EM78F568N, 0≦Ta≦70°C, VDD=5V, VSS=0V)

(, -40≦Ta≦85°C, VDD=5V, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time		11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	1000			ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* These parameters are characterizes but not tested.

* Data in the Minimum, Typical, Maximum(“Min”,“Typ”,”Max”) column are based on characterization results at 25℃. This data is for design guidance only and is not tested.

N= selected prescaler ratio.

These parameters are characterizes but not tested.

Note: The priority of share pins(for pin above three function share)

1. The Priority of P56/TC2 Pin

TC2/P56 Pin Priority	
High	Low
TC2	P56

2. The Priority of P53/SCL/SCK Pin

P53/SCK/SCL Pin Priority		
High	Second	Low
SCL	SCK	P53

3. The Priority of P57/TC3/PDO Pin

P57/TC3/PDO Pin Priority		
High	Second	Low
TC3	PDO	P57

4. The Priority of P52/RX/SI Pin

P52/RX/SI Pin Priority		
High	Second	Low
RX	SI	P52

5. The Priority of P51/SDA/TX/SO Pin

P51/SDA/TX/SO Pin Priority			
High	**Second**	**Third**	**Low**
SDA	TX	SO	P51

6. The Priority of P77/TCC Pin

P77/TCC Pin Priority	
High	**Low**
TCC	P77

7. The Priority of P76/PWMB Pin

P76/PWMB Pin Priority	
High	**Low**
PWMB	P76

8. The Priority of P75/PWMA Pin

P75/PWMA Pin Priority	
High	**Low**
PWMA	P75

9. The Priority of P50/VREF//SS Pin

P50/VREF//SS Pin Priority		
High	**Second**	**Low**
VREF	/SS	P50