EM78F564N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre
95 How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
3F, SSMEC Bldg., Gaoxin S. Ave. I
Shenzhen Hi-tech Industrial Park
(South Area), Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
Elan Microelectronics Shanghai, Ltd.
#34, First Fl., 2nd Bldg.,
Lane 122, Chunxiao Rd.
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600
elan-sh@elanic.com.cn

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Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2009/09/11
1.0	Initial released version	2009/11/27

1 General Description

The EM78F564N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 4K×13-bit Electrical Flash Memory. It provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM features, the EM78F564N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 4K×13 bits on-chip Flash memory
  - 144×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - 3 programmable Level Voltage Reset LVR : 4.1V, 3.7V, 2.7V
  - Less than 1.5 mA at 5V / 4 MHz
  - Typically 20 μA, at 3V / 32kHz
  - Typically 1.5 μA, during sleep mode
- I/O port configuration
  - 4 bidirectional I/O ports: P5, P6, P7 and P8
  - 25 I/O pins
  - Wake-up port : P6
  - High sink port : P6
  - 14 programmable pull-high I/O pins
  - 14 programmable pull-down I/O pins
  - 8 programmable open-drain I/O pins
  - External interrupt with Wake-up : P60
- Operating voltage range
  - 2.5V~5.5V at -40°C~85°C (Industrial)
  - 2.3V~5.5V at 0°C~70°C (Commercial)
- Operating frequency range (base on two clocks)
  - Crystal mode : DC~16MHz @ 4.5V~5.5V ; DC~8MHz @ 3V~5.5V ; DC~4MHz @ 2.3V~5.5V
  - ERC mode : DC~16MHz @ 4.5V~5.5V ; DC~8MHz @ 3V~5.5V ; DC~4MHz @ 2.3V~5.5V
  - IRC mode : DC~16MHz @ 4.5V~5.5V ; DC~4MHz @ 2.3V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.5V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
455kHz	± 3%	± 5%	± 2.5%	± 10.5%

- Fourteen available interrupts
  - Internal interrupt : 11
  - External interrupt : 3
- 8 channels Analog-to-Digital Converter with 10-bit resolution
- One set of comparator (offset voltage: smaller than 10 mV)
- Two channels Pulse Width Modulation (PWM) with 10-bit resolution
- Two 8-bit Timer/Counter
  - TC1 : Timer/Counter/Capture
  - TC3 : Timer/Counter/PDO (Programmable Divider Output)/PWM (pulse width modulation)
- One 16-bit Timer/Counter
  - TC2 : Timer/Counter/Window
- Serial transmitter/receiver interface
  - Serial Peripheral Interface (SPI): Three-wire synchronous communication
  - Universal Asynchronous Receiver/Transmitter (UART)
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - External interrupt input pin
  - 2/4/8/16 clocks per instruction cycle selected by code option
  - Power down (Sleep) mode
  - High EFT immunity
- Single instruction cycle commands
- Special Features
  - Programmable free running Watchdog Timer
  - Power-on voltage detector available (2.0V ~ 2.2V)
- Package Type:
  - 24-pin skinny DIP 300 mil : EM78F564NK24J/S
  - 24-pin SOP 300 mil : EM78F564NSO24J/S
  - 28-pin skinny DIP 300 mil : EM78F564NK28J/S
  - 28-pin SOP 300 mil : EM78F564NSO28J/S
  - 32-pin QFN 5×5 mm : EM78F564NQN32J/S

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Assignment

(1) 24-Pin SKDIP/SOP

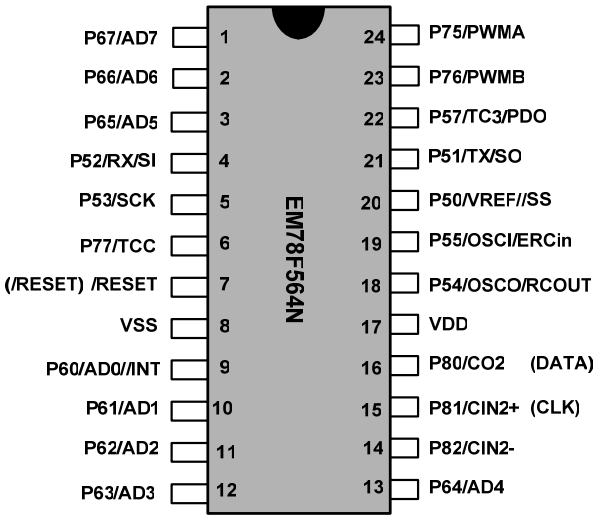


Figure 3-1 24-pin EM78F564N

(2) 28-Pin SKDIP/SOP

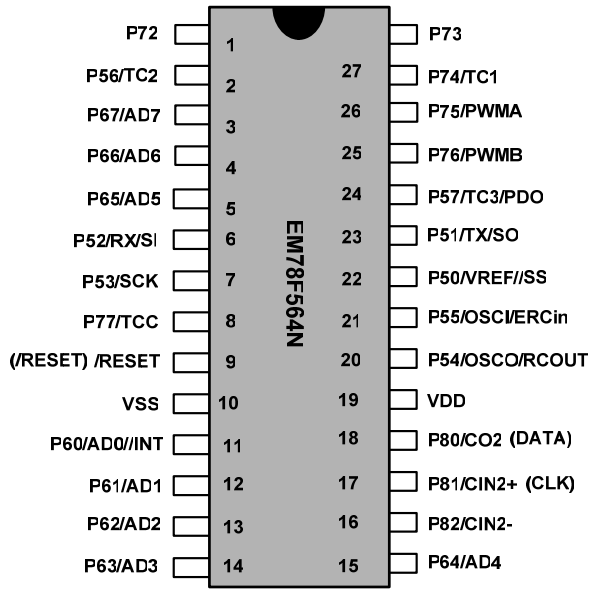


Figure 3-2 28-pin EM78F564N

(3) 32-Pin QFN

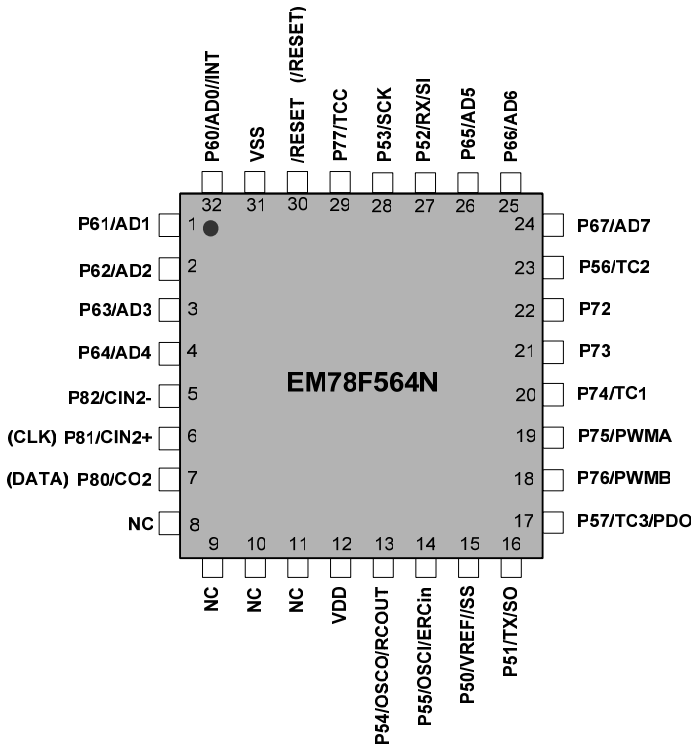


Figure 3-3 32-pin EM78F564N

4 Pin Description

Table 4-1 EM78F564N-24 Pins

Symbol	Pin No.	Type	Function
P50~P55, P57	20, 21, 4, 5, 18, 19, 22	I/O	Bidirectional 7-bit input/output pins. P50~P53 can be used as pull-down by software programming. P50 can be used as external reference voltage for ADC or SPI slave select P51 can be used as SPI serial data output or UART TX output P52 can be used as SPI serial data input or UART RX input P53 can be used as SPI serial clock input/output P57 can be used as 8-bit timer/counter or programmable divider output (PDO).
P60 ~P67	9~13, 3~1	I/O	Bidirectional 8-bit input/output ports. These can be used as pull-high or as open drain by software programming. P60~63 can be used as pull-down by software programming. These can be used as 8-channel 10-bit resolution A/D converter. P60 can be used as external interrupt.
P75, P76, P77	24, 23, 6	I/O	P75 ~ P77 are bidirectional I/O ports. P75~P76 can be used as pull-high or pull-down by software programming. P75, P76 can be used as PWMA/B output.
P80~P82	16~14	I/O	P80 ~ P82 are bidirectional I/O ports. P80 can act as CO2. P81 can act as CIN2+. P82 can act as CIN2-. * P80 is DATA pin for Writer programming (Required). * P81 is CLK pin for Writer programming (Required). * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
OSCI/ERCin	19	I/O	External clock crystal resonator oscillator input pin. External RC oscillator clock input pin.
OSCO/ RCOUT	18	I/O	Clock output from crystal oscillator. Clock output from internal RC oscillator.
TCC	6	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	7	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * /RESET is /RESET pin for Writer programming (Required). * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
VDD	17	-	Power supply pin
VSS	8	-	Ground

Table 4-2 EM78F564N-28 Pins

Symbol	Pin No.	Type	Function
P50~P57	22, 23, 6, 7, 20, 21, 2, 24	I/O	Bidirectional 8-bit input/output pins. P50~P53 can be used as pull-down by software programming. P50 can be used as external reference voltage for ADC or SPI slave select P51 can be used as SPI serial data output or UART TX output P52 can be used as SPI serial data input or UART RX input P53 can be used as SPI serial clock input/output P56 can be used as 16-bit timer/counter(TC2). P57 can be used as 8-bit timer/counter or programmable divider output (PDO).
P60~ P67	11~15, 5~3	I/O	Bidirectional 8-bit input/output ports. These can be used as pull-high or as open drain by software programming. P60~63 can be used as pull-down by software programming. These can be used as 8-channel 10-bit resolution A/D converter. P60 can be used as external interrupt.
P72~P77	1, 28~25, 8	I/O	P72 ~P77 are bidirectional I/O ports. P72~P76 can be used as pull-high or pull-down by software programming. P74 can be used as 8-bit timer/counter (TC1). P75, P76 can be used as PWMA/B output.
P80~P82	18~16	I/O	P80 ~ P82 are bidirectional I/O ports. P80 can act as CO2. P81 can act as CIN2+. P82 can act as CIN2-. * P80 is DATA pin for Writer programming (Required). * P81 is CLK pin for Writer programming (Required). * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
OSCI / ERCin	21	I/O	External clock crystal resonator oscillator input pin. External RC oscillator clock input pin.
OSCO / RCOUT	20	I/O	Clock output from crystal oscillator. Clock output from internal RC oscillator.
TCC	8	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	9	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * /RESET is /RESET pin for Writer programming (Required). * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
VDD	19	-	Power supply pin
VSS	10	-	Ground

Table 4-3 EM78F564N-32 Pins

Symbol	Pin No.	Type	Function
P50~P57	15, 16, 27, 28, 13, 14, 23, 17	I/O	Bidirectional 8-bit input/output pins. P50~P53 can be used as pull-down by software programming. P50 can be used as external reference voltage for ADC or SPI slave select. P51 can be used as SPI serial data output or UART TX output. P52 can be used as SPI serial data input or UART RX input. P53 can be used as SPI serial clock input/output P56 can be used as 16-bit timer/counter(TC2). P57 can be used as 8-bit timer/counter or programmable divider output (PDO).
P60~ P67	32, 1~4, 26~24	I/O	Bidirectional 8-bit input/output ports. These can be used as pull-high or can be used as open drain by software programming. P60~63 can be used as pull-down by software programming. These can be used as 8-channel 10-bit resolution A/D converter. P60 can be used as external interrupt.
P72~P77	22~18, 29	I/O	P72 ~P77 are bidirectional I/O ports. P72~P76 can be used as pull-high or pull-down by software programming. P74 can be used as 8-bit timer/counter (TC1). P75, P76 can be used as PWMA/B output.
P80~P82	7~5	I/O	P80 ~ P82 are bidirectional I/O ports. P80 can act as CO2. P81 can act as CIN2+. P82 can act as CIN2-. * P80 is DATA pin for Writer programming (Required). * P81 is CLK pin for Writer programming (Required). * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
OSCI / ERCin	14	I/O	External clock crystal resonator oscillator input pin. External RC oscillator clock input pin.
OSCO / RCOUT	13	I/O	Clock output from crystal oscillator. Clock output from internal RC oscillator.
TCC	29	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	30	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset. * /RESET is /RESET pin for Writer programming. (Required) * For ISP (In System Programming) design rules, refer to "*EM78F6xxN/5xxN MCU Programming*" Application Notes.
NC	8~11	-	No Connection
VDD	12	-	Power supply pin
VSS	31	-	Ground

5 Block Diagram

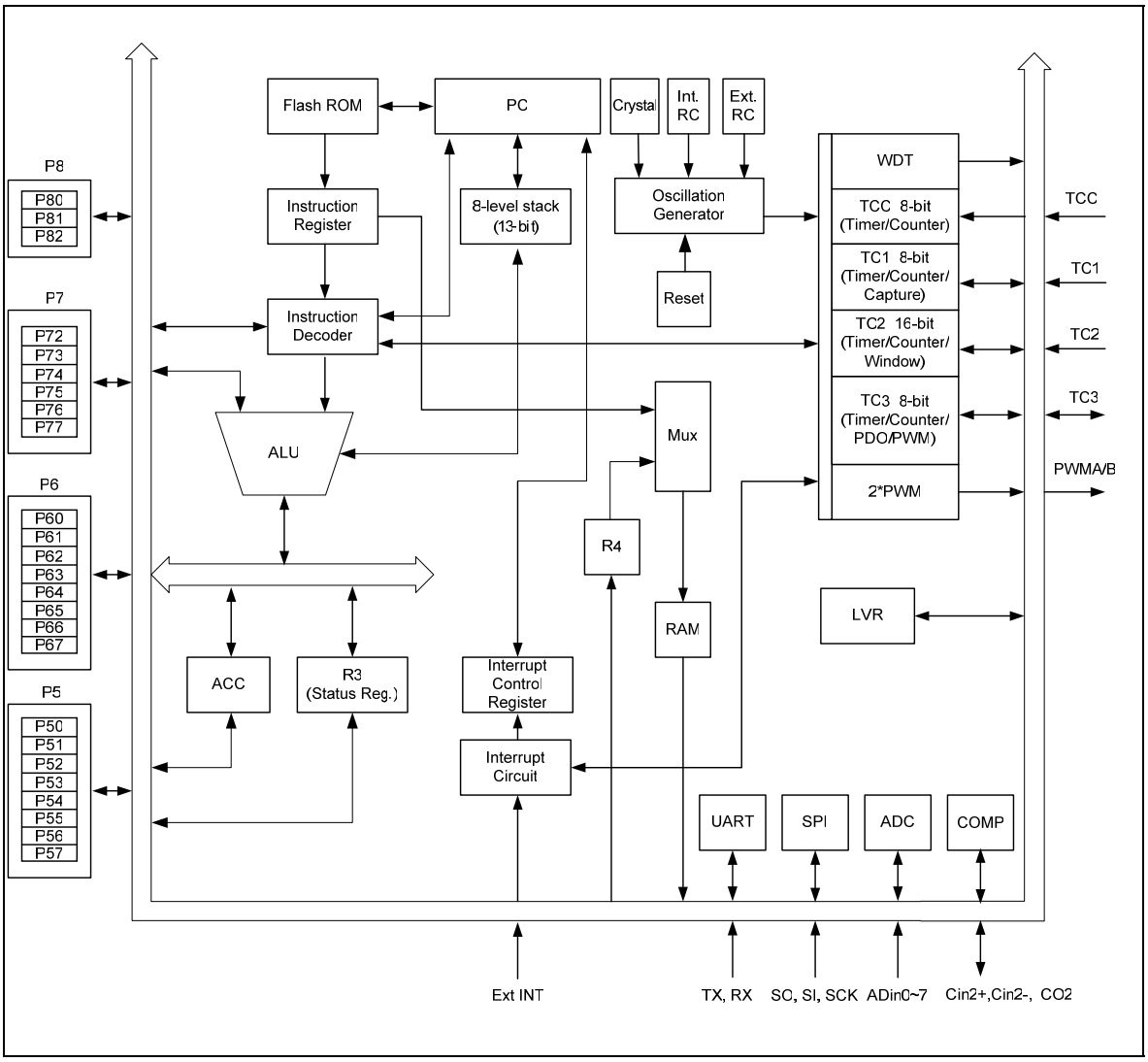


Figure 5-1 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

Depending on the device type, R2 and hardware stack are 12-bit wide. The structure is depicted in Figure 6-1.

The configuration structure generates 4K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "0"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

"CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

"LJMP" instruction allows direct loading of the program counter bits (A0~A11). Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).

"LCALL" instruction loads the program counter bits (A0 ~A11), and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12})

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows loading an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except “ADD R2, A” that is written to R2 (e.g. "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8 or fclk/16) except for instructions that would change the contents of R2 and “LCALL”, “LJMP”, “TBRD” instruction. The “LCALL”, “LJMP” and “TBRD” instructions need two instructions cycle.

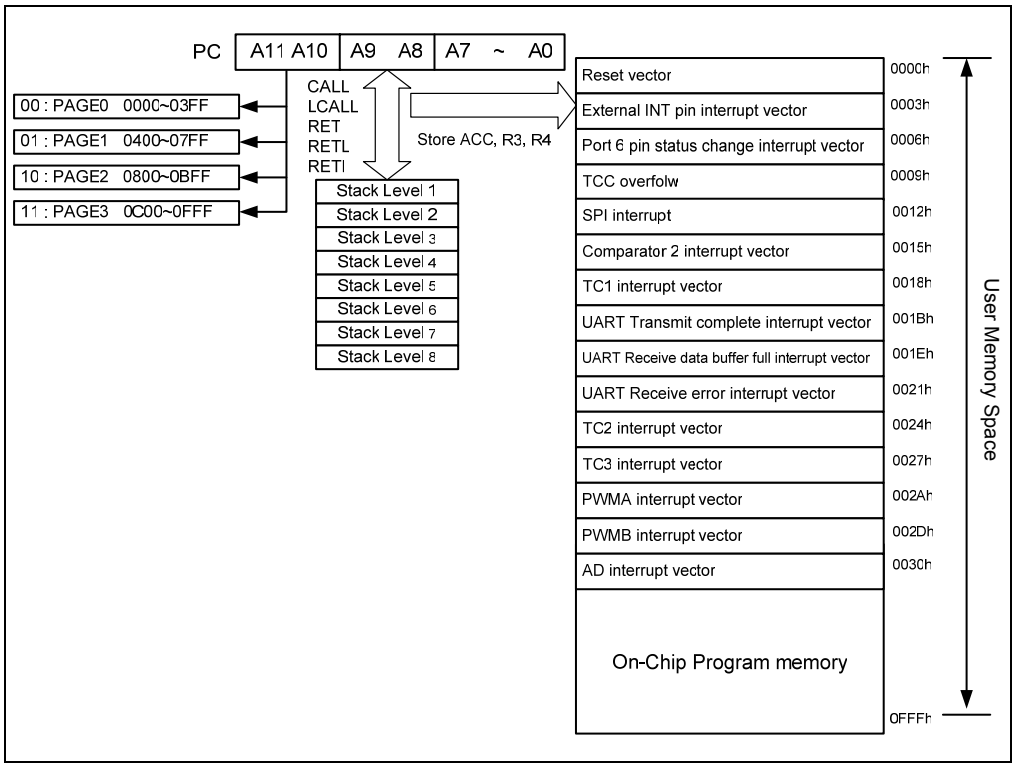


Figure 6-1 Program Counter Organization

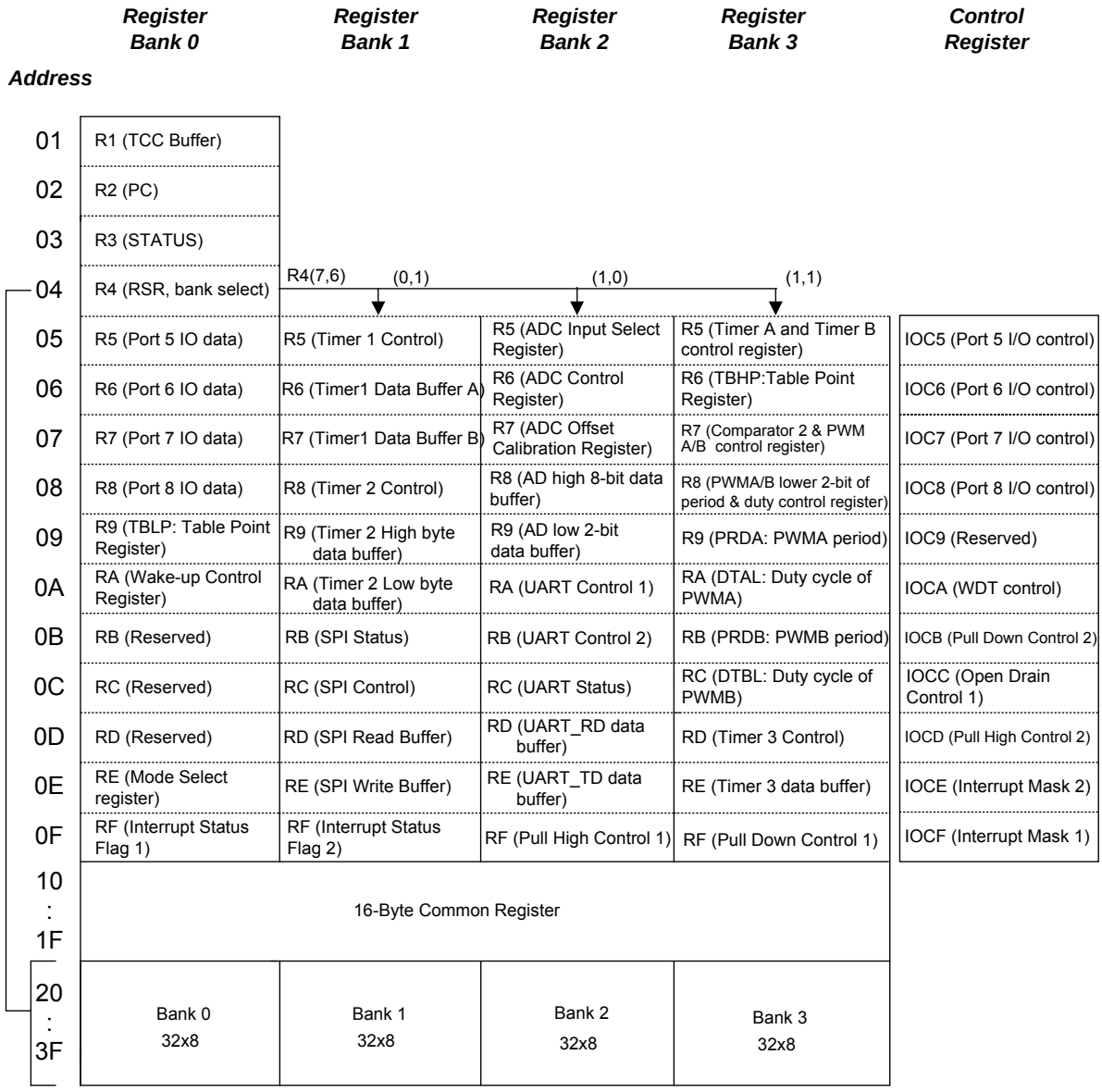


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7 ~ 5: Not used, set to “0” at all time.

Bit 4 (T): Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R8 are I/O registers.

6.1.7 Bank 0 R9 (TBLP : Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: This is the least 8 significant bits of address for program code.

NOTE

- *Bank 0 R9 overflow will carry to Bank 3 R6.*
- *Bank 0 R9 underflow will borrow from Bank 3 R6.*

6.1.8 Bank 0 RA (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WE	ICWE	ADWE	EXWE	SPIWE	-	-	-

Bit 7 (CMP2WE): Comparator 2 wake-up enable bit.

0 : Disable Comparator 2 wake-up

1 : Enable Comparator 2 wake-up

When the Comparator 2 output status changed is used to enter an interrupt vector or to wake-up the EM78F564N from sleep, the CMP2WE bit must be set to “Enable“.

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0 : Disable Port 6 input status change wake-up

1 : Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When ADC Complete is used to enter an interrupt vector or to wake-up the EM78F564N from sleep with A/D conversion running, the ADWE bit must be set to “Enable“.

Bit 4 (EXWE): External /INT wake-up enable bit

0 : Disable External /INT pin wake-up

1 : Enable External /INT pin wake-up

Bit 3 (SPIWE): SPI wake-up enable bit, When SPI act as slave device

0 : Disable SPI wake-up, when SPI acts as slave device

1 : Enable SPI wake-up, when SPI acts as slave device

Bits 2 ~ 0: Not used, set to “0” at all time.

6.1.9 Bank 0 RB ~ RD

These are reserved registers.

6.1.10 Bank 0 RE (Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	-	-	-	-

Bit 7: Not used, set to "0" at all time

Bit 6 (TIMERSC): TCC, TC1, TC2, TC3, Timer A, Timer B clock source select.

0 : Fs is used as Fc

1 : Fm is used as Fc

Bit 5 (CPUS): CPU Oscillator Source Select.

0 : Fs : Sub frequency for WDT internal RC time base

1 : Fm : Main-oscillator clock

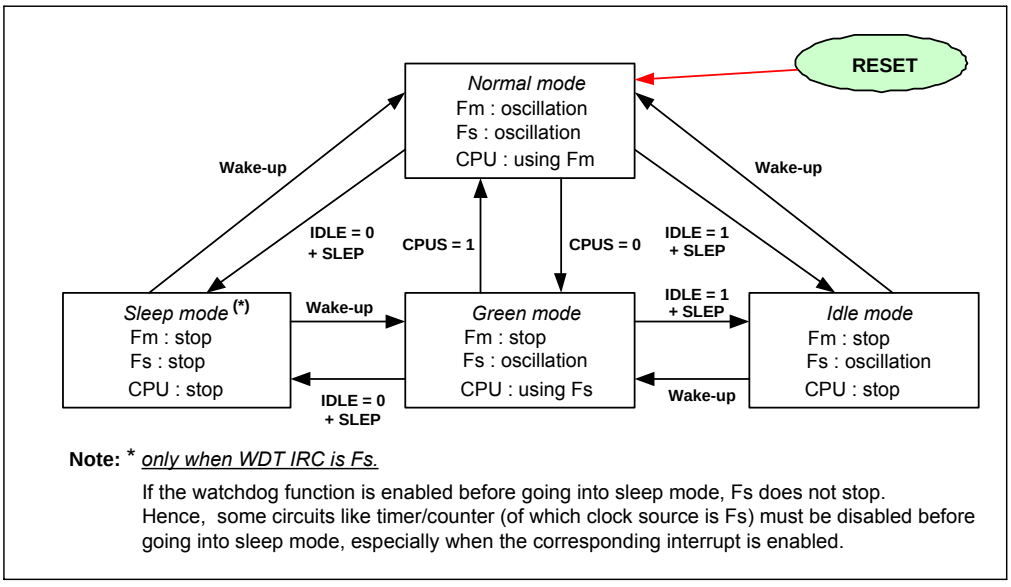
When CPUS=0, the CPU oscillator selects the Sub-oscillator and the Main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

0 : IDLE="0" + SLEP instruction → Sleep mode

1 : IDLE="1" + SLEP instruction → Idle mode

CPU Operation Mode



Note: * *only when WDT IRC is Fs.*

If the watchdog function is enabled before going into sleep mode, Fs does not stop. Hence, some circuits like timer/counter (of which clock source is Fs) must be disabled before going into sleep mode, especially when the corresponding interrupt is enabled.

Figure 6-3 EM78F564N CPU Operation Mode

Oscillator (Normal Mode Source)	CPU Mode Status	Oscillator Stable Time (S)[1]	Count from Normal/Green (CLK)[2]
Crystal ; 1M ~ 16MHz	Sleep/Idle → Normal	0.5 ms ~ 2 ms	254 CLK
	Green → Normal		254 CLK
	Sleep/Idle → Green	< 100 µs	32 CLK
ERC ; 3.5MHz	Sleep/Idle → Normal	< 5 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	
IRC ; 455K, 4M, 8M, 16MHz	Sleep/Idle → Normal	< 2 µs	32 CLK
	Green → Normal		
	Sleep/Idle → Green	< 100 µs	

NOTE

- *[1]The oscillator stable time depends on the oscillator characteristics.*
- *[2]After the oscillator has stabilized, the CPU will count 254/32 CLK in Normal/Green mode and continue to work in Normal/Green mode.*

Ex 1 : The 4 MHz IRC wakes-up from Sleep mode to Normal mode, the total wake-up time is 2 µs + 32 CLK @ 4 MHz.

Ex 2 : The 4 MHz IRC wakes-up from Sleep mode to Green mode, the total wake-up time is 100 µs + 32 CLK @ 16kHz.

Bits 3 ~ 0: Not used, set to “0” at all time.

6.1.11 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADIF	SPIIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

Note: **" 1 "** means with interrupt request **" 0 "** means no interrupt occurs

Bit 7: Not used, set to "0" at all time.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion.

Set when AD conversion is completed, reset by software.

Bit 5 (SPIIF): SPI mode interrupt flag. Flag is cleared by software.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) interrupt flag.

Set when a selected period is reached, reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag.

Set when a selected period is reached, reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

NOTE

- *RF can be cleared by instruction but cannot be set.*
- *IOCF is the interrupt mask register.*
- *The result of reading RF is the "logic AND" of RF and IOCF.*

6.1.12 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.1.13 Bank 1 R5 TC1CR (Timer 1 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	-	-

Bit 7 (TC1CAP): Software capture control

0 : Software capture disable

1 : Software capture enable

Bit 6 (TC1S): Timer/Counter 1 start control

0 : Stop and clear counter

1 : Start

Bit 5 ~ Bit 4 (TC1CK1 ~ TC1CK0): Timer/Counter 1 clock source select

TC1CK1	TC1CK0	Clock Source	Resolution (4 MHz)	Max. Time (4 MHz)	Resolution (16kHz)	Max. Time (16kHz)
		Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	$Fc/2^{12}$	1024 µs	262144 µs	256 ms	65536 ms
0	1	$Fc/2^{10}$	256 µs	65536 µs	64 ms	16384 ms
1	0	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
1	1	External clock (TC1 pin)	-	-	-	-

Bit 3 (TC1M): Timer/Counter 1 mode select

0 : Timer/Counter 1 mode

1 : Capture mode

Bit 2 (TC1ES): TC1 signal edge

0 : increment if the transition from low to high (rising edge) takes place on the TC1 pin.

1 : increment if the transition from high to low (falling edge) takes place on TC1 pin.

Bits 1 ~ 0: Not used, set to “0” at all time.

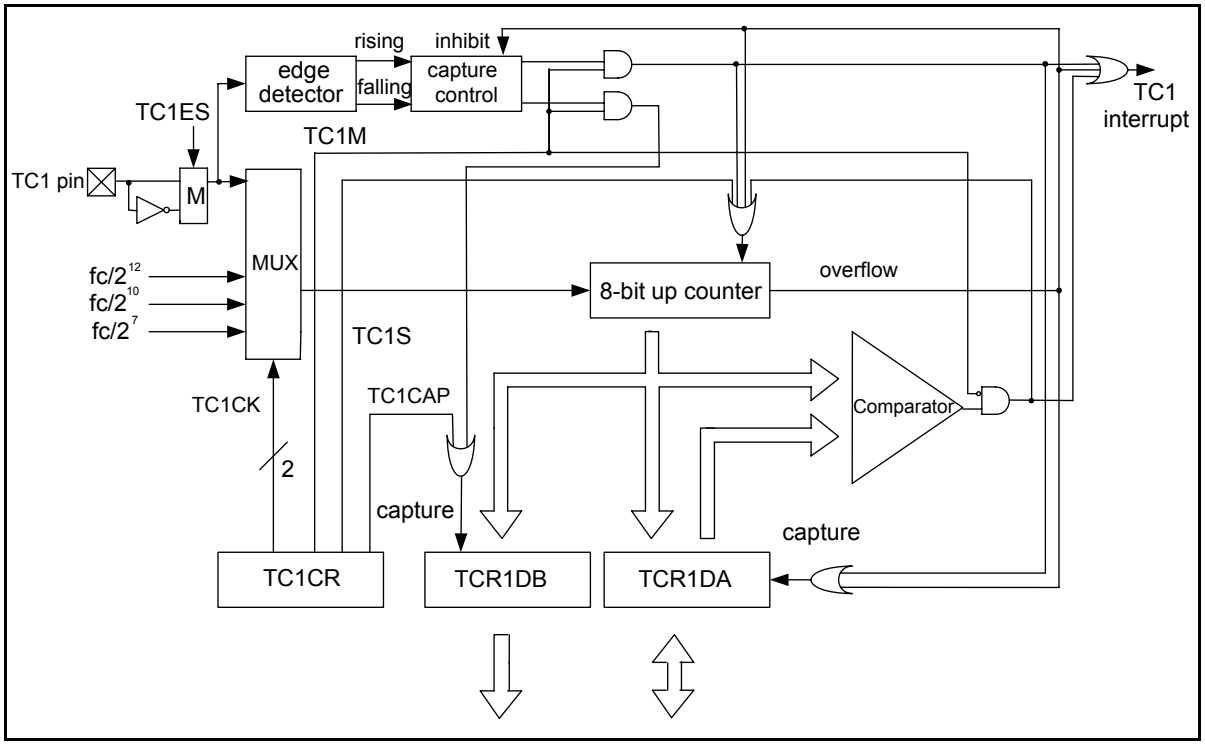


Figure 6-4 Timer/Counter 1 Configuration

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to “1” and the TC1CAP is automatically cleared to “0” after capture.

In Counter mode, counting up is performed using the external clock input pin (TC1 pin) and either rising or falling edge can be selected by TC1ES, **but both edges cannot be used**. When the contents of the up-counter matched with the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into the TCR1DB by setting TC1CAP to “1” and the TC1CAP is automatically cleared to “0” after capture.

In Capture mode, the pulse width, period and duty of the TC1 input pin are measured in this mode, which can be used to decode the remote control signal. The counter is set as free running by the internal clock. On a rising (falling) edge of TC1 pin input, the contents of the counter is loaded into TCR1DA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of the TC1 pin input, the contents of the counter are loaded into TCR1DB. The counter is still counting, on the next rising edge of the TC1 pin input, the contents of the counter are loaded into TCR1DA, the counter is cleared and interrupt is generated again. If an overflow occurs before an edge is detected, the FFH is loaded into TCR1DA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detection) is generated, capture and overflow detection are halted until TCR1DA is read out.

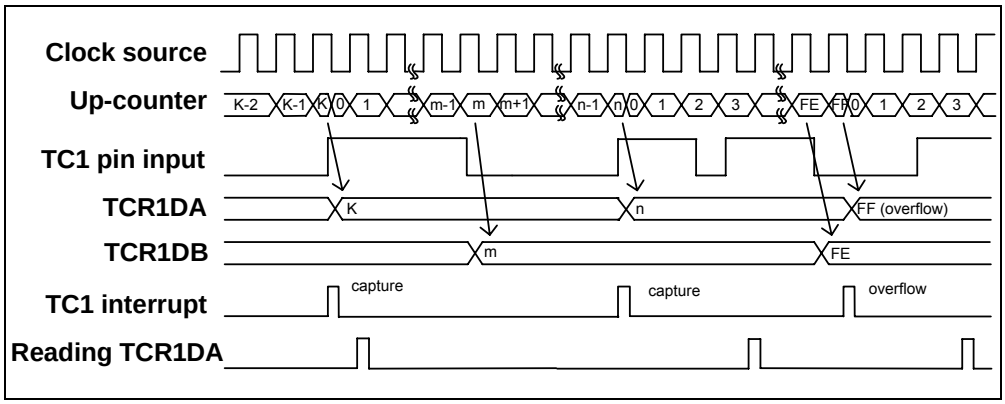


Figure 6-5 Timing Chart of Capture Mode

6.1.14 Bank 1 R6 TCR1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0

Bit 7 ~ Bit 0 (TCR1DA7 ~ TCR1DA0): Data buffer of 8-bit Timer/Counter 1.

6.1.15 Bank 1 R7 TCR1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0

Bit 7 ~ Bit 0 (TCR1DB7 ~ TCR1DB0): Data buffer of 8-bit Timer/Counter 1.

6.1.16 Bank 1 R8 TC2CR (Timer 2 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7 ~ 6 (RCM1 ~ RCM0): IRC mode selection bits. The Bank 1 R8<7,6> will be enabled when Word 1<12> COBS0 = ”1”.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
16 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 2.5%	4.5V ~ 5.5V	< 1.25 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
8 MHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 2.5%	3.0V ~ 5.5V	< 2.5 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs
455kHz	0	0	4 MHz ± 10%	2.2V ~ 5.5V	< 6 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 2.5%	2.2V ~ 5.5V	< 45 µs

NOTE

- *The initial values of Bank1 R8<7,6> will be kept the same as Word1<3,2>.*
- *If the user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

For Example:

1st step When user selects the 4 MHz at the Writer, the initial values of Bank 1 R8<7,6> would be “00”, the same as the value of Word 1<3,2> is “00”. If the MCU is free-running, it will work at 4 MHz ± 2.5%. Refer to the table below.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 µs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 µs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 µs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 µs

2nd step If it is desired to set Bank 1 R8<7,6> = "01" while the MCU is working at 4 MHz ± 2.5%, the MCU needs to hold for 1.5 μs, then it will continue to work at 16 MHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	**1**	**16 MHz ± 10%**	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 μs

3rd step If it is desired to set Bank 1 R8<7,6> = "11" while the MCU is working at 16 MHz ± 10%, the MCU needs to hold for 50 μs, then it will continue to work at 455kHz ± 10%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	0	0	4 MHz ± 2.5%	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	**1**	**455kHz ± 10%**	2.2V ~ 5.5V	< 50 μs

4th step If it is desired to set Bank 1 R8<7,6> = "00" while the MCU is working at 455kHz ± 10%, the MCU needs to hold for 5 μs, then it will continue to work at 4 MHz ± 2.5%.

Writer Trim IRC	Bank 1 R8<7,6>		Frequency	Operating Voltage Range	Stable Time
	RCM1	RCM0			
4 MHz	**0**	**0**	**4 MHz ± 2.5%**	2.2V ~ 5.5V	< 5 μs
	0	1	16 MHz ± 10%	4.5V ~ 5.5V	< 1.5 μs
	1	0	8 MHz ± 10%	3.0V ~ 5.5V	< 3 μs
	1	1	455kHz ± 10%	2.2V ~ 5.5V	< 50 μs

Bit 5 (TC2ES): TC2 signal edge

0 : increment if a transition from low to high (rising edge) takes place on the TC2 pin.

1 : increment if a transition from high to low (falling edge) takes place on the TC2 pin.

Bit 4 (TC2M): Timer/Counter 2 mode select

0 : Timer/counter mode

1 : Window mode

Bit 3 (TC2S): Timer/Counter 2 start control

0 : Stop and clear the counter

1 : Start

Bit 2 ~ Bit 0 (TC2CK2 ~ TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	0	$Fc/2^{23}$	2.1 sec	38.2 hr	524.3 s	9544 hr
0	0	1	$Fc/2^{13}$	2.048 ms	134.22 sec	512 ms	33554.432 s
0	1	0	$Fc/2^{8}$	64 µs	4.194 sec	16 ms	1048.576 s
0	1	1	$Fc/2^{3}$	2 µs	131.072 ms	0.5 ms	32768 ms
1	0	0	Fc	250 ns	16.384 ms	0.0625 ms	4096 ms
1	0	1	–	–	–	–	–
1	1	0	–	–	–	–	–
1	1	1	External clock (TC2 pin)	–	–	–	–

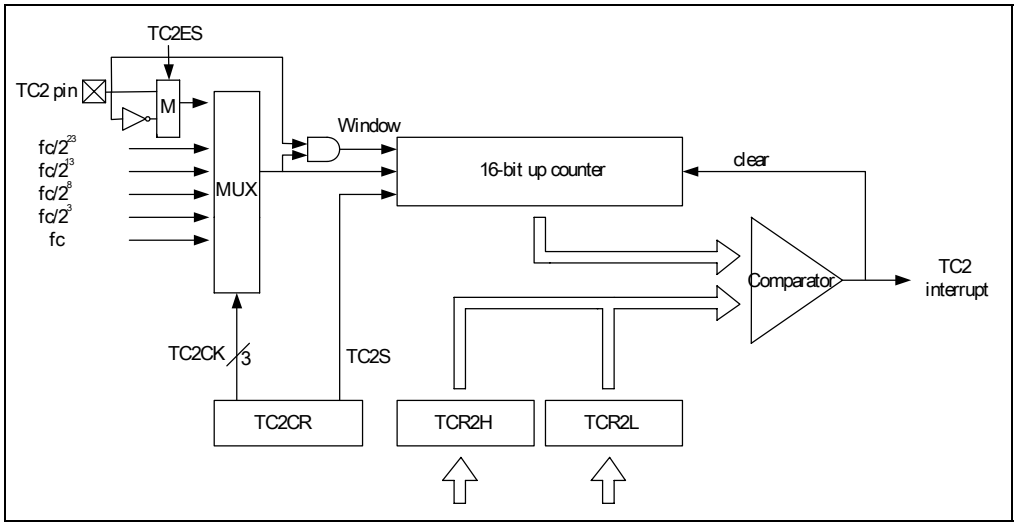


Figure 6-6 Configuration of Timer/Counter 2

In Timer mode, counting up is performed using internal clock. When the contents of the up-counter matched the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

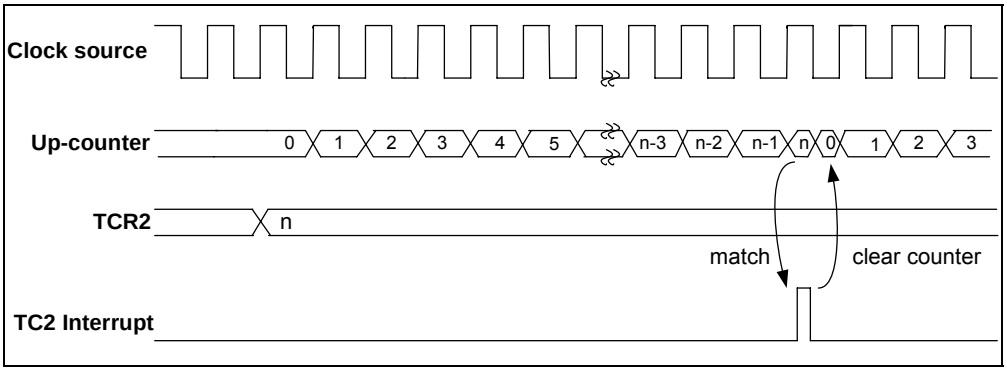


Figure 6-7 Timer Mode Timing Chart

In Counter mode, counting up is performed using external clock input pin (TC2) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter match the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

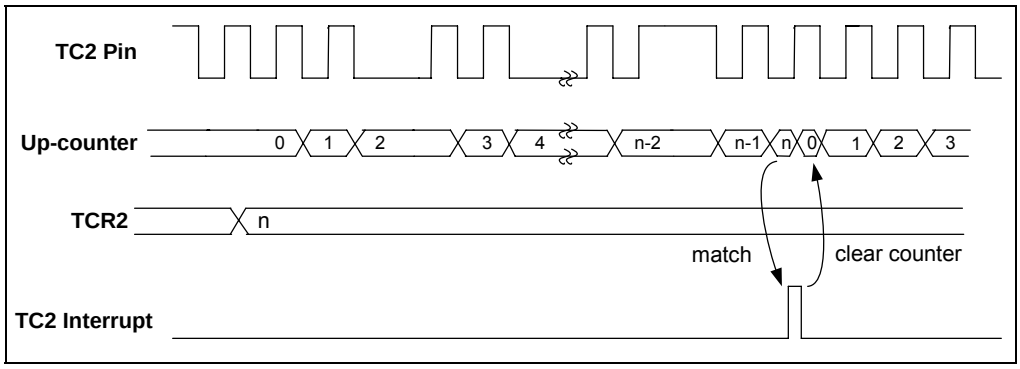


Figure 6-8 Counter Mode Timing Chart

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of up-counter match with the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

In Writing to the TCR2DL, comparison is inhibited until TCR2DH is written.

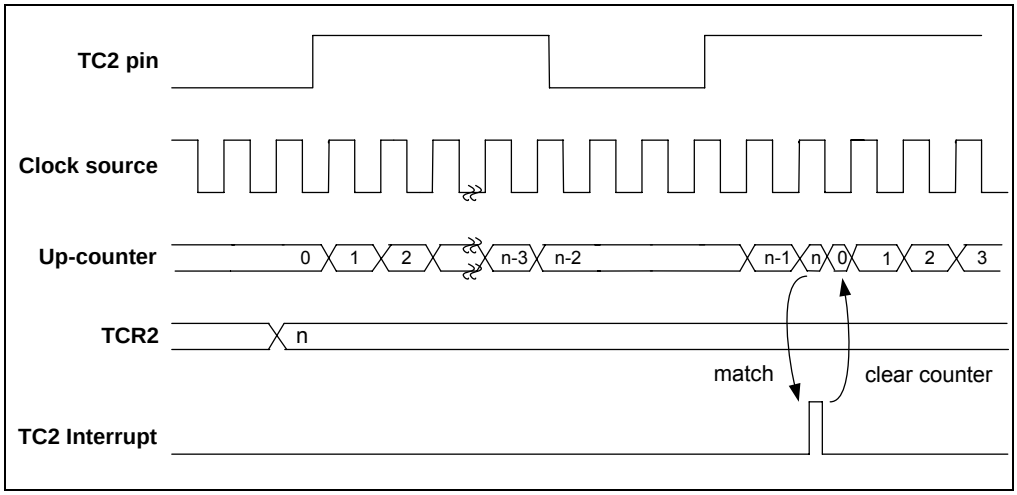


Figure 6-9 Window Mode Timing Chart

6.1.17 Bank 1 R9 TC2DH (Timer 2 High Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TCR2D15 ~ TCR2D8): High byte data buffer of 16-bit Timer/Counter 2.

6.1.18 Bank 1 RA TC2DL (Timer 2 Low Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0): Low byte data buffer of 16-bit Timer/Counter 2.

6.1.19 Bank 1 RB SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	-	OD3	OD4	-	RBF

Bit 7 (DORD): Data transmission order

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6 ~ Bit 5 (TD1 ~ TD0): SDO Status output Delay times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” at all time.

Bit 3 (OD3): Open-drain Control bit

0 : Open-drain disable for SDO

1 : Open-drain enable for SDO

Bit 2 (OD4): Open-drain Control bit

0 : Open-drain disable for SCK

1 : Open-drain enable for SCK

Bit 1: Not used, set to "0" at all time

Bit 0 (RBF): Read Buffer Full flag

0 : Receiving is not complete, SPIRB has not fully exchanged.

1 : Receiving completed; SPIRB is fully exchanged.

6.1.20 Bank 1 RC SPIC (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during low-level.

1 : Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only transmission is implemented.

This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 : Reset as soon as the shifting is complete, and the next byte is ready to shift.

1 : Start to shift, and keep at "1" while the current byte is still being transmitted.

This bit will reset to 0 at every 1-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit:

0 : After the Serial data output, the SDO remains high.

1 : After the Serial data output, the SDO remains low.

Bit 2 ~ Bit 0 (SBRS 2 ~ SBRS0): SPI Baud Rate Select bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.21 Bank 1 RD SPIRB (SPI Read Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bit 7 ~ Bit 0 (SPID7 ~ SPID0): SPI Read data buffer

6.1.22 Bank 1 RE SPIWB (SPI Write Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bit 7 ~ Bit 0 (SWB7 ~ SWB0): SPI Write data buffer

6.1.23 Bank 1 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	-	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF

Bit 7 (CMP2IF): Comparator 2 Interrupt Flag. Set when a change occurs in the Comparator 2 output, reset by software.

Bit 6: Not used, set to ”0” at all time.

Bit 5 (TC3IF): 8-bit Timer/Counter 3 Interrupt Flag.

Bit 4 (TC2IF): 16-bit Timer/Counter 2 Interrupt Flag.

Bit 3 (TC1IF): 8-bit Timer/Counter 1 Interrupt Flag.

Bit 2 (UERRIF): UART receiving error interrupt flag.

Bit 1 (RBFF): UART receive mode data buffer full interrupt flag.

Bit 0 (TBEF): UART transmit mode data buffer empty interrupt flag.

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

6.1.24 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register individually defines the Port 6 pins as analog input or digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin.

0 : Disable ADC7, P67 act as I/O pin.

1 : Enable ADC7 to act as analog input pin.

Bit 6 (ADE6): AD converter enable bit of P66 pin.

0 : Disable ADC6, P66 act as I/O pin.

1 : Enable ADC6 to act as analog input pin.

Bit 5 (ADE5): AD converter enable bit of P65 pin

0 : Disable ADC5, P65 functions as I/O pin.

1 : Enable ADC5 to function as analog input pin.

Bit 4 (ADE4): AD converter enable bit of P64 pin

0 : Disable ADC4, P64 act as I/O pin.

1 : Enable ADC4 to act as analog input pin.

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0 : Disable ADC3, P63 act as I/O pin.

1 : Enable ADC3 to act as analog input pin.

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0 : Disable ADC2, P62 act as I/O pin.

1 : Enable ADC2 to act as analog input pin.

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 : Disable ADC1, P61 act as I/O pin

1 : Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0 : Disable ADC0, P60 act as I/O pin.

1 : Enable ADC0 to act as analog input pin.

The following table shows the priority of P60/ADC0//INT.

P60 / ADC0 / /INT Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.25 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the Vref of the ADC.

0 : Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1 : Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of ADC oscillator clock rate

00 = 1: 4 (default value)

01 = 1: 1

10 = 1: 16

11 = 1: 2

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
01	F_{OSC}	1 MHz
10	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0 : reset on completion of AD conversion. This bit cannot be reset by software.

1 : A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : switch off the resistor reference to save power even while the CPU is operating.

1 : ADC is operating.

Bits 2 ~ 0 (ADIS2~ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = AN6/P66

111 = AN7/P67

The following table shows the priority of P50/VREF//SS pin. They can only be changed when the ADIF bit and the ADRUN bit are both low.

P50/VREF//SS Pin Priority		
High	Medium	Low
/SS	VREF	P50

6.1.26 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-

Bit 7 (CALI): Calibration enable bit for A/D offset

0 : Calibration disable

1 : Calibration enable

Bit 6 (SIGN): Polarity bit of offset voltage

0 : Negative voltage

1 : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

Bits 2 ~ 0: Not used, set to "0" at all time.

6.1.27 Bank 2 R8 ADDH (AD High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

When the A/D conversion is completed, the result of high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.28 Bank 2 R9 ADDL (AD Low 2-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	AD1	AD0

Bits 7 ~ 2: Unimplemented, read as '0'.

Bits 1 ~ 0 (AD1~AD0): AD low 2-bit data buffer. R9 is read only.

6.1.29 Bank 2 RA URC1 (UART Control 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (URTD8): Transmission Data Bit 8

Bit 6 ~ Bit 5 (UMODE1 ~ UMODE0): UART mode

UMODE1	UMODE0	UART Mode
0	0	Mode 1: 7-bit
0	1	Mode 1: 8-bit
1	0	Mode 1: 9-bit
1	1	Reserved

Bit 4 ~ Bit 2 (BRATE2 ~ BRATE0): Transmit Baud Rate Select

BRATE2	BRATE1	BRATE0	Baud Rate	4 MHz	8 MHz
0	0	0	Fc/13	19200	38400
0	0	1	Fc/26	9600	19200
0	1	0	Fc/52	4800	9600
0	1	1	Fc/104	2400	4800
1	0	0	Fc/208	1200	2400
1	0	1	Fc/416	600	1200
1	1	0	TC3	–	–
1	1	1	Reserved		

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Automatically reset to 0 when writing to the URTD register. The **UTBE** bit will be cleared by hardware when enabling transmission. The **UTBE** bit is read-only. Therefore, writing to the URTD register is necessary when user wants to start transmit shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.30 Bank 2 RB URC2 (UART Control 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBIM1	SBIM0	UINVEN	-	-	-

Bits 7 ~ 6: Not used, set to “0” at all time.

Bit 5 ~ Bit 4 (SBIM1 ~ SBIM0): Serial bus interface operating mode select.

SBIM1	SBIM0	Operating Mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	Reserved

Bit 3 (UNIVEN): Enable UART TXD and RXD port inverse output.

0: Disable **TXD** and **RXD** port inverse output.

1: Enable **TXD** and **RXD** port inverse output.

Bits 2 ~ 0: Not used, set to ”0” at all time

6.1.31 Bank 2 RC URS (UART Status)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URRD8): Receiving Data Bit 8

Bit 6 (EVEN): Select parity check

0 : Odd parity

1 : Even parity

Bit 5 (PRE): Enable parity addition

0 : Disable

1 : Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error occurred.

Bit 3 (OVERR): Over running error flag. Set to 1 when an overrun error occurred.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error occurred.

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URS and URRD register. The **URBF** will be cleared by hardware when enabling receiving. The URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0 : Disable

1 : Enable

6.1.32 Bank 2 RD URRD (UART_RD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7 ~ 0 (URRD7 ~ URRD0): UART receive data buffer. **Read only.**

6.1.33 Bank 2 RE URTD (UART_TD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7 ~ 0 (URTD7 ~ URTD0): UART transmit data buffer. **Write only.**

6.1.34 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	“1”	“1”

Bit 7 (/PH77): Control bit used to enable pull-high of the P77 pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 6 (/PH76): Control bit used to enable pull-high of the P76 pin.

Bit 5 (/PH75): Control bit used to enable pull-high of the P75 pin.

Bit 4 (/PH74): Control bit used to enable pull-high of the P74 pin.

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin.

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin.

Bits 1 ~ 0: Not used, set to “1” at all time.

The RF Register is both readable and writable.

6.1.35 Bank 3 R5 (TMRCON: Timer A and Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAEN	TAP2	TAP1	TAP0	TBEN	TBP2	TBP1	TBP0

Bit 7 (TAEN): Timer A enable bit.

0 : disable Timer A (default)

1 : enable Timer A

Bits 6 ~ 4 (TAP2 ~ TAP0): Timer A clock prescaler option bits.

Bit 3 (TBEN): Timer B enable bit.

0 : disable Timer B (default)

1 : enable Timer B

Bits 2 ~ 0 (TBP2 ~ TBP0): Timer B clock prescaler option bits.

TAP2/TBP2	TAP1/TBP1	TAP0/TBP0	Prescale
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.36 Bank 3 R6 (TBHP : Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	RBit11	RBit10	RBit9	RBit8

Bit 7 (MLB): Choosing MSB or LSB machine code to be moved to the register.

The machine code is pointed by TBLP and TBHP register.

Bits 6 ~ 4: Not used, set to “0” at all time.

Bits 3 ~ 0: These are the most 4 significant bits of address for program code.

6.1.37 Bank 3 R7 (CMPCON: Comparator 2 Control Register and PWMA/B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	CPOUT2	COS21	COS20	PWMAE	PWMBE

Bit 7 ~ Bit 5: Not used, set to “0” at all time.

Bit 4 (CPOUT2): The result of Comparator 2 output.

Bit 3 ~ Bit 2 (COS21 ~ COS20): Comparator 2 Select bits.

COS21	COS20	Function Description
0	0	Comparator 2 is not used, P80 act as normal I/O pin
0	1	Act as a Comparator 2 and P80 act as normal I/O pin
1	0	Act as a Comparator 2 and P80 act as Comparator 2 output pin (CO)
1	1	Not used

Bit 1 (PWMAE): PWMA enable bit.

0 : PWMA is off and its related pin carries out the P75 function (default).

1 : PWMA is on, and its related pin will be set automatically to output.

Bit 0 (PWMBE): PWMB enable bit.

0 : PWMB is off and its related pin carries out the P76 function (default).

1 : PWMB is on, and its related pin will be set automatically to output.

6.1.38 Bank 3 R8 (PWMCON: PWMA/B Lower 2 Bits of the Period and Duty Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA [1]	PRDA [0]	DTA [1]	DTA [0]	PRDB [1]	PRDB [0]	DTB [1]	DTB [0]

Bits 7 ~ 6 (PRDA [1], PRDA [0]): Least Significant Bits of PWMA Period Cycle.

Bits 5 ~ 4 (DTA [1], DTA [0]): Least Significant Bits of PWMA Duty Cycle.

Bits 3 ~ 2 (PRDB [1], PRDB [0]): Least Significant Bits of PWMB Period Cycle.

Bits 1 ~ 0 (DTB [1], DTB [0]): Least Significant Bits of PWMB Duty Cycle.

6.1.39 Bank 3 R9 (PRDAH: Most Significant Byte (Bit 9 ~ Bit 2) of PWMA)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA [9]	PRDA [8]	PRDA [7]	PRDA [6]	PRDA[5]	PRDA [4]	PRDA [3]	PRDA [2]

The content of Bank 3 of R9 is a period (time base) of PWMA Bit 9~Bit 2. The frequency of PWMA is the reverse of the period.

6.1.40 Bank 3 RA (DTAH: Most Significant Byte (Bit 9 ~ Bit 2) of PWMA Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

A specified value keeps the output of PWMA to remain high until the value matches with TMRA.

6.1.41 Bank 3 RB (PRDBH: Most Significant Byte (Bit 9~Bit 2) of PWMB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

The content of Bank 3 of RB is a period (time base) of PWMB Bit 9 ~ Bit 2. The frequency of PWMB is the reverse of the period.

6.1.42 Bank 3 RC (DTBH: Least Significant Byte (Bit 9 ~ Bit 2) of PWMB Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

A specified value keeps the output of PWMB to remain at high until the value matches with TMRB.

6.1.43 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0 : Stop and clear the counter

1 : Start

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	0	$Fc/2^{11}$	512 µs	131072 µs	128 ms	32768 ms
0	0	1	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
0	1	0	$Fc/2^{5}$	8 µs	2048 µs	2 ms	512 ms
0	1	1	$Fc/2^{3}$	2 µs	512 µs	500 µs	128 ms
1	0	0	$Fc/2^{2}$	1 µs	256 µs	250 µs	64 ms
1	0	1	$Fc/2^{1}$	500 ns	128 µs	125 µs	32 ms
1	1	0	Fc	250 ns	64 µs	62.5 µs	16 ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider Output
1	1	Pulse Width Modulation Output

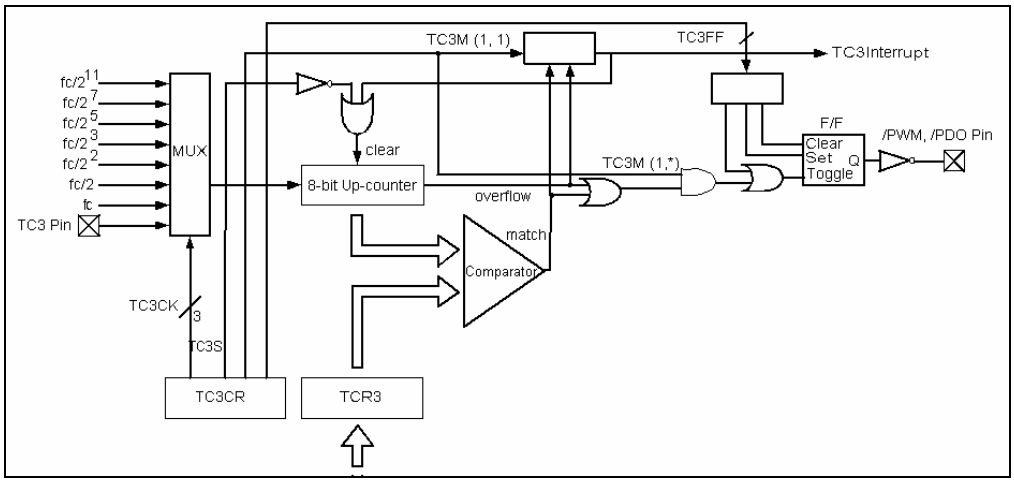


Figure 6-10 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using an external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time the /PDO output is toggled.

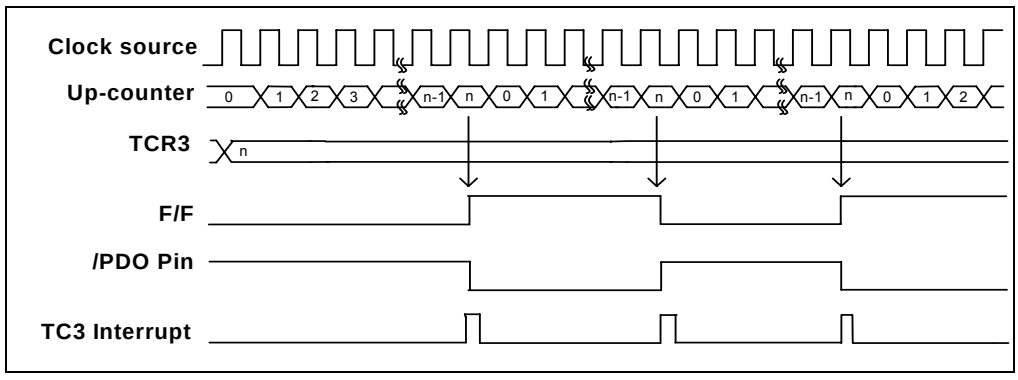


Figure 6-11 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output Mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the first time, TCR3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

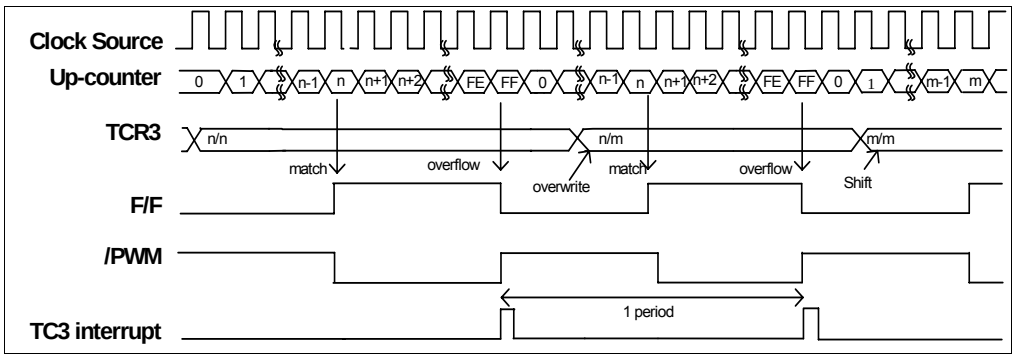


Figure 6-12 (a) PWM Mode Timing Chart

6.1.44 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bits 7 ~ 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3.

6.1.45 Bank 3 RF (Pull-down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD77	/PD76	/PD75	/PD74	/PD73	/PD72	"1"	"1"

Bit 7 (/PD77): Control bit used to enable pull-down of the P77 pin.

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD76): Control bit used to enable pull-down of the P76 pin.

Bit 5 (/PD75): Control bit used to enable pull-down of the P75 pin.

Bit 4 (/PD74): Control bit used to enable pull-down of the P74 pin.

Bit 3 (/PD73): Control bit used to enable pull-down of the P73 pin.

Bit 2 (/PD72): Control bit used to enable pull-down of the P72 pin.

Bits 1 ~ 0: Not used, set to "1" at all time.

The RF Register is both readable and writable.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0 : interrupt occurs at a rising edge of the INT pin

1 : interrupt occurs at a falling edge of the INT pin

Bit 6 (/INT): Interrupt enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock

1 : transition on TCC pin

Bit 4 (TE): TCC signal edge

0 : increment if a transition from low to high takes place on the TCC pin

1 : increment if a transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0 : prescaler disable bit, TCC rate is 1:1

1 : prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC8 (I/O Port Control Register)

A value of "1" sets the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

IOC5 ~ IOC8 registers are both readable and writable.

6.2.4 IOC9

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0 : P60, bidirectional I/O pin

1 : /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1".

When EIS is "0", the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6).

The EIS is both readable and writable.

Bits 5 ~ 4: Not used, set to “0” at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	/PD53	/PD52	/PD51	/PD50

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bit 3 (/PD53): Control bit used to enable pull-down of the P53 pin.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

The IOCB Register is both readable and writable.

6.2.7 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain output of the P67 pin.

0 : Disable open-drain output

1 : Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain output of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain output of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain output of the P64 pin.

Bit 3 (OD63): Control bit used to enable open-drain output of the P63 pin.

Bit 2 (OD62): Control bit used to enable open-drain output of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain output of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin.

The IOCC Register is both readable and writable.

6.2.8 IOCD (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0 : Disable CMP2IF interrupt

1 : Enable CMP2IF interrupt

When the Comparator 2 output status changed is used to enter an interrupt vector or enter the next instruction, the CMP2IE bit must be set to “Enable“.

Bit 6: Not used, set to “0” at all time.

Bit 5 (TC3IE): Interrupt enable bit

0 : Disable TC3IF interrupt

1 : Enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit

0 : Disable TC2IF interrupt

1 : Enable TC2IF interrupt

Bit 3 (TC1IE): Interrupt enable bit

0 : Disable TC1IF interrupt

1 : Enable TC1IF interrupt

Bit 2 (UERRIE): UART receive error interrupt enable bit.

0 : Disable UERRIF interrupt

1 : Enable UERRIF interrupt

Bit 1 (URIE): UART receive mode Interrupt enable bit.

0 : Disable RBFF interrupt

1 : Enable RBFF interrupt

Bit 0 (UTIE): UART transmit mode interrupt enable bit.

0 : Disable TBEF interrupt

1 : Enable TBEF interrupt

NOTE

- *User must set to "0" Bit 6 of the IOCE register.*
- *The IOCE register is both readable and writable.*

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADIE	SPIIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bit 7: Not used, set to "0" at all time

Bit 6 (ADIE): ADIF interrupt enable bit

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC complete status is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to "Enable".

Bit 5 (SPIIE): SPIIF interrupt enable bit.

0 : Disable SPIIF interrupt

1 : Enable SPIIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit.

0 : Disable PWMBIF interrupt

1 : Enable PWMBIF interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit.

0 : Disable PWMAIF interrupt

1 : Enable PWMAIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0 : Disable EXIF interrupt

1 : Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

NOTE

- *User must set to "0" Bit 7 of the IOCF register.*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.*
- *The IOCF register is both readable and writable.*

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2~PST0 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW2~PSW0 bits of the IOCA register are used to determine the prescaler of WDT. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-12-1 depicts the EM78F564N circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be an internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). If the TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at high or low level) must be greater than 1/ Fc. **The TCC will stop running when sleep mode occurs**.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to the WDTE bit of the IOCA register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

[1] **Note:** VDD=5V, WDT time-out period = 16ms ± 7.5%
VDD=3V, WDT time-out period = 18ms ± 7.5%

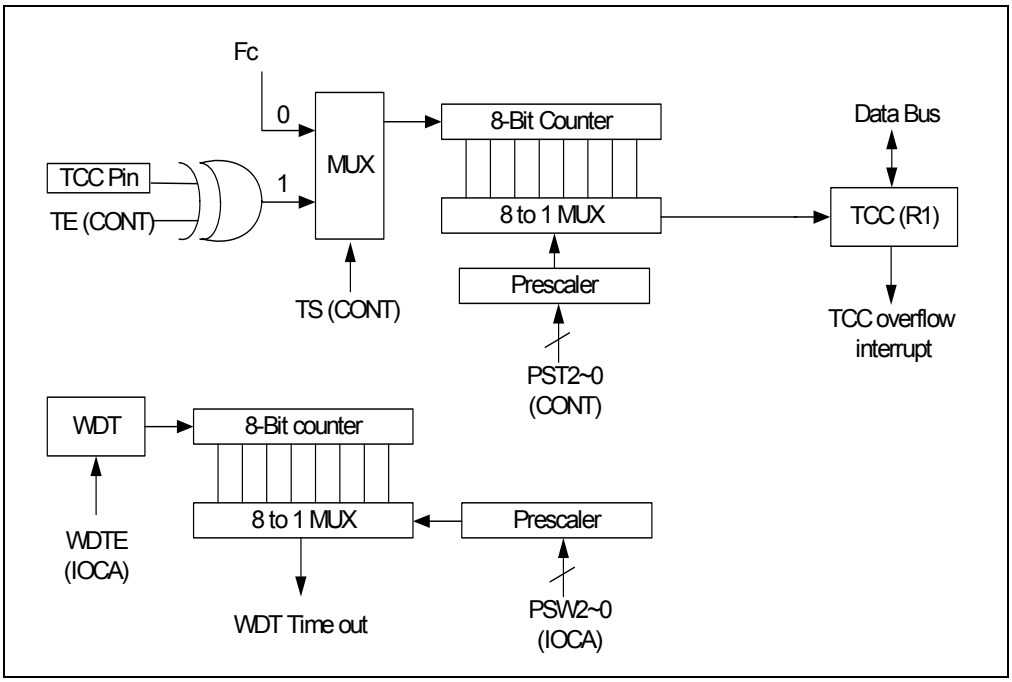
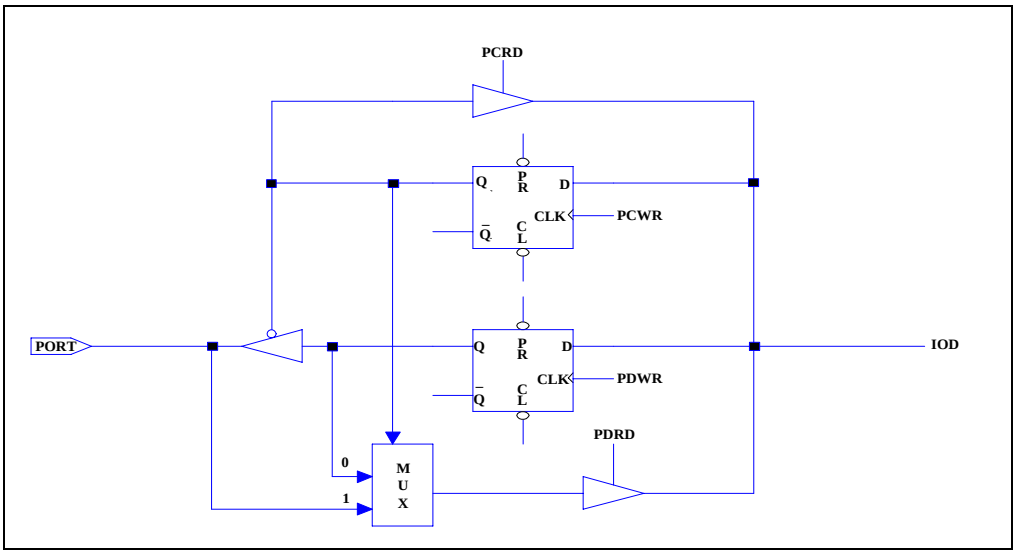


Figure 6-12 (b) EM78F564N Block Diagram of TCC and WDT

6.4 I/O Ports

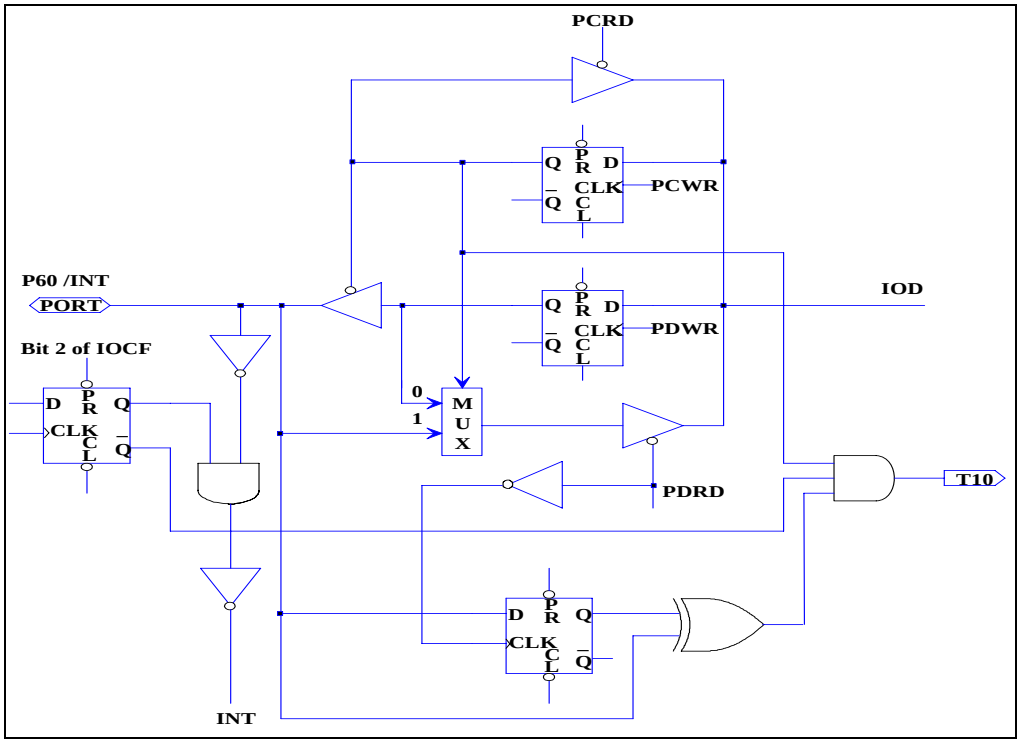
The I/O registers, Ports 5, 6, 7 and 8, are bidirectional tri-state I/O ports. Port 6 or 7 can be pulled high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6 P50~P53, P60 ~ P63 and Port 7 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Ports 5 ~ 8 are shown in the following Figures 6-13, 6-14 (a), 6-14 (b), and Figure 6-15.



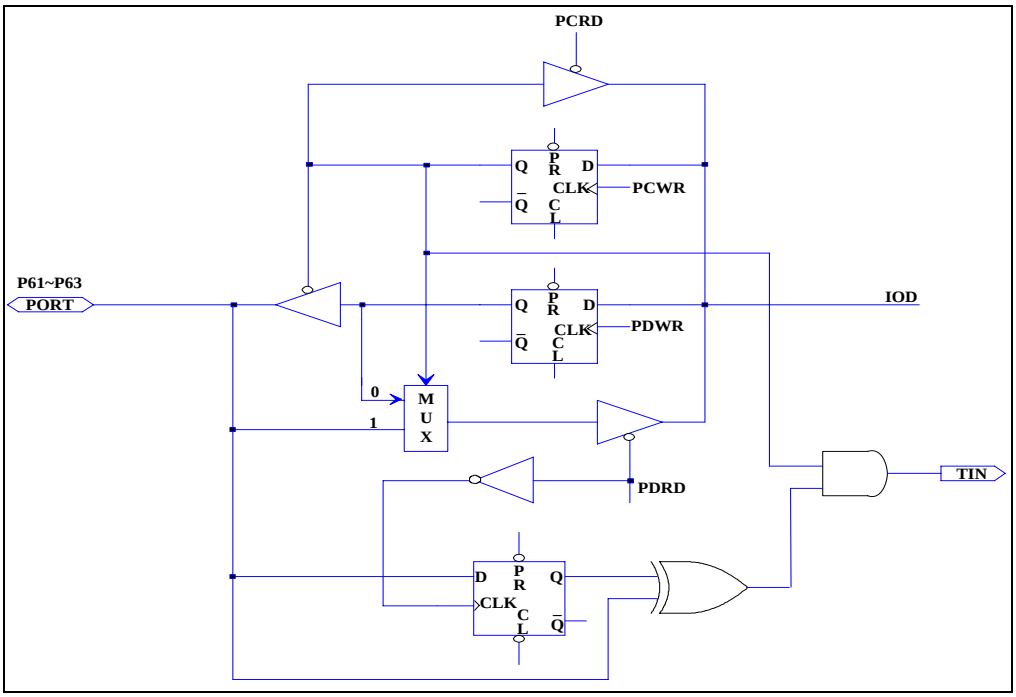
Note: Pull-down is not shown in the figure.

Figure 6-13 I/O Port and I/O Control Register Circuit for Ports 5 ~ 8



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-14 (a) I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-14 (b) I/O Port and I/O Control Register Circuit for P61~P67, P72~P77

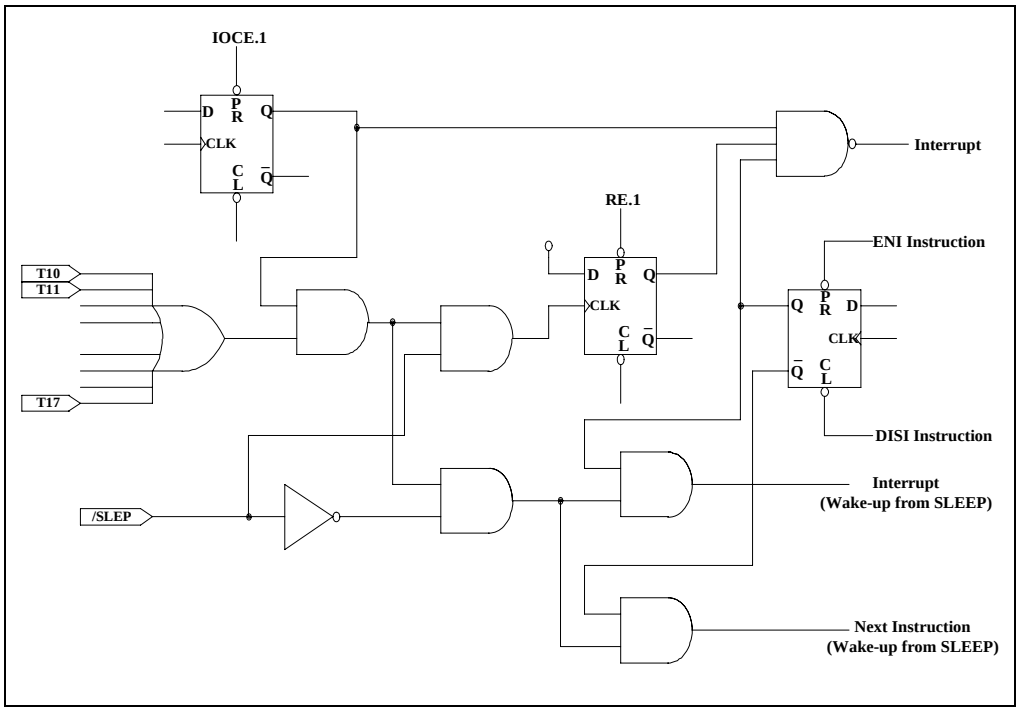


Figure 6-15 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 6.4-1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3 a. Enable interrupt (Set IOCF.1), after wake-up if “ENI” switch to interrupt vector (006H), if “DISI” excute next instruction 3 b. Disable interrupt (Set IOCF.1), always execute next instruction 4. Enable wake-up enable bit (Set RA.6) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt Vector (006H)

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18 ms[3] (one oscillator start-up timer period) after a reset is detected.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.

Note: [2] The Software disables WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change wake-up function. (Code Option Register and Bit 6 (ENWDTB) are set to “1”).

[3] Vdd = 5V, set up time period = 16ms ± 7.5%
Vdd = 3V, set up time period = 18ms ± 7.5%

- The bits of the RB, RC, RD registers are set to their previous status.
- The bits of the CONT register are set to all "0".
- The bits of the IOCA register are set to all "0".
- The bits of the IOCB register are set to all "1".
- The bits of the IOCC register are set to all "0".
- The bits of the IOCD register are set to all "1".
- The bits of the IOCE register are set to all "0".
- The bits of the IOCF register are set to all "0".

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, the WDT (if enabled) is cleared but keeps on running. After a wake-up, in RC mode the wake-up time is 10 µs. High crystal mode wake-up time is 800 µs.

The controller can be awakened by:

(1) External reset input on /RESET pin
(2) WDT time-out (if enabled)
(3) Port 6 input status changes (if enabled)
(4) Comparator output status change (if CMPWE is enabled)
(5) A/D conversion completed (if ADWE is enabled)
(6) External (P60, /INT) pin changes (if EXWE is enabled)
(7) SPI received data, When SPI act as slave device (if SPIWE is enabled)

The first two cases will cause the EM78F564N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5, 6, 7 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0×6, 0×15, 0×30, 0×3, 0×12 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. After a wake-up, in RC mode the wake-up time is 10 µs. High crystal mode wake-up time is 800 µs.

One or more of Cases 2 to 7 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78F564N can be awakened only by Case 1 or 2. Refer to the Interrupt section for further details.

[b] If Port 6 Input Status Change is used to wake-up the EM78F564N and the ICWE bit of RA register is enabled before SLEP, WDT must be disabled. Hence, the EM78F564N can be woke-up only by Case 3.

[c] If Comparator 2 output status change is used to wake-up the EM78F564N and the CMPWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F564N can be waken-up only by Case 4

[d] If AD conversion completed is used to wake-up the EM78F564N and the ADWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F564N can be waken-up only by Case 5.

[e] If External (P60,/INT) pin change is used to wake-up EM78F564N and EXWE bit of RA register is enabled before SLEP, WDT must be disabled. Hence, the EM78F564N can be wake-up only by Case 6.

[f] When SPI act as slave device, after receiving data, it will wake-up the EM78F564N and the SPIWE bit of RA register is enabled before SLEP, and WDT must be disabled by software. Hence, the EM78F564N can be waken-up only by Case 7.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78F564N, (as in Case [b] above), the following instructions must be executed before SLEP:

```
MOV             A, @0xxx1000b  ; Select WDT prescaler and
                               ; Disable the WDT
IOW             IOCA
WDTC                           ; Clear WDT and prescaler
MOV             R6, R6         ; Read Port 6
ENI (or DISI)                  ; Enable (or disable) global
                               ; interrupt
BC              R4, 7          ; Select Bank 0
BC              R4, 6
MOV             A, @0100xxxxb  ; Enable Port 6 input change
                               ; wake-up bit
MOV             RA,A
MOV             A, @xxxxxx1xb  ; Enable Port 6 input change
                               ; interrupt
IOW             IOCF
SLEP                           ; Sleep
```

Similarly, if the Comparator 2 Interrupt is used to wake-up the EM78F564N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BS              R4, 7           ; Select Bank 3
BS              R4, 6
MOV             A, @xxxx10xxb   ; Select a comparator and P80 act
                                ; as CO pin
MOV             R7,A
MOV             A, @0xxx1000b   ; Select WDT prescaler and
                                ; Disable the WDT
IOW             IOCA
WDTC                            ; Clear WDT and prescaler
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
BC              R4, 7           ; Select Bank 0
BC              R4, 6
MOV             A, @1000xxxxb   ; Enable comparator output status
                                ; change wake-up bit
MOV             RA,A
MOV             A, @10000000b   ; Enable comparator output status
                                ; change interrupt
IOW             IOCE
SLEP                            ; Sleep
```

All kinds of wake-up mode and interrupt mode are shown below:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	If EXWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction	If EXWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Port 6 pin change	If ICWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction	If ICWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCC overflow interrupt	×	Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
SPI interrupt	If SPIWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction **SPI must be in slave mode**	If SPIWE bit is enabled: Wake-up+ interrupt (if interrupt is enabled)+ next instruction **SPI must be in slave mode**	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Comparator 2 (Comparator Output Status Change)	If CMPWE bit is enabled: Wake-up + interrupt (if interrupt is enabled)+ next instruction	If CMPWE bit is enabled: Wake-up + interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TC1 interrupt	×	Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
UART Transmit complete interrupt	×	×	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
UART Receive data buffer full interrupt	×	×	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
UART Receive error interrupt	×	×	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TC2 interrupt	×	Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TC3 interrupt	×	Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
PWM A/B (When TimerA/B Match PRDA/B)	×	Wake-up+ interrupt (if interrupt is enabled)+ next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
AD Conversion Complete Interrupt	If ADWE bit is enabled: Wake-up + interrupt (if interrupt is enabled)+ next instruction **Fm and Fs don't stop**	If ADWE bit is enabled: Wake-up + interrupt (if interrupt is enabled)+ next instruction **Fm and Fs don't stop**	interrupt (if interrupt is enabled)+ next instruction **Fm and Fs don't stop**	Interrupt (if interrupt is enabled) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

After wake up:

1. If interrupt is enabled → interrupt + next instruction
2. If interrupt is disabled → next instruction

Table 6.5-1 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	-	-	-	-	-	C82	C81	C80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to interrupt vector address or continue to execute next instruction.							

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	Bank 1	Bank 0	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	P5 (Bank 0)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6 (Bank 0)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	P7 (Bank 0)	Bit Name	P77	P76	P75	P74	P73	P72	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	P8 (Bank 0)	Bit Name	-	-	-	-	-	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 0)	Bit Name	CMP2WE	ICWE	ADWE	EXWE	SPIWE	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0E	RE (Bank 0)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET and WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR) (Bank 0)	Bit Name	-	ADIF	SPIIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 1)	Bit Name	TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 1)	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 1)	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 1)	Bit Name	RCM1	RCM0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	WORD1<3,2>		0	0	0	0	0	0
		/RESET and WDT	WORD1<3,2>		0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 1)	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 1)	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 1)	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0C	RC (Bank 1)	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 1)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 1)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 1)	Bit Name	CMP2IF	-	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 2)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 2)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 2)	Bit Name	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 2)	Bit Name	-	-	-	-	-	-	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	RA (Bank 2)	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 2)	Bit Name	-	-	SBIM1	SBIM0	UINVEN	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 2)	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 2)	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 2)	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 2)	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 3)	Bit Name	TAEN	TAP2	TAP1	TAP0	TBEN	TBP2	TBP1	TBP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (Bank 3)	Bit Name	MLB	-	-	-	RBit11	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 3)	Bit Name	-	-	-	CPOUT2	COS21	COS20	PWMAE	PWMBE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×08	R8 (Bank 3)	Bit Name	PRDA[1]	PRDA[0]	DTA[1]	DTA[0]	PRDB[1]	PRDB[0]	DTB[1]	DTB[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 3)	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 3)	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 3)	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 3)	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 3)	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 3)	Bit Name	/PD77	/PD76	/PD75	/PD74	/PD73	/PD72	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	IOCA	Bit Name	WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0
		Power-un	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	CMP2IE	-	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	-	ADIE	SPIIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **"x"** = not used **"P"** = previous value before reset

"u" = unknown or don't care **"t"** = check Table 6-5-2-1

6.5.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition

2. High-low-high pulse on /RESET pin

3. Watchdog timer time-out

The values of T and P, listed in Table 6-5-2-1 are used to check how the processor wakes up. Table 6-5-2-2 shows the events that may affect the status of T and P.

Table 6-5-2-1 Values of RST, T and P after Reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

Table 6-5-2-2 Status of T and P Being Affected by Events.

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

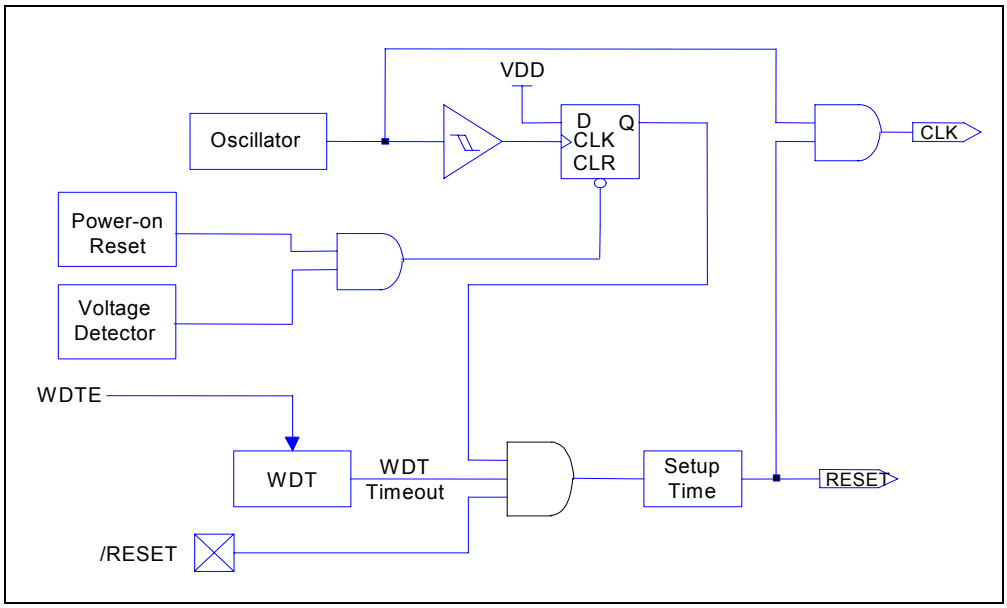


Figure 6-16 Block Diagram of Controller Reset

6.6 Interrupt

The EM78F564N has 14 interrupts (3 external, 11 internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	SPI	ENI + SPIIE=1	SPIIF	0012	4
External	Comparator 2	ENI+CMP2IE=1	CMP2IF	0015	5
Internal	TC1	ENI + TC1IE=1	TC1IF	0018	6
Internal	UART Transmit	ENI + UTIE=1	TBEF	001B	7
Internal	UART Receive	ENI + URIE=1	RBFF	001E	8
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	0021	9
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	10
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	11
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	12
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	13
Internal	AD	ENI+ADIE=1	ADIF	0030	14

RE and RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF and RE) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt has an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), **but in Low Crystal oscillator (LXT) mode, the noise rejection circuit will be disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 and R4 will be pushed back.

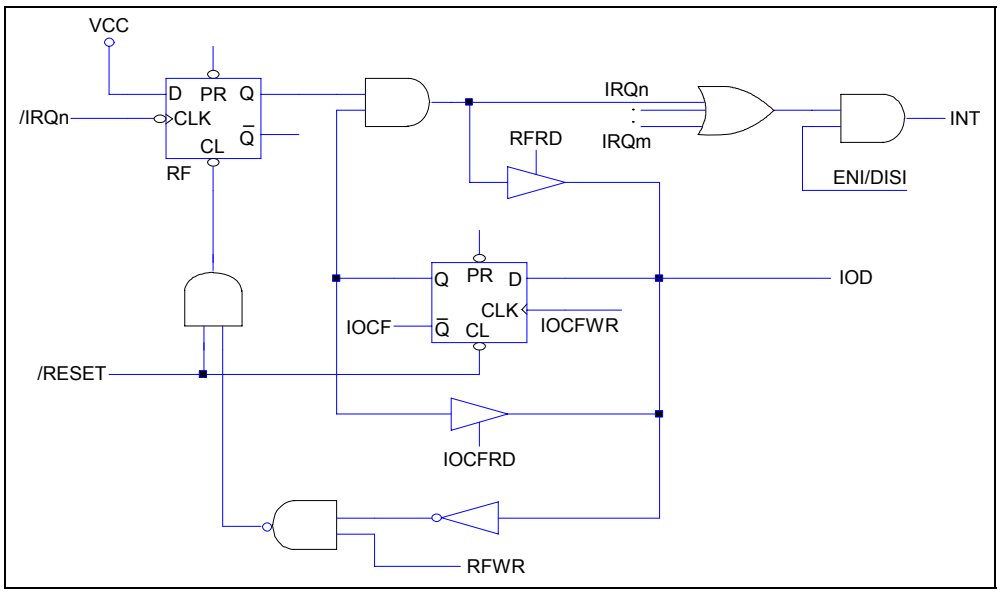


Figure 6-17 Interrupt Input Circuit

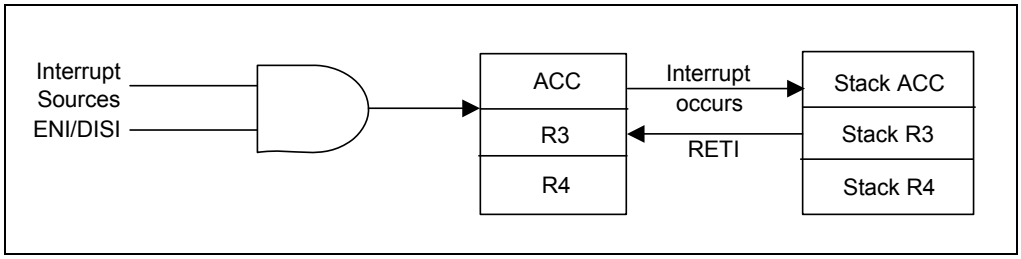


Figure 6-18 Interrupt Back-up Diagram

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 10-bit analog multiplexer, three control registers [AISR/R5 (Bank 2), ADCON/R6 (Bank 2), ADOC/R7 (Bank 2)], two data registers (ADDH, ADDL/R8, R9) and an ADC with 10-bit resolution. The functional block diagram of the ADC is shown in Figure 6-19. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2 ~ ADIS0.

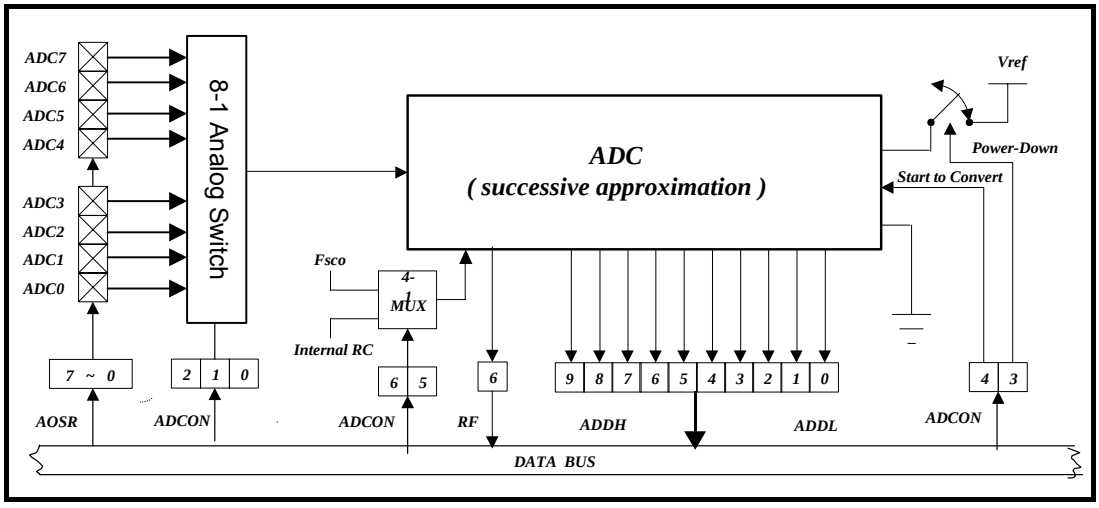


Figure 6-19 Functional Block Diagram of Analog-to-Digital Conversion

6.7.1 ADC Control Register (AISR/R5, ADCON/R6, ADOC/R7)

6.7.1.1 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register individually defines the Port 6 pins as analog input or as digital I/O.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
*Init_Value	0	0	0	0	0	0	0	0

Bit 7 (ADE7): AD converter enable bit of P67 pin.

0 : Disable ADC7, P67 functions as I/O pin

1 : Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

0 : Disable ADC6, P66 functions as I/O pin

1 : Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin

0 : Disable ADC5, P65 functions as I/O pin

1 : Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin.

0 : Disable ADC4, P64 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0 : Disable ADC3, P63 functions as I/O pin

1 : Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0 : Disable ADC2, P62 functions as I/O pin

1 : Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 : Disable ADC1, P61 functions as I/O pin

1 : Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0 : Disable ADC0, P60 functions as I/O pin

1 : Enable ADC0 to function as analog input pin

6.7.1.2 Bank 2 R6 ADCON (A/D Control Register)

The ADCON register controls the operation of the A/D conversion and determines which pin should be currently active.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): ADC's Vref input source

0 : ADC's Vref is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1 : ADC's Vref is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of oscillator clock rate of ADC

00 = 1: 4 (default value)

01 = 1: 1

10 = 1: 16

11 = 1: 2

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
01	F_{OSC}	1 MHz
10	$F_{OSC}/16$	16 MHz
11	$F_{OSC}/2$	2 MHz

Bit 4 (ADRUN): ADC starts to run

0 : reset on completion of the conversion. This bit cannot be reset by software.

1 : an A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : switch off the resistor reference to save power even while the CPU is operating

1 : ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = AN6/P66

111 = AN7/P67

They can only be changed when the ADIF bit and the ADRUN bit are both Low.

6.7.1.3 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-

Bit 7 (CALI): Calibration enable bit for A/D offset

0 : disable Calibration

1 : enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 : Negative voltage

1 : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

Bits 2 ~ 0: Not used, set to "0" at all time

6.7.2 ADC Data Buffer (ADDH, ADDL/R8, R9)

When the A/D conversion is completed, the result is loaded to the ADDH, ADDL. The ADRUN bit is cleared, and the ADIF is set.

6.7.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before conversion can be started.

6.7.4 A/D Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at a maximum frequency without sacrificing the AD conversion accuracy. For the EM78F564N, the conversion time per bit is 1μs. Table 6-8-4-1 shows the relationship between Tct and the maximum operating frequencies.

Table 6-8-4-1 Tct vs. Maximum Operation Frequency

CKR1: CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/4	4 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
01	Fosc	1 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
10	Fosc/16	16 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)
11	Fosc/2	2 MHz	1 MHz (1 μs)	16×1 μs = 16 μs (62.5kHz)

NOTE

The pin not used as an analog input can be used as regular input or output pin. During conversion, do not perform output instruction to maintain precision for all the pins.

6.7.5 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during sleep mode. **As the SLEP instruction is executed, all MCU operations will stop except for the Oscillator, TCC, TC1, TC2, TC3, Timer A, Timer B and A/D conversion.**

The AD Conversion is considered completed when:

1 ADRUN Bit of R6 Register Is Cleared to “0”.

2 Wake-up from A/D Conversion Remains in Operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of the ADPD bit is.

6.7.6 Programming Steps/Considerations

6.7.6.1 Programming Steps

Follow these steps to obtain data from the ADC**:**

1. Write to the four bits (ADE7~ADE0) on the R5 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R6/ADCON register to configure the AD module**:**
   a) Select AD input channel (ADIS2 : ADIS0)
   b) Define the AD conversion clock rate (CKR1 ~ CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed

6. Set the ADRUN bit to 1
7. Wait for wake-up or for ADRUN bit to be cleared to “0”
8. Read the ADDATAH and ADDATAL conversion data registers.
9. Clear the interrupt flag bit (ADIF) when A/D interrupt function has occurred.
10. For the next conversion, go to Step 1 or Step 2 as required. At least two TCT’s are required before the next acquisition starts.

NOTE

To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.7.6.2 Demonstration Programs

```
; To define the general registers
R_0 == 0                    ; Indirect addressing register
PSW == 3                    ; Status register
PORT5 == 5
PORT6 == 6
RA== 0XA                    ; Wake-up control register
RF== 0XF                    ; Interrupt status register

; To define the control register
IOC50 == 0X5                ; Control Register of Port 5
IOC60 == 0X6                ; Control Register of Port 6
C_INT == 0XF                ; Interrupt Control Register

;ADC Control Registers
ADDATAH == 0x8              ; The contents are the results of ADC
ADDATAL == 0x9              ; The contents are the results of ADC
AISR == 0x05                ; ADC input select register
ADCON == 0x6                ; 7    6    5    4    3   2   1    0
                            (VREFS)(CKR1:0)(ADRUN)(ADPD)(ADIS2:0)
ADOC == 0x07                ; ADC offset calibration register

;To define bits
;In ADCON
ADRUN == 0x4                ; ADC is executed as the bit is set
ADPD == 0x3                 ; Power Mode of ADC
```

```
ORG 0                       ; Initial address
JMP INITIAL
ORG 0x30                    ; Interrupt vector

(User's program)            ; Determined by User

BANK      0
CLR RF                      ; To clear the ADIF bit
BANK      2
BS ADCON  , ADRUN           ; To start to execute the next AD
                            ; conversion if necessary
RETI

INITIAL:
BANK       2
MOV A      , @0B00000001    ; To define P60 as an analog input
MOV AISR   , A
MOV A      , @0B00001000    ; To select P60 as an analog input
                            ; channel, and AD power on
MOV ADCON  , A              ; To define P60 as an input pin and
                            ; set clock rate at fosc/4
MOV A      , @0B00000000
MOV ADOC   , A              ; To disable calibration

En_ADC:
MOV A      , @0BXXXXXXX1    ; To define P60 as an input pin, and
                            ; the others are dependent
IOW PORT6                   ; on applications
BANK       0
MOV A      , @0BXX1XXXXX    ; Enable the ADWE wake-up function
                            ; of ADC, "X" by application
MOV RA     , A
MOV A      , @0BX1XXXXXX    ; Enable the ADIE interrupt function
                            ; of ADC, "X" by application
IOW C_INT

ENI                         ; Enable the interrupt function
BANK       2
BS ADCON   , ADRUN          ; Start to run the ADC
                            ; If the interrupt function is
                            ; employed, the following three
                            ; lines may be ignored
SLEP                        ; Into sleep mode
POLLING:
JBC ADCON  , ADRUN          ; To check the ADRUN bit
                            ; continuously
 JMP POLLING                ; ADRUN bit will be reset as the AD
                            ; conversion is completed
(User's program)            ; Read AD convert data from ADDATAH/L
```

6.8 Dual Set of PWM (Pulse Width Modulation)

6.8.1 Overview

In PWM mode, PWMA and PWMB pins produce up to a 10-bit resolution PWM output (see Figure 6-20 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output in high. The baud rate of the PWM is the inverse of the period. Figure 6-21 depicts the relationships between a period and a duty cycle.

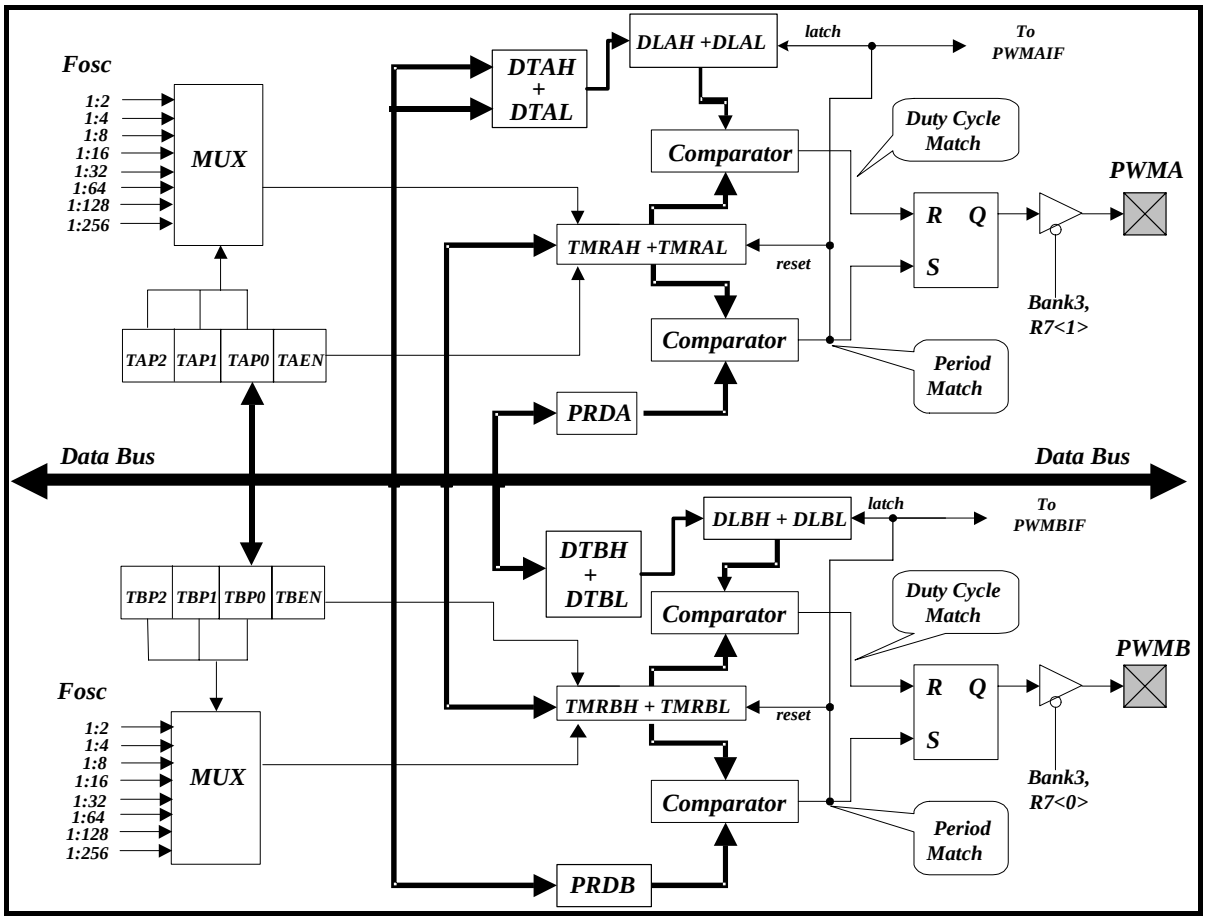


Figure 6-20 Functional Block Diagram of the two PWMs

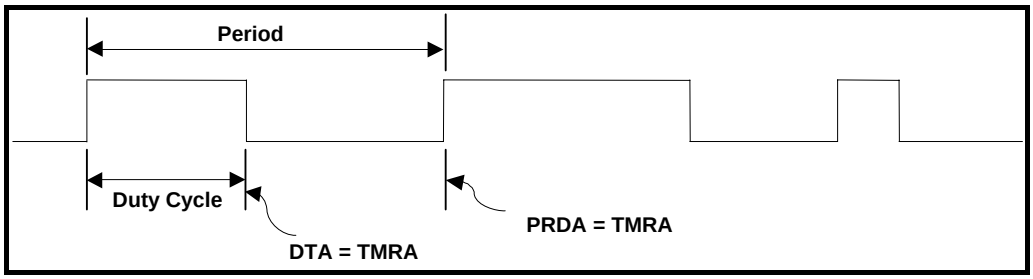


Figure 6-21 PWM Output Timing

6.8.2 Increment Timer Counter (TMRX: TMRAH/L or TMRBH/L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, they can be turned down for power conservation, by setting TAEN Bit [R5<7> Bank 3] or TBEN Bit [R5<3> Bank 3] to 0.

6.8.3 PWM Period (PRDX : PRDA or PRDB)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

(1) TMRX is cleared.

(2) The PWMX pin is set to 1.

(3) The PWM duty cycle is latched from DTA/DTB to DLA/DLB.

NOTE

The PWM output will not be set, if the duty cycle is 0.

(4) The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM Time Period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \ prescaler\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz TMRX (0, 0, 0) = 1 : 2,

Then

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 2 = 25\,\mu s$$

6.8.4 PWM Duty Cycle (DTX: DTA or DTB)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 2,

Then

$$Duty\ cycle\ =\ (10)\times\left(\frac{1}{4M}\right)\times 2\ =\ 5\,\mu s$$

6.8.5 Comparator X

Changing the output status while a match occurs will simultaneously set the PWMXIF flag.

6.8.6 PWM Programming Procedures/Steps

(1) Load PRDX with the PWM period.

(2) Load DTX with the PWM Duty Cycle.

(3) Enable the interrupt function by writing IOCF, if required.

(4) Set PWMX pin to be output by writing a desired value to Bank 3 R7.

(5) Load a desired value to Bank 3 R5 with the TMRX prescaler value, and enable both PWMX and TMRX.

6.8.7 Timer Mode

6.8.7.1 Overview

Timer X: Timer A (TMRA) and Timer B (TMRB) are 10-bit clock counters with programmable prescalers, respectively. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. Timer A and Timer B stopped running when sleep mode occurs, with A/D Conversion not running. However, if A/D conversion is running when sleep mode occurs, Timer A and Timer B will keep on running.

6.8.7.2 Functional Description

Figure 6-22 shows the TMRX block diagram. Each signal and blocks are described as follows:

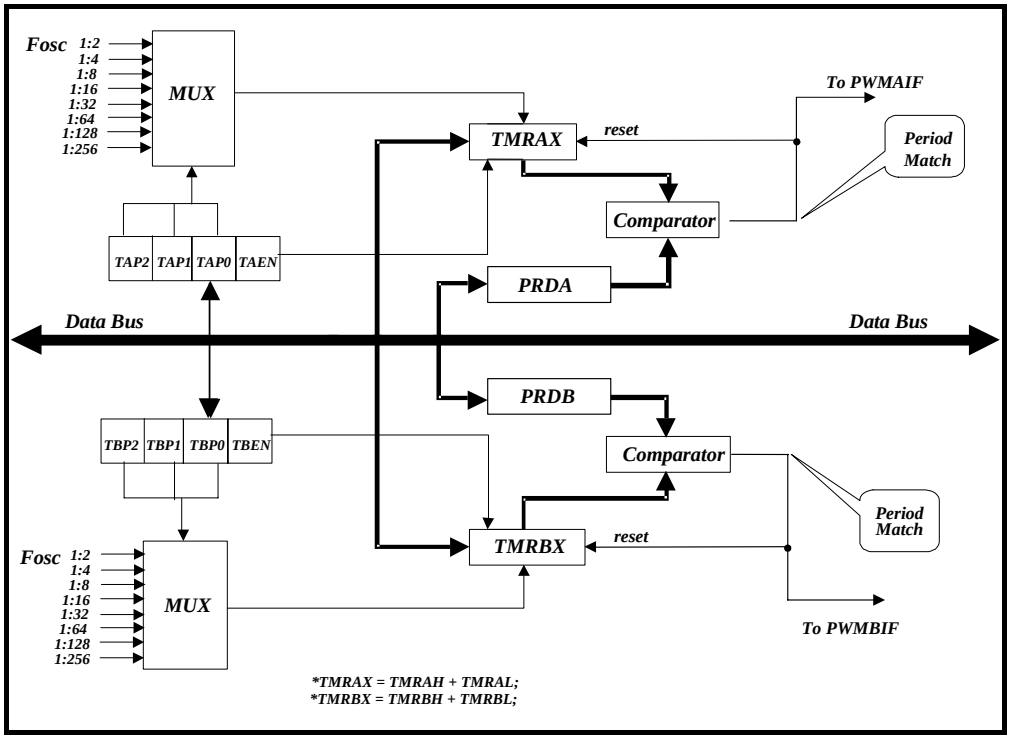


Figure 6-22 TMRX Block Diagram

Fosc: Internal clock

Prescaler (TAP2, TAP1 and TAP0 / TBP2, TBP1 and TBP0): Options of 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256 are defined by TMRX. It is cleared when any type of reset occurs.

TMRAX and TMRBX (TMRAH/TMRAL and TMRBH/TMRBL: Timer X register; TMRX is incremented until it matches with PRDX, and then is reset to **1 (default valve)**.

PRDX (PRDA and PRDB): PWM time period register.

Comparator X (Comparator A and Comparator B):

Reset TMRX while a match occurs. The PWMXIF flag is set at the same time.

6.8.7.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers, as shown in the Table 6.9.7-1 below. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 1: Bit 0 of Bank 3 R7 register must be set to '0'.

Table 6-8-7-1 Related Control Registers of TMRA and TMRB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R5 Bank 3	Timer A and Timer B Control Register	TAEN	TAP2	TAP1	TAP0	TBEN	TBP2	TBP1	TBP0

6.8.7.4 Timer Programming Procedures/Steps

(1) Load PRDX with the Timer period.

(2) Enable interrupt function by writing to IOCF, if required.

(3) Load a desired value to PWMCON and TMRCON with the TMRX prescaler value and enable TMRX and disable PWMX.

6.9 Timer/Counter 1

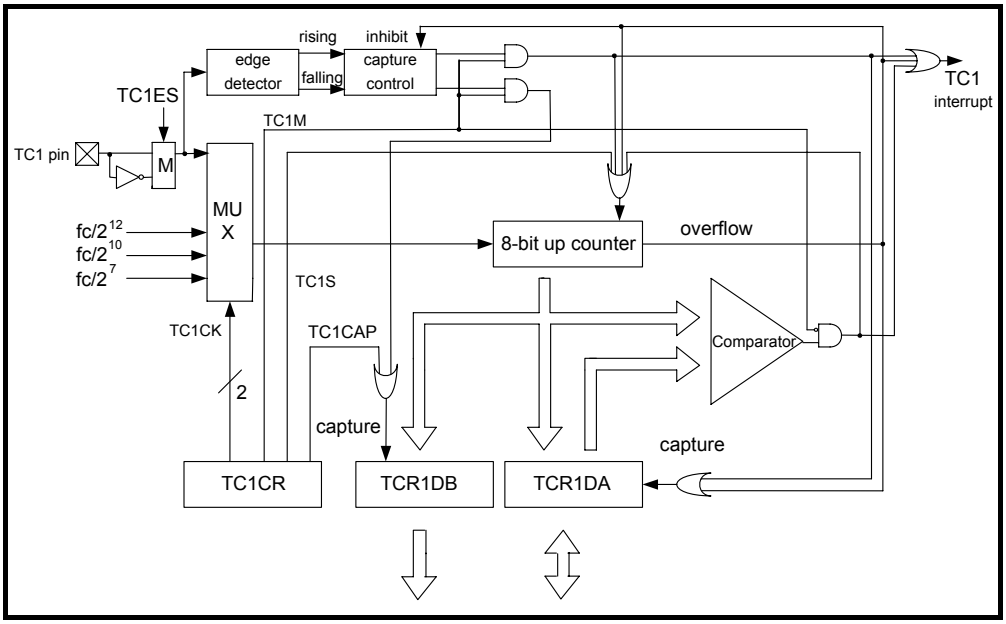


Figure 6-23 Configuration of Timer/Counter 1

In Timer mode, counting up is performed using an internal clock. When the contents of the up-counter matched the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to "1" and the TC1CAP is automatically cleared to "0" after capture.

In Counter mode, counting up is performed using an external clock input pin (TC1) and either rising or falling edge can be selected by TC1ES but **both edges cannot be used**. When the contents of the up-counter matched the TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to "1" and the TC1CAP is automatically cleared to "0" after capture.

In Capture mode, the pulse width, period and duty of the TC1 input pin are measured in this mode, which can be used to decode the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TC1 pin input, the contents of counter is loaded into TCR1DA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of TC1 pin input, the contents of the counter are loaded into TCR1DB. The counter is still counting, on the next rising edge of TC1 pin input, the contents of the counter are loaded into TCR1DA, the counter is cleared and interrupt is generated again. If an overflow before the edge is detected, the FFH is loaded into TCR1DA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detection) is generated, capture and overflow detection are halted until TCR1DA is read out.

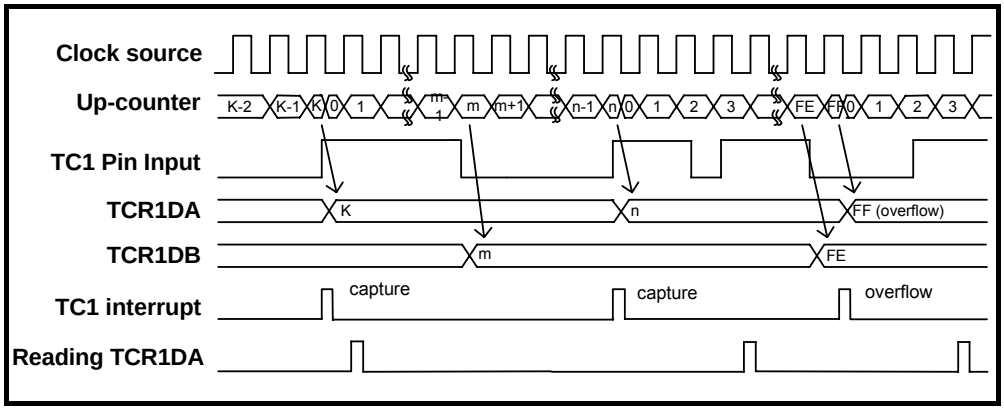


Figure 6-24 Capture Mode Timing Chart

6.10 Timer/Counter 2

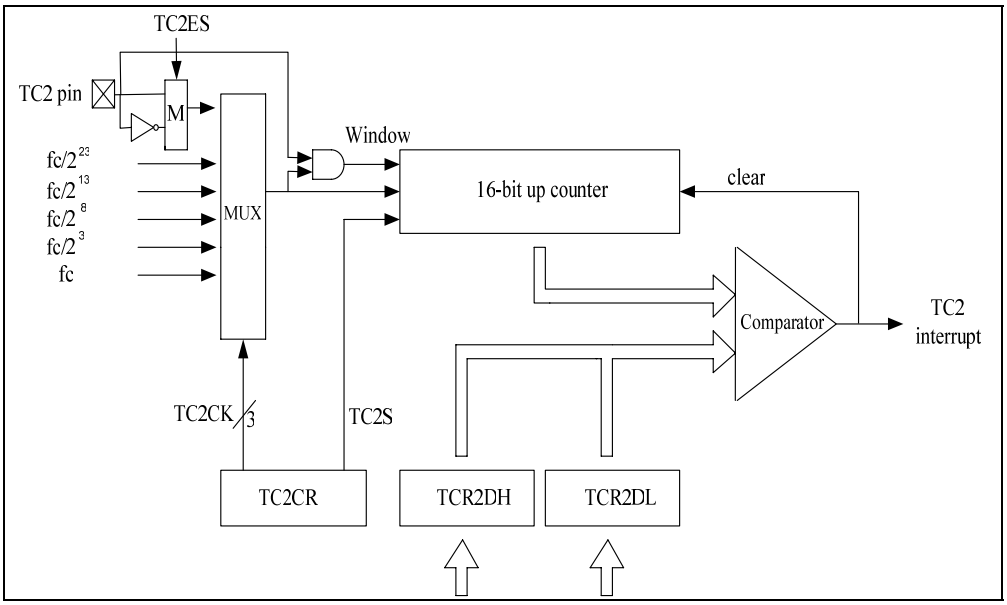


Figure 6-25 Configuration of Timer/Counter 2

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

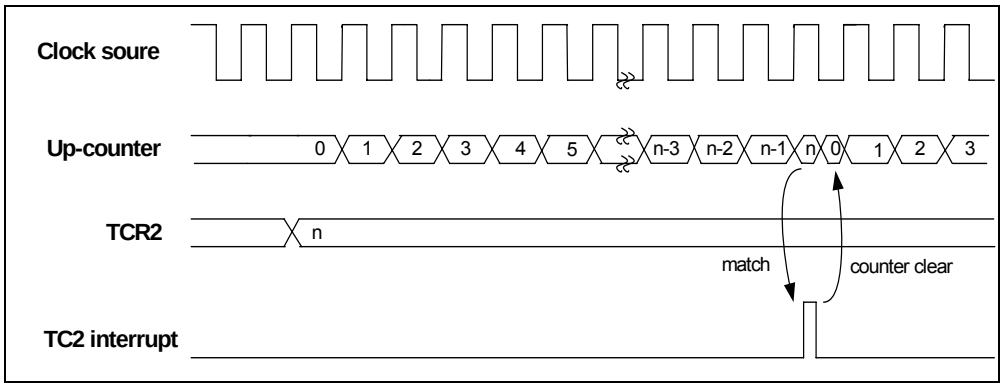


Figure 6-26 Timer Mode Timing Chart

In Counter mode, counting up is performed using an external clock input pin (TC2) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter matched, the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

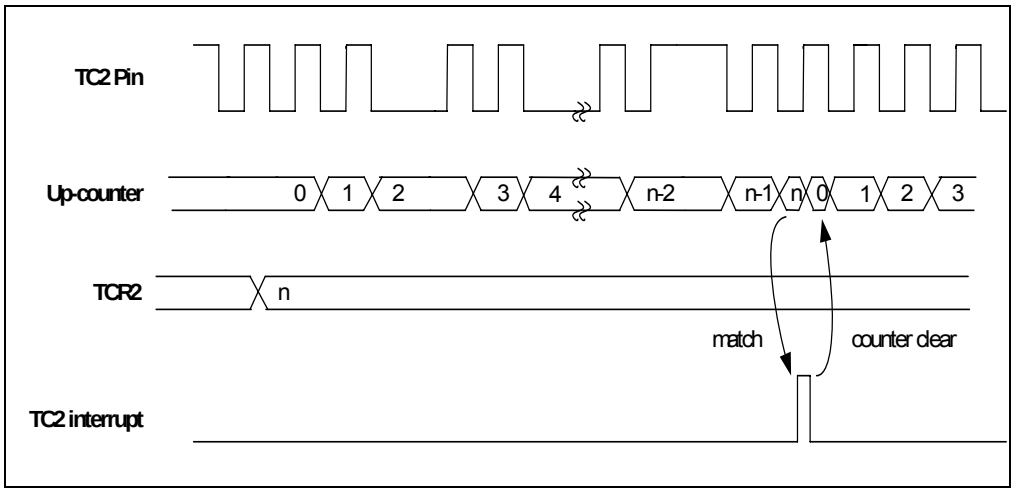


Figure 6-27 Counter Mode Timing Chart

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter matched with the TCR2 (TCR2DH+TCR2DL), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

While writing to the TCR2DL, the comparison is inhibited until TCR2DH is written.

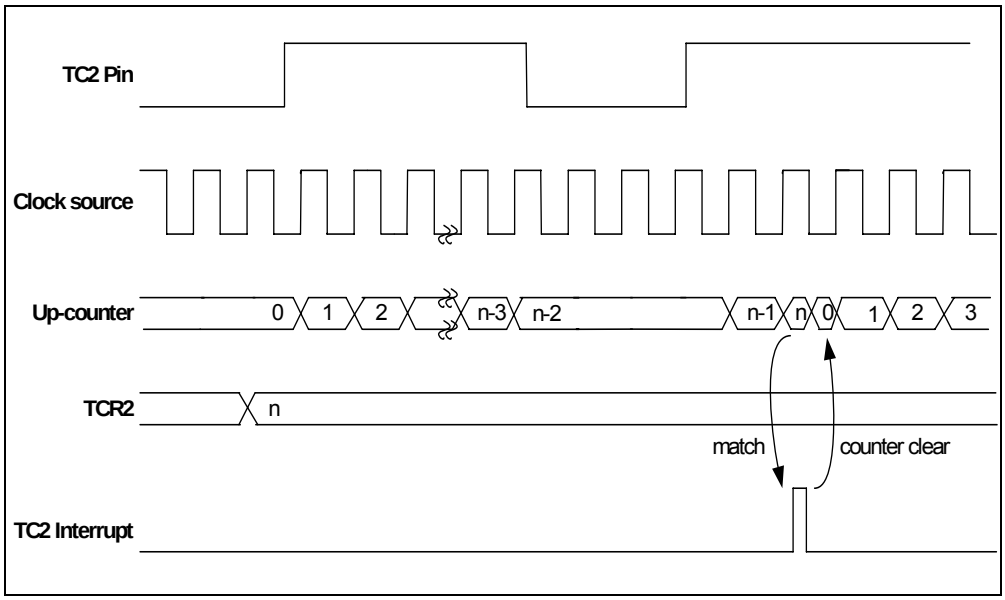


Figure 6-28 Window Mode Timing Chart

6.11 Timer/Counter 3

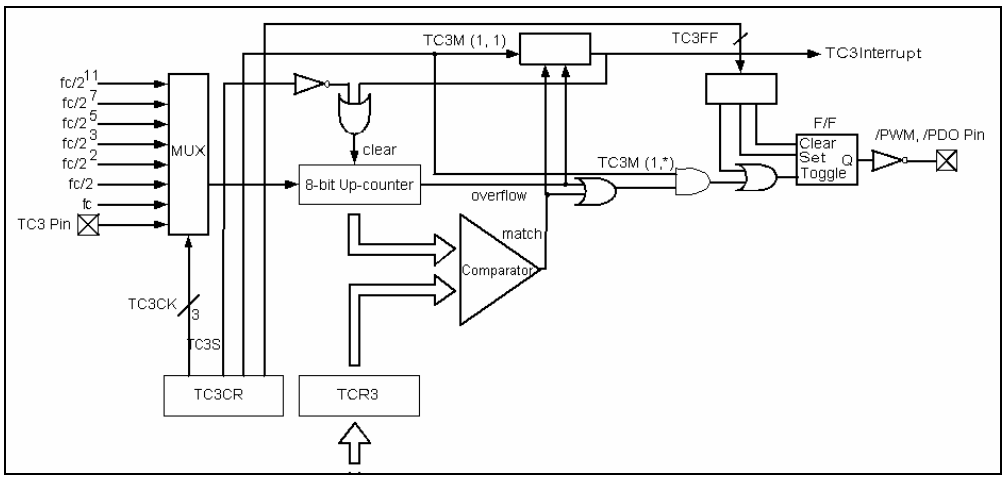


Figure 6-29 Timer/Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3). When the contents of the up-counter matched with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

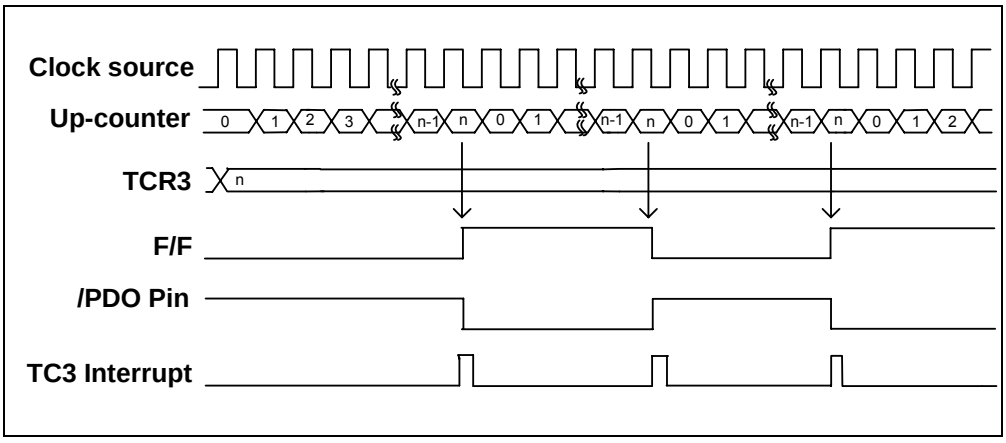


Figure 6-30 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, the first time, TCR3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

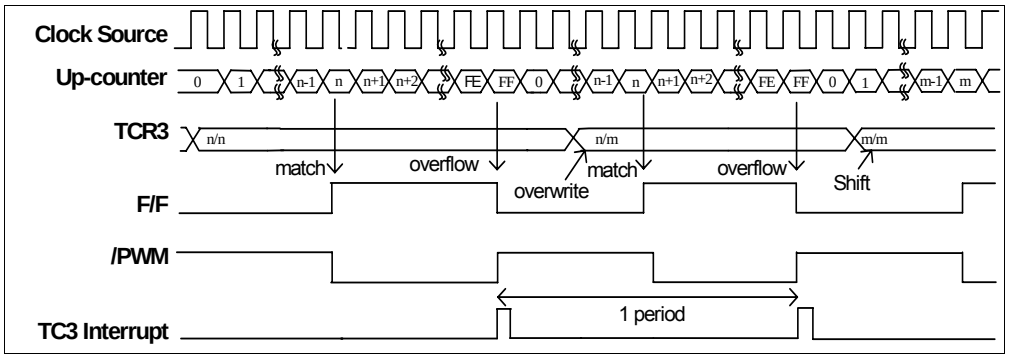


Figure 6-31 PWM Mode Timing Chart

6.12 Comparator

The EM78F564N has two comparators, which has two analog inputs and one output. The comparator can be employed to wake-up from sleep mode. Figure 6-32 shows the comparator circuit.

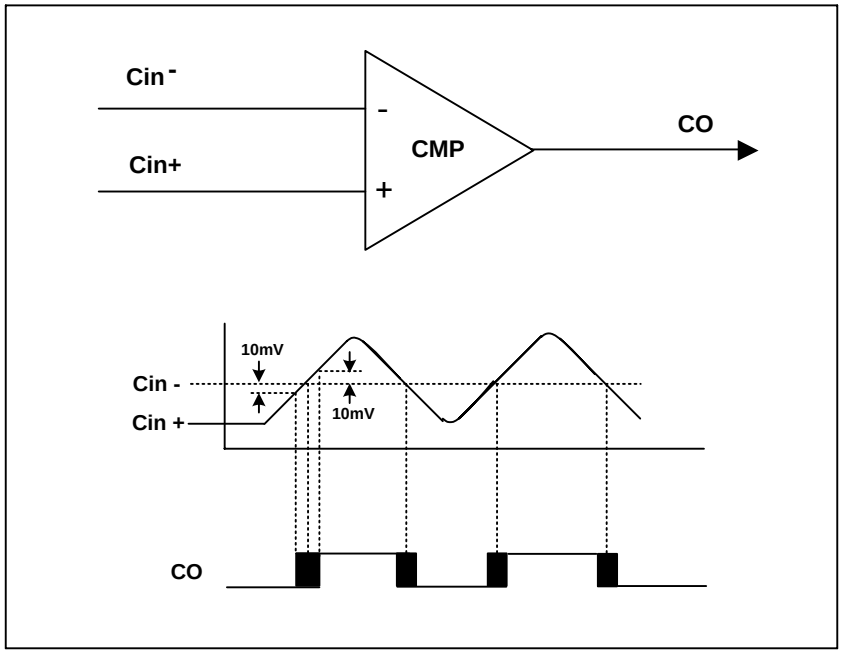


Figure 6-32 Comparator Operating Mode

6.12.1 External Reference Signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

6.12.2 Comparator Outputs

- The compared result is stored in the CPOUT2 of R7 Bit 4 of Bank 3.
- The comparator is output to CO2 (P80) by programming Bit 3, Bit 2 <COS21, COS20> of Register R7 Bank 3.
- Figure 6-33 shows the comparator output block diagram.

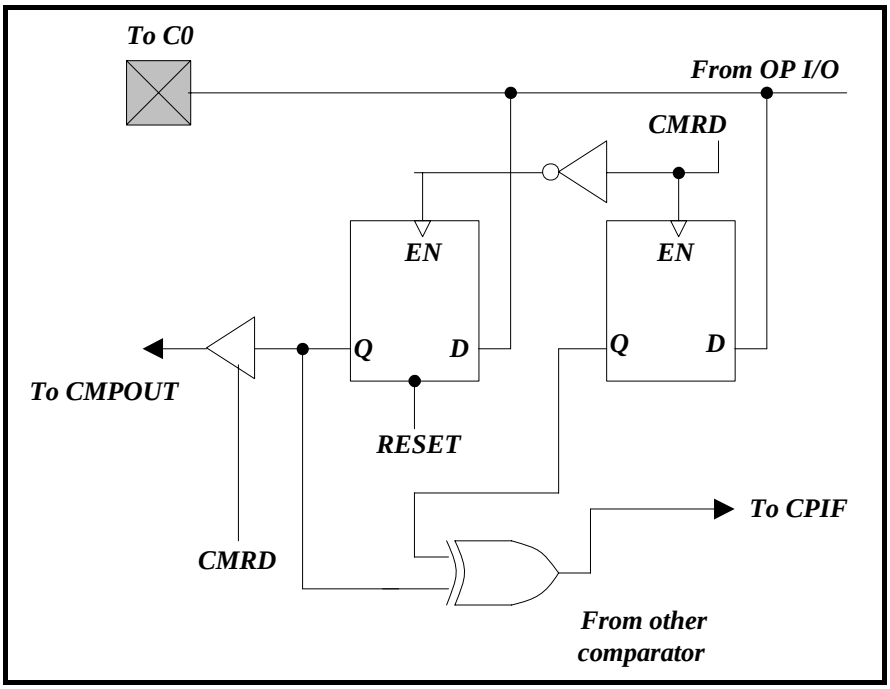


Figure 6-33 Comparator Output Configuration

6.12.3 Interrupt

- CMP2IE (IOCE.7) and the “ENI” instruction execution must be enabled.
- Interrupt occurs whenever a change occurs on the output pin of the comparator.
- The actual change on the pin can be determined by reading the Bit CPOUT2, R7 Bit 4 of Bank 3.
- CMP2IF (RF.7 Bank 1), the comparator interrupt flag, can only be cleared by software.

6.12.4 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake-up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.13 UART

UART is a communication protocol, the control setup are shown in the following:

6.13.1 Bank 2 RA URC1 (UART Control 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (URTD8): Transmission data Bit 8.

Bits 6 ~ 5 (UMODE1 ~ UMODE0): UART mode.

UMODE1	UMODE0	UART Mode
0	0	Mode 1: 7-bit
0	1	Mode 1: 8-bit
1	0	Mode 1: 9-bit
1	1	Reserved

Bits 4 ~ 2 (BRATE2 ~ BRATE0): Transmit Baud rate select.

BRATE2	BRATE1	BRATE0	Baud Rate	4 MHz	8 MHz
0	0	0	Fc/13	19200	38400
0	0	1	Fc/26	9600	19200
0	1	0	Fc/52	4800	9600
0	1	1	Fc/104	2400	4800
1	0	0	Fc/208	1200	2400
1	0	1	Fc/416	600	1200
1	1	0	TC3	–	–
1	1	1	Reserved		

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when writing into the URTD register. UTBE bit will be cleared by hardware when enabling transmission. UTBE bit is read only. Hence, writing to the URTD register is necessary when user wants to start transmit shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.13.2 Bank 2 RB URC2 (UART Control 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBIM1	SBIM0	UINVEN	-	-	-

Bits 7 ~ 6: Not used, set to ”0” at all time

Bit 5 ~ Bit 4 (SBIM1 ~ SBIM0): Serial bus interface operating mode select.

SBIM1	SBIM0	Operating Mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	Reserved

Bit 3 (UNIVEN): Enable UART TXD and RXD port inverse output.

0 : Disable **TXD** and **RXD** port inverse output.

1 : Enable **TXD** and **RXD** port inverse output.

Bits 2 ~ 0: Not used, set to ”0” at all time

6.13.3 Bank 2 RC URS (UART Status)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URRD8): Receiving data Bit 8

Bit 6 (EVEN): Select parity check

0 : Odd parity

1 : Even parity

Bit 5 (PRE): Enable parity addition

0 : Disable

1 : Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error occurs.

Bit 3 (OVERR): Overrun error flag. Set to 1 when overrun error occurs.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error occurs.

NOTE

The Interrupt flag is automatically set by hardware. It must be cleared by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URS and URRD register. **URBF** will be cleared by hardware when enabling receiving. The **URBF** bit is read only. Hence, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0 : Disable

1 : Enable

6.13.4 Bank 2 RD URRD (UART_RD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7 ~ 0 (URRD7 ~ URRD0): UART receive data buffer. **Read only.**

6.13.5 Bank 2 RE URTD (UART_TD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7 ~ 0 (URTD7 ~ URTD0): UART transmit data buffer. **Write only.**

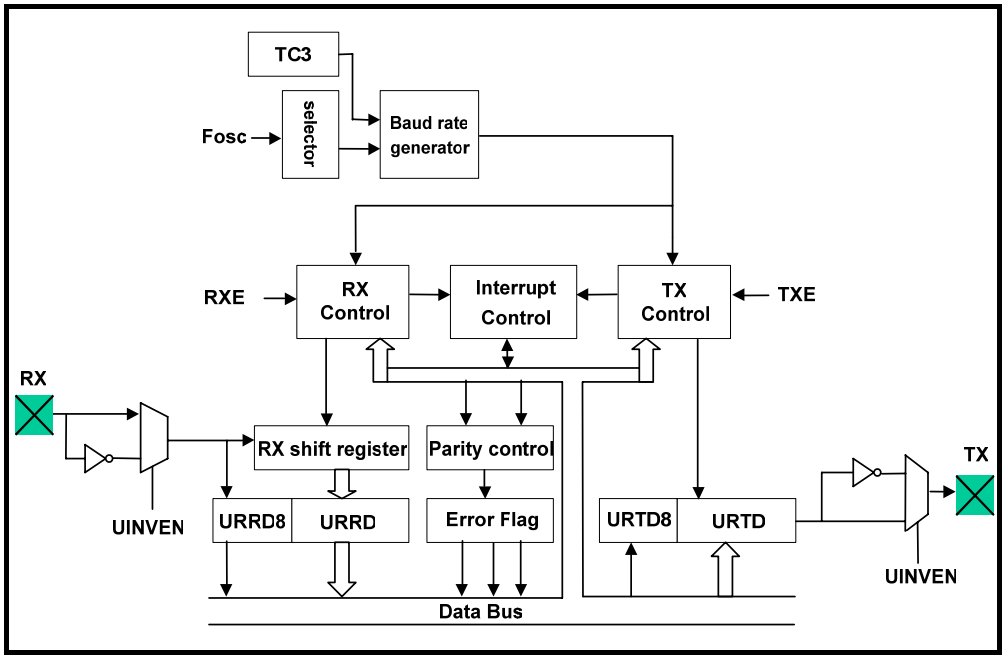


Figure 6-34 UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and a stop bit.

Full duplex data transfer is possible because the UART has independent transmit and receive sections. Double buffering in both sections enable the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the mark state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

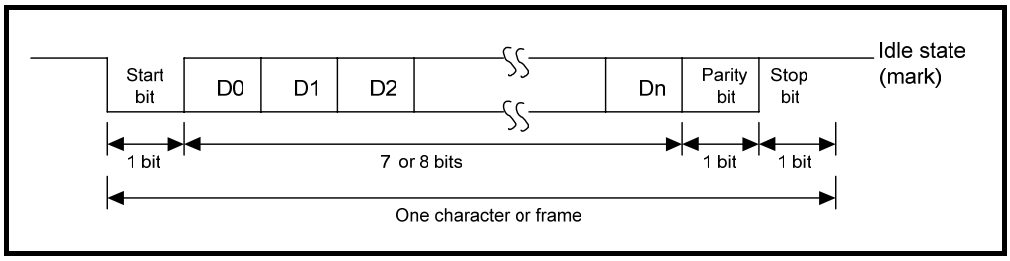


Figure 6-35 Data Format in UART

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

6.13.6 UART Mode

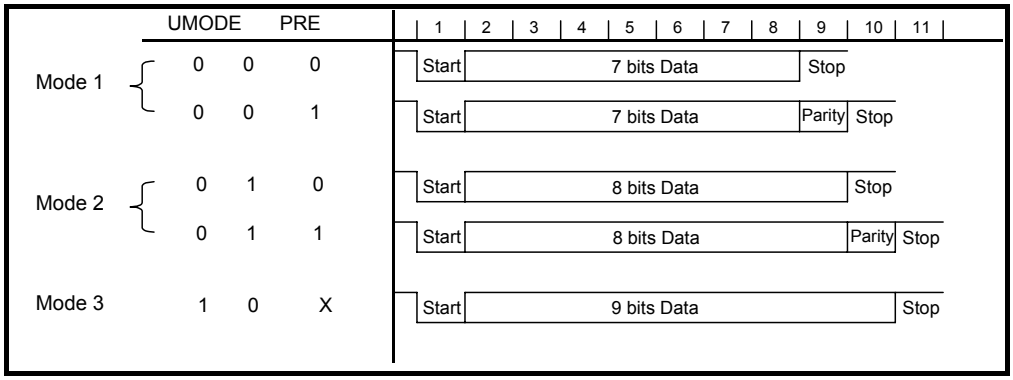


Figure 6-36 UART Mode

There are three modes in UART. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-36 shows the data format in each mode.

6.13.7 Transmission

In transmitting serial data, the UART operates as follows.

1. Set the **TXE** bit of URC1 register to enable UART transmission function.
2. Write data into the URTD register and the **UTBE** bit of URC1 register will be set by hardware. Then start transmitting.

3. Serial transmit data are transmitted in the following order from the TX pin.
   (a) Start bit: one “0” bit is output.
   (b) Transmit data: 7, 8 or 9 bits data are output from LSB to MSB.
   (c) Parity bit: one parity bit (odd or even selectable) is output.
   (d) Stop bit: one “1” bit (stop bit) is output.
   (e) Mark state: output “1” continues until the start bit of the next transmit data.
4. After transmitting the stop bit, the UART generates a **TBEF** interrupt (if enabled)

6.13.8 Receiving

In receiving, the UART operates as follows.

1. Set the **RXE** bit of the URS register to enable the UART receiving function.

   The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received.

   After one character is received, the UART generates an **RBFF** interrupt (if enabled). The **URBF** bit of the URS register will be set to 1.
4. The UART makes the following checks:
   (a) Parity check: The number of 1 in the receive data must match the even or odd parity setting of the **EVEN** bit in the URS register.
   (b) Frame check: The start bit must be 0 and the stop bit must be 1.
   (c) Overrun check: **URBF** bit of the URS register must be cleared (this means that the URRD register should be read out) before the next received data is loaded into the URRD register.

If any checks failed, the UERRIF interrupt will be generated (if enabled). The error flag is indicated in **PRERR, OVERR** or **FMERR** bit. The error flag should be cleared by software, else the UERRIF interrupt will occur during the next byte received.

5. Read received data from the URRD register. The **URBF** bit will be cleared by hardware.

6.13.9 Baud Rate Generator

The baud rate generator comprises of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The **BRATE2~BRATE0** bit of the URC1 register can determine the desired baud rate.

Note:

1. Priority of P52/RX/SI pin

P52/RX/SI Pin Priority		
High	Medium	Low
SI	RX	P52

2. Priority of P51/TX/SO pin

P51/TX/SO Pin Priority		
High	Medium	Low
SO	TX	P51

6.14 SPI

6.14.1 Overview and Features

Overview:

Figures 6-37, 6-38 and 6-39 show how the EM78F564N communicates with other devices through the SPI module. If EM78F564N is a master controller, it sends clock pulses through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78F564N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. User can also set the SPIS Bit 7 (DORD) to determine the SPI transmission order, SPIC Bit 3 (SDOC) to control the SO pin after serial data output status and SPIS Bit 6 (TD1), Bit 5 (TD0) determine the SO status output delay times.

Features:

- Operation in either Master mode or Slave mode
- 3-wire or 4-wire full duplex synchronous communication
- Programmable baud rates of communication
- Programming clock polarity, (Bank 1 0x0C CES bit)
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SO status select
- SO status output delay times
- SPI handshake pin
- Up to 8 MHz (maximum) bit frequency

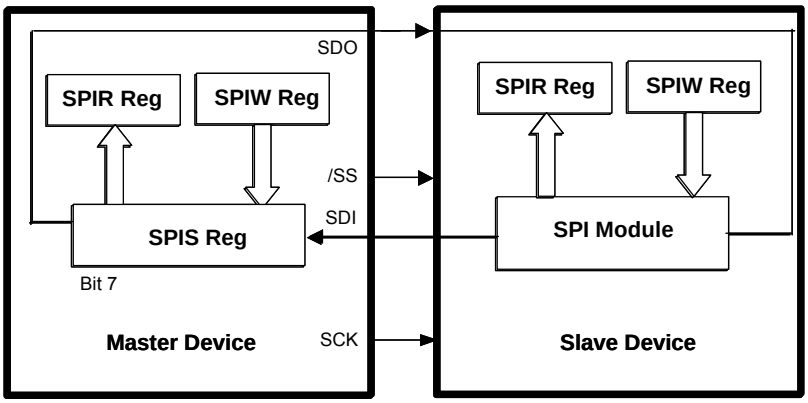


Figure 6-37 SPI Master/Slave Communication

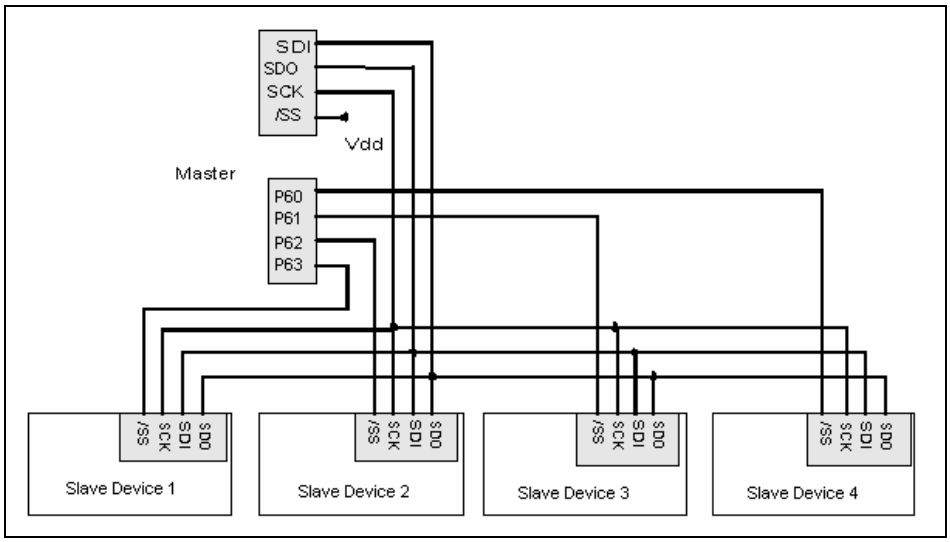


Figure 6-38 SPI Configuration of a Single-Master and Multi-Slave Device

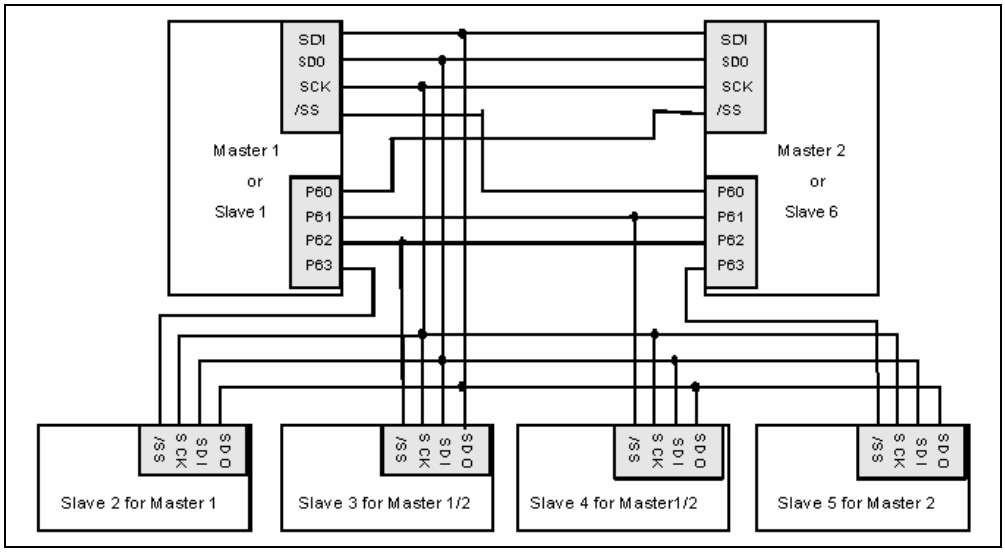


Figure 6-39 SPI Configuration of a Single-Master and Multi-Slave Device

6.14.2 SPI Function Description

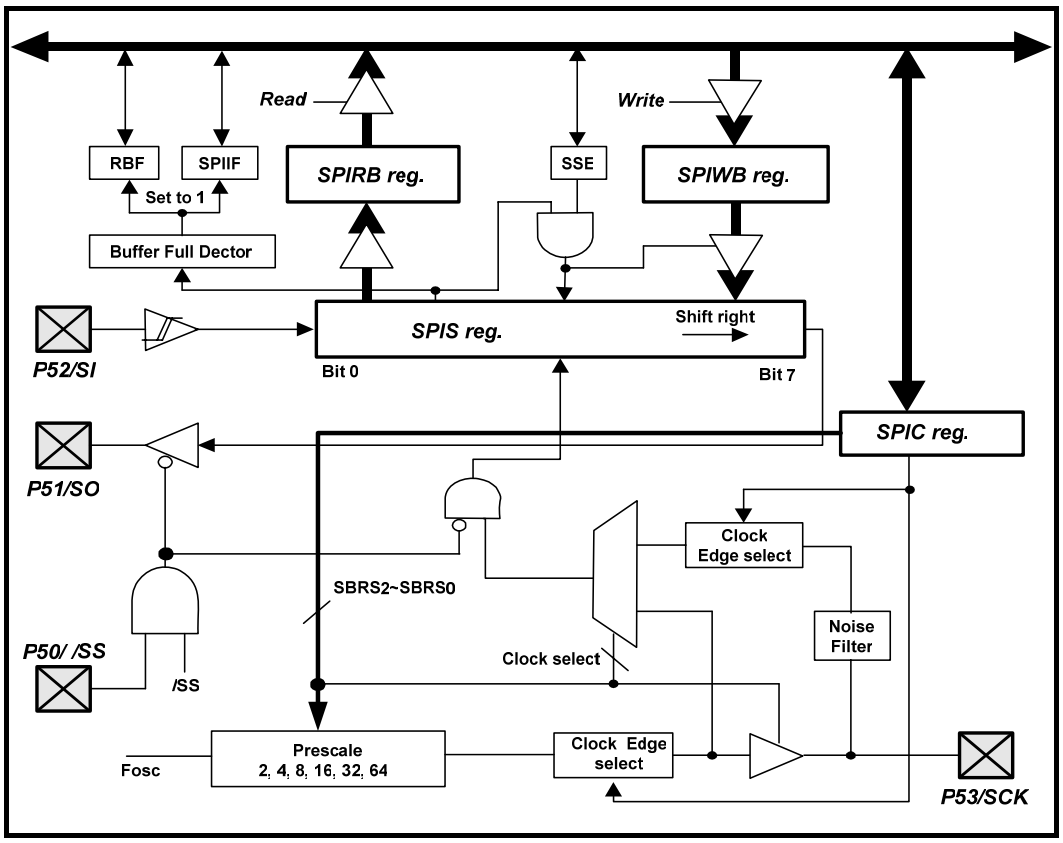


Figure 6-40 SPI Block Diagram

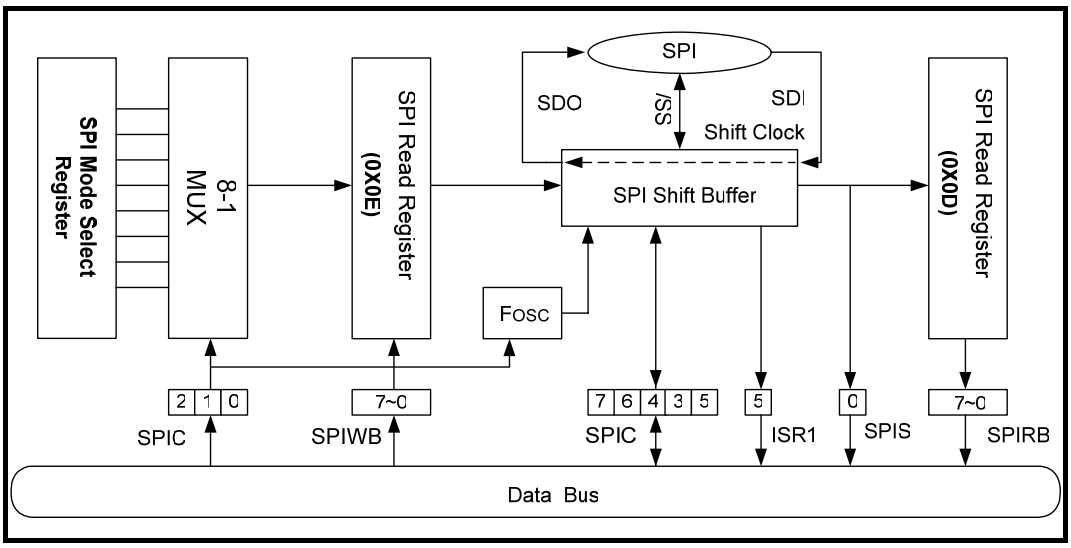


Fig 6-41 Functional Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Figure 6-40 and Figure 6-41.

- P52 / SI : Serial Data In
- P51 / SO : Serial Data Out
- P53 / SCK : Serial Clock
- P50 / /SS : /Slave Select (Option). This pin (/SS) may be required in slave mode
- RBF: Set by Buffer Full Detector, and reset by hardware.
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed
- SSE: Loads the data in the SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIS and the SPIWB registers are loaded at the same time. Once data are written, the SPIS starts transmission/reception. The data received are moved to the SPIRB register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIIF (Read Buffer Full Interrupt) flags are then set.
- SPIRB reg : Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIRB register reads.
- SPIWB reg.: Write buffer. The buffer will ignore any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“ if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0 : Program the clock frequency/rates and sources
- Clock Select : Select either internal or external clock as the shifting clock
- Edge Select : Select the appropriate clock edges by programming the CES bit

6.14.3 SPI Signal and Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Figure 6-40, are as follows:

SI/P52

- Serial Data In
- Receive sequentially the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Defined as high-impedance, if not selected

- Program the same clock rate and clock edge to latch on both the master and slave devices
- The byte received will update the transmitted byte
- Both the RBF and SPIIF bits (located in Register 0x0B in Bank 1 and 0x0F in Bank 0) will be set as the SPI operation is completed.
- Timing is shown in Figures 6-42 and 6-43.

SO/P51

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- The SSE (located in Register 0x0C) bit will be reset, as the SPI operation is completed
- Timing is shown in Figures 6-42 and 6-43.

SCK/P53

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins
- The CES (located in Register 0x0C) is used to select the edge to communicate
- The SBRS2~SBRS0 (located in Register 0x0C) is used to determine the baud rate of communication
- The CES, SBRS2, SBRS1, and SBRS0 bits have no effect in slave mode
- Timing is shown in Figure 6-42 and 6-43

/SS/P50

- Slave Select : negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last 8^{th} cycle is completed
- Ignores the data on the SDI and SDO pins while /SS is high, since the SDO is no longer driven
- Timing is shown in Figure 6-42 and 6-43

6.14.4 Programming the Related Registers

As the SPI mode is defined, the related registers are shown in Table 6.15.4-1 and Table 6.15.4-2.

Table 6.14.4-1 Related Control Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1 0x0C	*SPIC/RC	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
0x0F	IOCF	–	ADIE	SPIIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

***SPIC:** SPI control register

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.

1 : Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only transmission is implemented.

- This can occur only in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 : Reset as soon as the shifting is complete, and the next byte is ready to shift

1 : Start to shift, and keep on “1” while the current byte is still being transmitted

- This bit will reset to 0 at every 1-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit

0 : After the Serial data output, the SDO remains high

1 : After the Serial data output, the SDO remains low

Bit 2 ~ Bit 0 (SBRS2 ~ SBRS0): SPI Baud Rate Select bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

IOCF: Interrupt Mask Register

Bit 7: Not used, set to “0” at all time.

Bit 6 (ADIE): ADIF interrupt enable bit.

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC Complete status is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to “Enable“.

Bit 5 (SPIIE): SPIIF interrupt enable bit

0 : Disable SPIIF interrupt

1 : Enable SPIIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit

0 : Disable PWMBIF interrupt

1 : Enable PWMBIF interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit

0 : Disable PWMAIF interrupt

1 : Enable PWMAIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

Table 6-14-4-2 Related Status/Data Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1 0×0B	SPIS/RB	DORD	TD1	TD0	-	OD3	OD4	-	RBF
Bank 1 0×0D	SPIRB/RD	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
Bank 1 0×0E	SPIWB/RE	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

SPIS: SPI Status register

Bit 7 (DORD): Read Buffer Full Interrupt flag

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6~Bit 5 (TD1 ~ TD0): SDO Status Output Delay Times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” at all time

Bit 3 (OD3): Open-drain Control bit (P51)

0 : SO open-drain disable

1 : SO open-drain enable

Bit 2 (OD4): Open drain-Control bit (P53)

0 : SCK open-drain disable

1 : SCK open-drain enable

Bit 1: Not used, set to “0” at all time

Bit 0 (RBF): Read Buffer Full flag

0 : Receiving is ongoing, SPIB is empty

1 : Receiving is completed, SPIB is full

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPISR. The RBF bit and the SPIIF bit in the SPIS register will also be set.

SPIWB: SPI Write Buffer. As a transmitted data is loaded, the SPIS register stands by and starts to shift the data when sensing an SCK edge with SSE set to “1”.

6.14.5 SPI Mode Timing

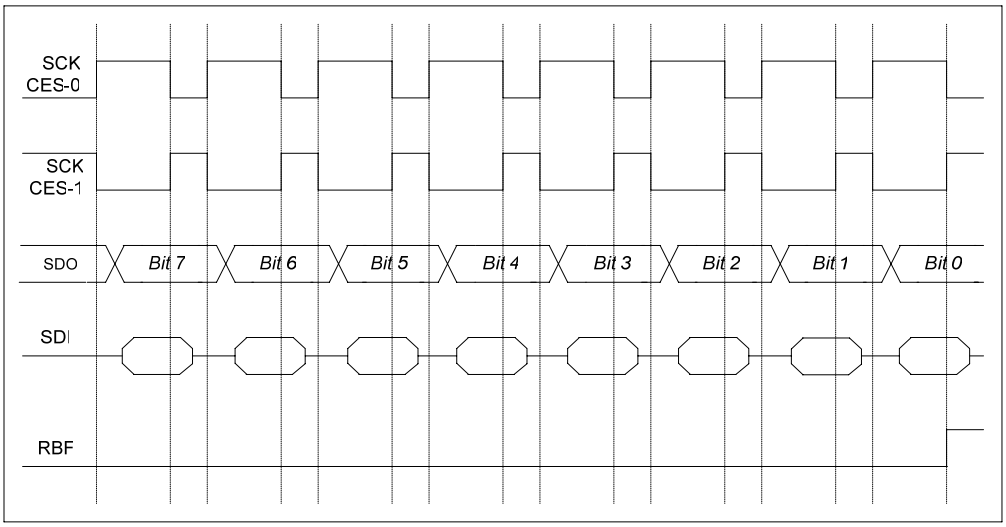


Figure 6-42 SPI Mode with /SS Disable

The SCK edge is selected by programming bit CES. The waveform shown in Figure 6-42 is applicable regardless whether the EM78F564N is in master or slave mode, with /SS disabled. However, the waveform in Figure 6-43 can only be implemented in slave mode, with /SS enabled.

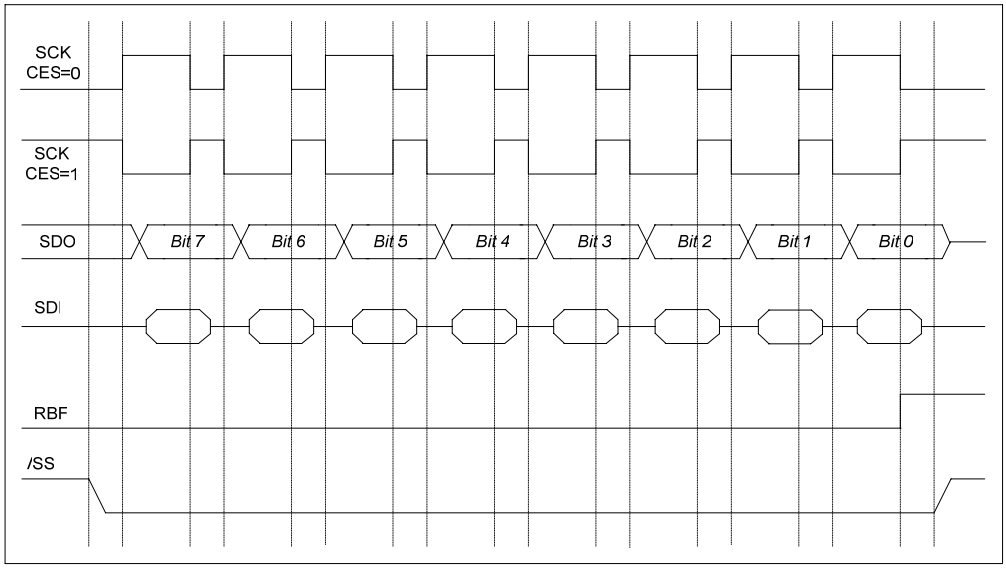


Figure 6-43 SPI Mode with /SS Enable

6.14.6 SPI Software Application

```
Example for SPI:(unused interrupt)
For Master


ORG 0X0
SETTING:
BANK            0
MOV A           , @0B00000000
MOV 0x05        , A
MOV A           , @0B00000100     ; SDI input and SDO, SCK
                                  ; output
IOW 0x05
BANK            2
MOV A           , @0B00010000     ; Select SPI Mode
MOV 0x0B        , A
BANK            1
MOV A           , @0B01000000     ; Enable SPI, Master
                                  ; and Baud Rate = Fosc/2
MOV 0x0C        , A
MOV A           , @0B00000000     ; shift left(MSB first)
MOV 0x0B        , A

START:
BANK            1
MOV A           , @0XAA           ; Move 0XAA at write SPI
                                  ; buffer
MOV 0X0E        , A
BS  0X0C        , 4               ; Start to shift SPI data
JBC 0X0C        , 4               ; Polling loop for checking
                                  ; SPI transmission completed
JMP $-1
JMP START                         ; Transmission DATA again.
```

```
Example for SPI:(unused interrupt)
For Slave


ORG 0X0
SETTING:
BANK            0
MOV A           , @0B00000000
MOV 0x05        , A
MOV A           , @0B00000100     ; SDI input and SDO, SCK
                                  ; output
IOW 0x05
BANK            2
MOV A           , @0B00010000     ; Select SPI Mode
MOV 0x0B        , A
BANK            1
MOV A           , @0B01000111     ; Enable SPI, Slave
                                  ; and /SS disable
MOV 0x0C        , A
MOV A           , @0B00000000     ; shift left(MSB first)
MOV 0x0B        , A

START:
BANK            1
BS  0X0C        , 4               ; Start to receive SPI data
JBS 0X0B        , 0               ; Polling loop for checking
                                  ; SPI receive completed
JMP $-1
MOV A           , 0X0D            ; Read SPI buffer and
                                  ; move to SRAM 0x10
MOV 0X10        , A
JBC 0X0B        , 0               ; Polling loop for checking
                                  ; SPI buffer was read.
JMP $-1
JMP START                         ; Receive DATA again.
```

6.15 Oscillator

6.15.1 Oscillator Modes

The EM78F564N device can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). User can select one of such modes by programming OSC2, OCS1 and OSC0 in the Code Option register. Table 6-16-1 depicts how these four modes are defined.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in Table 6-16-1:

Table 6-15-1 Oscillator Modes as Defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC (Internal RC oscillator mode); P55, P54 act as I/O pin	1	0	0
IRC (Internal RC oscillator mode); P55 act as I/O pin P54 act as RCOUT pin	1	0	1
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as I/O pin	1	1	0
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as RCOUT pin with Open-drain	1	1	1

In LXT2, LXT1, XT, HXT and ERC mode, OSCI and OSCO are used, they cannot be used as normal I/O pins.

In IRC mode, P55 is used as normal I/O pin.

NOTE

1. Frequency range of HXT mode is 16 MHz ~ 6 MHz.

2. Frequency range of XT mode is 6 MHz ~ 1 MHz.

3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz.

4. Frequency range of LXT2 mode is 32kHz.

Table 6-15-2 Summary of Maximum Operating Speeds

Conditions	VDD	Max Fxt. (MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	4.5	16.0

6.15.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78F564N can be driven by an external clock signal through the OSCI pin as shown in Figure 6-44 below.

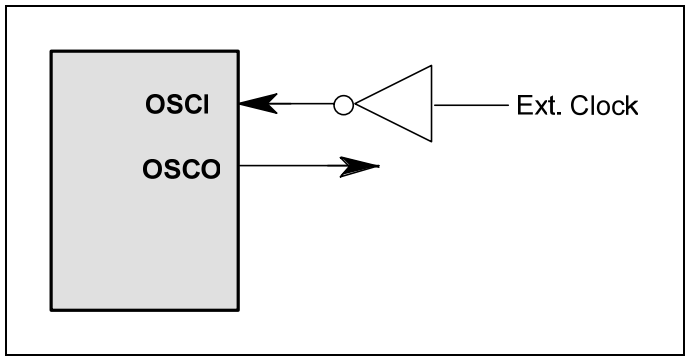


Figure 6-44 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-45 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 6-16-3 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

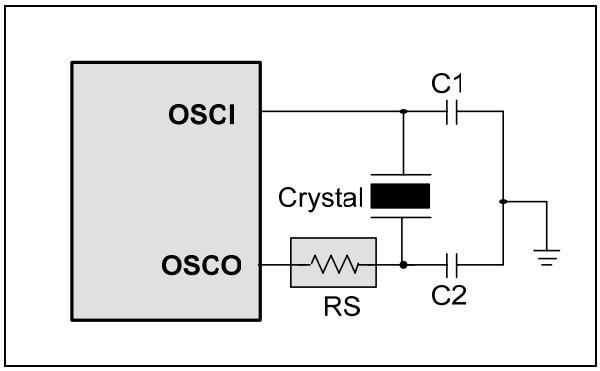


Figure 6-45 Circuit for Crystal/Resonator

Table 6-15-3 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100kHz	45pF	45pF
		200kHz	20pF	20pF
		455kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1M~6 MHz)	1.0 MHz	25pF	25pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100kHz	45pF	45pF
		200kHz	20pF	20pF
		455kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	20pF	20pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
		6.0 MHz	20pF	20pF
	HXT (6~16 MHz)	6.0 MHz	25pF	25pF
		8.0 MHz	20pF	20pF
		10.0 MHz	20pF	20pF
		12.0 MHz	20pF	20pF
		16.0 MHz	15pF	15pF

6.15.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Figure 6-46) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable since the NMOS cannot discharge correctly the current of the capacitance.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, will affect the system frequency.

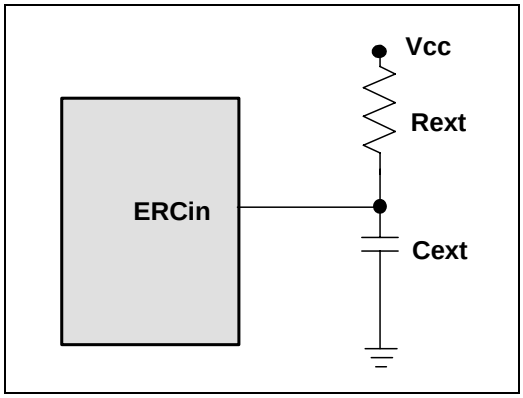


Figure 6-46 Circuit for External RC Oscillator Mode

Table 6-15-4 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: [1]: Measured based on DIP packages.

[2]: The values are for design reference only.

6.15.4 Internal RC Oscillator Mode

EM78F564N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz and 455kHz) that can be set by Code Option Word1<3,2> or switch by Bank1 R8<7,6>, RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option Word1<8~4>, C4~C0 (auto calibration).

Table 6-15-5 Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.5V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 2.5%	± 10.5%
16 MHz	± 3%	± 5%	± 2.5%	± 10.5%
8 MHz	± 3%	± 5%	± 2.5%	± 10.5%
455kHz	± 3%	± 5%	± 2.5%	± 10.5%

6.16 Code Option Register

The EM78F564N has a Code option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.16.1 Code Option Register (Word 0)

Word 0												
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	NRHL	NRE	–	CLKS1	CLKS0	ENWDTB	OSC2	OSC1	OSC0	Protect		
1	–	8/fc	Disable	–	High	High	Enable	High	High	High	Enable		
0	–	32/fc	Enable	–	Low	Low	Disable	Low	Low	Low	Disable		

Bit 12: Not used, set to "0" at all time

Bit 11 (NRHL): Noise rejection high/low pulse define bit. The INT pin is a falling edge trigger.

0 : Pulses equal to 32/fc [s] is regarded as signal (default)

1 : Pulses equal to 8/fc [s] is regarded as signal

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 10 (NRE): Noise rejection enable. The INT pin is a falling edge trigger.

0 : enable noise rejection (default) but in Low Crystal oscillator (LXT2) mode, the noise rejection circuit is always disabled

1 : disable noise rejection

Bit 9: Not used, set to "0" at all time.

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks (default)	0	0
2 clocks	0	1
8 clocks	1	0
16 clocks	1	1

Refer to the Instruction Set section.

Bit 6 (ENWDTB): Watchdog timer enable bit

0 : Disable (default)

1 : Enable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode) (default)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC (Internal RC oscillator mode); P55, P54 act as I/O pin	1	0	0
IRC (Internal RC oscillator mode); P55 act as I/O pin P54 act as RCOUT pin	1	0	1
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as I/O pin	1	1	0
ERC (External RC oscillator mode); P55 act as ERCin pin P54 act as RCOUT pin with Open-Drain	1	1	1

Note: 1. Frequency range of HXT mode is 16 MHz ~ 6 MHz.
2. Frequency range of XT mode is 6 MHz ~ 1 MHz.
3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz.
4. Frequency range of LXT2 mode is 32kHz.

Bit 2 ~ Bit 0 (Protect): Protect Bit. Protect type is as follows:

Protect	Protect
1	Enable
0	Disable

6.16.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	COBS0	TCEN	–	–	C4	C3	C2	C1	C0	RCM1	RCM0	LVR1	LVR0
1	Register	TCC	–	–	High	High	High	High	High	High	High	High	High
0	Option	P77	–	–	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12 (COBS0): IRC mode selection bit.

0: IRC frequency selection from code option (default)

1: IRC frequency selection from register.

Bit 11 (TCEN): TCC enable bit.

0: P77/TCC is set as P77 (default)

1: P77/TCC is set as TCC.

Bit 10: Not used, set to "1" at all time.

Bit 9: Not used, set to "1" at all time.

Bit 8 ~ Bit 4 (C4 ~ C0): Internal RC mode calibration bits. C4 ~ C0 must be set to "0" only (auto-calibration).

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
0	0	4 (default)
0	1	16
1	0	8
1	1	455kHz

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	0	NA	NA
0	1	2.7V	2.9V
1	0	3.7V	3.9V
1	1	4.1V	4.3V

LVR1, LVR0="0, 0" **:** LVR disable, power-on reset point of EM78F564N is 2.0~2.2V (default)

LVR1, LVR0="0, 1" **:** If Vdd < 2.7V, the EM78F564N will be reset.

LVR1, LVR0="1, 0" **:** If Vdd < 3.7V, the EM78F564N will be reset.

LVR1, LVR0="1, 1" **:** If Vdd < 4.1V, the EM78F564N will be reset.

6.16.3 Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	SC3	SC2	SC1	SC0	–	–	–	–	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	–	–	–	–	High	High	High	High	High
0	Low	Low	Low	Low	–	–	–	–	Low	Low	Low	Low	Low

Bits 12 ~ 9 (SC3 ~ SC0): Calibrator of sub frequency (WDT frequency, auto calibration).

Bit 8: Not used, set to "0" at all time.

Bit 7: Not used, set to "1" at all time.

Bits 6 ~ 5: Not used, set to "0" at all time.

Bits 4 ~ 0: Customer's ID code.

6.17 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply has stabilized. The EM78F564N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V~2.2V. It will work well if Vdd can rise quickly enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.18 External Power-on Reset Circuit

The circuit shown in Figure 6-47 uses an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40 KΩ. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) functions as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to the /RESET pin.

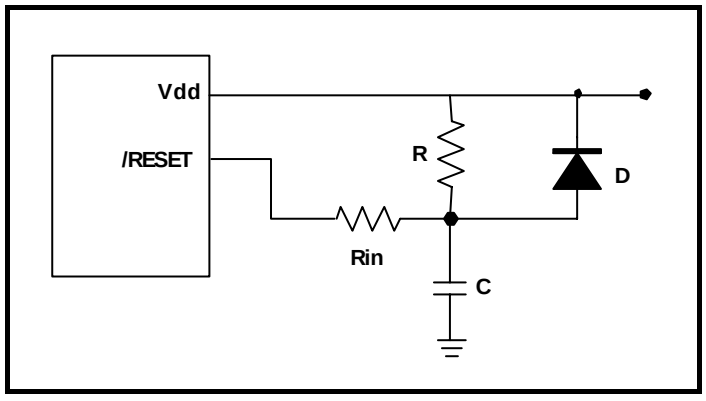


Figure 6-47 External Power-up Reset Circuit

6.19 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-48 and Figure 6-49 shows how to make a residue-voltage protection circuit.

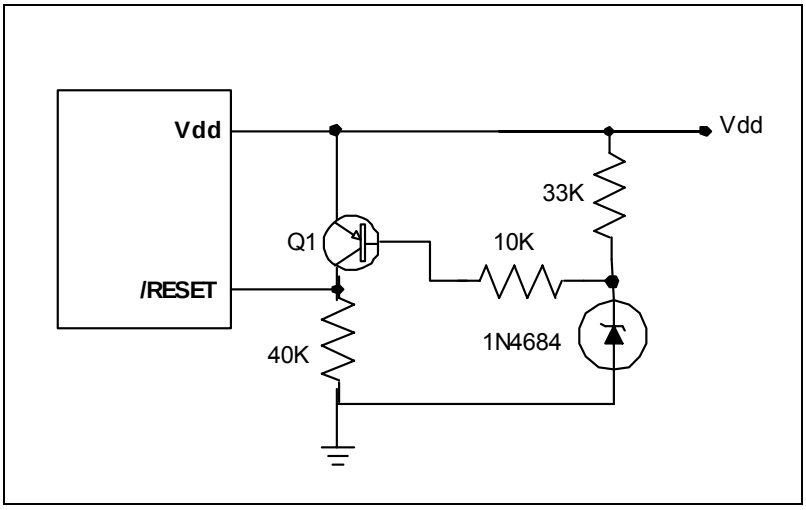


Figure 6-48 Residue Voltage Protection Circuit 1

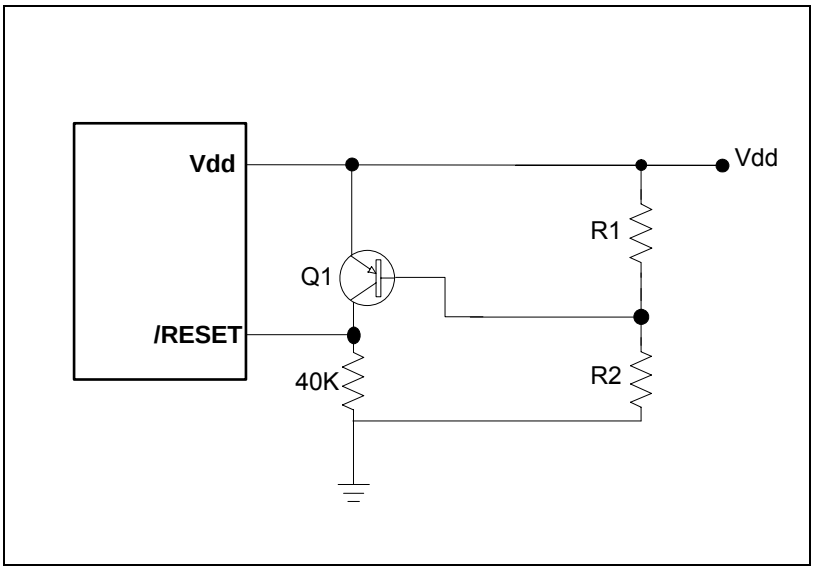


Figure 6-49 Residue Voltage Protection Circuit 2

6.20 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ·etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try to modify the instruction as follows:

(A) Change one instruction cycle to consist of four oscillator periods.

(B) "LJMP", "LCALL", "TBRD", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit called CLK1:0. One instruction cycle consists of two oscillator clocks if CLK1:0 is ”01”, and four oscillator clocks if CLK1:0 is ”00”.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source for TCC should be CLK = Fc as indicated in Figure 6-12-1.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z

Note: [1] This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	K → R4(7:6)	None

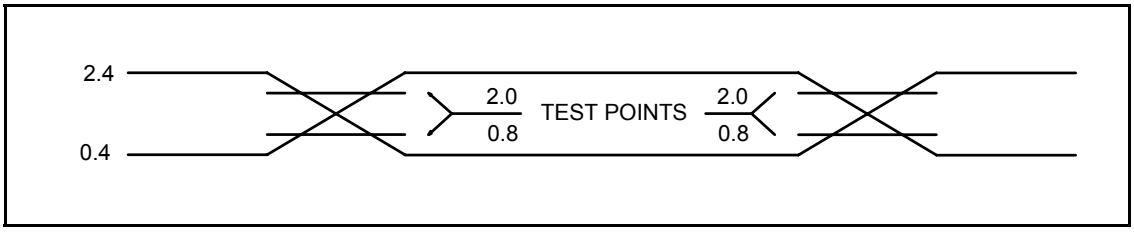
Note: [2] This instruction is not recommended for interrupt status register operation.

[3] This instruction cannot operate under interrupt status register.

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
1 1110 1010 kkkk k kkkk kkkk kkkk	1EAk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1 → [SP], k → PC	None
1 1110 1011 kkkk k kkkk kkkk kkkk	1EBk	LJMP k	Next instruction: k kkkk kkkk kkkk k → PC	None
1 1110 11rr rrrr	1Err	TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else Bank 3 R6.7=1, machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

7 Timing Diagram

AC Test Input/Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.4V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**," and 0.8V for logic "**0**"*

Figure 7-1 AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK1:0 = "01")

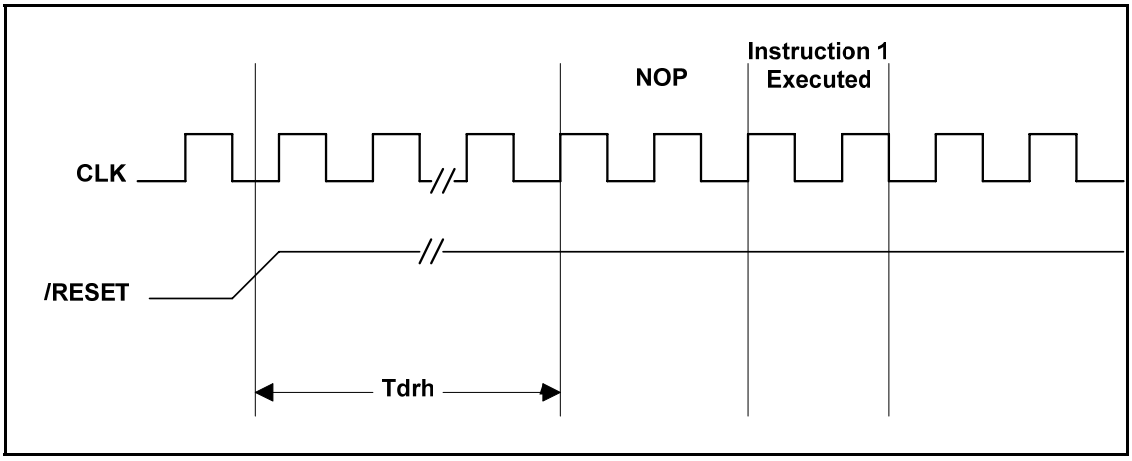


Figure 7-2 Reset Timing Diagram

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.3	to	5.5V
Working frequency	DC	to	16 MHz
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

Note: These parameters are theoretical values and have not been tested.

9 DC Electrical Characteristics

Ta=25°C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	370	F+30%	kHz
	IRC: VDD to 5 V	4 MHz, 16 MHz, 8 MHz, 455kHz	F-2.5%	F	F+2.5%	Hz
IIL	Input Leakage Current for Input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	0.7VDD	–	VDD + 0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD + 0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD + 0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.5V (IOH =3.7mA)	-3.0	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 7, 8)	VOL = GND+0.5V	9	11	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = GND+0.5V	15	18	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	–	-70	-80	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	–	20	30	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	1.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	8	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled.	–	37	40	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled.	–	39	43	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled. (*VDD = 3V)	–	110	120	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC4	Operating supply current at two clocks	/RESET = 'High', Fosc=455kHz (IRC type, CLKS1:0="01"), Output pin floating, WDT enabled. (*VDD = 3V)	–	100	110	μA
ICC5	Operating supply current at two clocks	/RESET = 'High', Fosc = 4 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	1.5	mA
ICC6	Operating supply current at two clocks	/RESET = 'High', Fosc = 10 MHz (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	2.7	3	mA

Note: These parameters are theoretical values and have not been tested.

*Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, ”Max.”) columns are based on characterization results at 25°C. These data are for design reference only and are not tested.

Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	–	–	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

A/D Converter Characteristics (Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C)

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0V (V reference from Vdd)	1150	1300	1450	μA
	Ivref			-10	0	10	μA
IAI2	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0V (V reference from VREF)	700	800	900	μA
	IVref			450	500	550	μA
RN		Resolution	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	8	9	–	Bits
LN		Linearity error	Vdd = 2.5 to 5.5V Ta=25°C	–	±2	±4	LSB
DNL		Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25°C	–	±0.5	±0.9	LSB
FSE		Full scale error	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	–	±1	±2	LSB
OE		Offset error	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	–	±1	±2	LSB
ZAI		Recommended impedance of analog voltage source	–	–	8	10	KΩ
TAD1		A/D clock period	Vdd=V_{AREF}=2.5~5.5V, V_{ASS} =0V	4	–	–	us
TAD2		A/D clock period	Vdd=V_{AREF}=3.0~5.5V, V_{ASS} =0V	1	–	–	us
TCN		A/D conversion time	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	14	–	14	TAD
ADIV		A/D OP input voltage range	Vdd=V_{AREF}=5.0V, V_{ASS} =0V	0	–	V_{AREF}	V
PSR		Power Supply Rejection	Vdd=5.0V±0.5V	–	–	±2	LSB

Note: 1. The parameters are theoretical values and have not been tested. Such parameters are for design reference only.
2. When A/D is off, no current is consumed other than minor leakage current.
3. The A/D conversion result does not decrease with an increase in the input voltage, and there's no missing code.
4. Specifications are subject to change without prior notice.

Comparator Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	RL = 5.1K (Note [1])	–	–	10	mV
Vcm	Input common-mode voltages range	(Note [2])	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	μA
TRS	Response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), overdrive=30mV (Note [3])	–	0.7	–	μs
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load),	–	300	–	ns
VS	Operating range	–	2.5	–	5.5	V

Note: [1] The output voltage is in the unit gain circuitry and over the full input common-mode range.

[2] The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.

[3] The response time specified is a 100 mV input step with 30 mV overdrive.

10 AC Electrical Characteristics

EM78F564N, 0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	14	16	18	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	14	16	18	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

Note: The parameters are theoretical values and have not been tested. Such parameters are for design reference only.

Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, ”Max.”) columns are based on characterization results at 25°C.

*N = selected prescaler ratio.

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F564NK24J/S	Skinny DIP	24	300 mil
EM78F564NSO24J/S	SOP	24	300 mil
EM78F564NK28J/S	Skinny DIP	28	300 mil
EM78F564NSO28J/S	SOP	28	300 mil
EM78F564NQN32J/S	QFN	32	5×5 mm

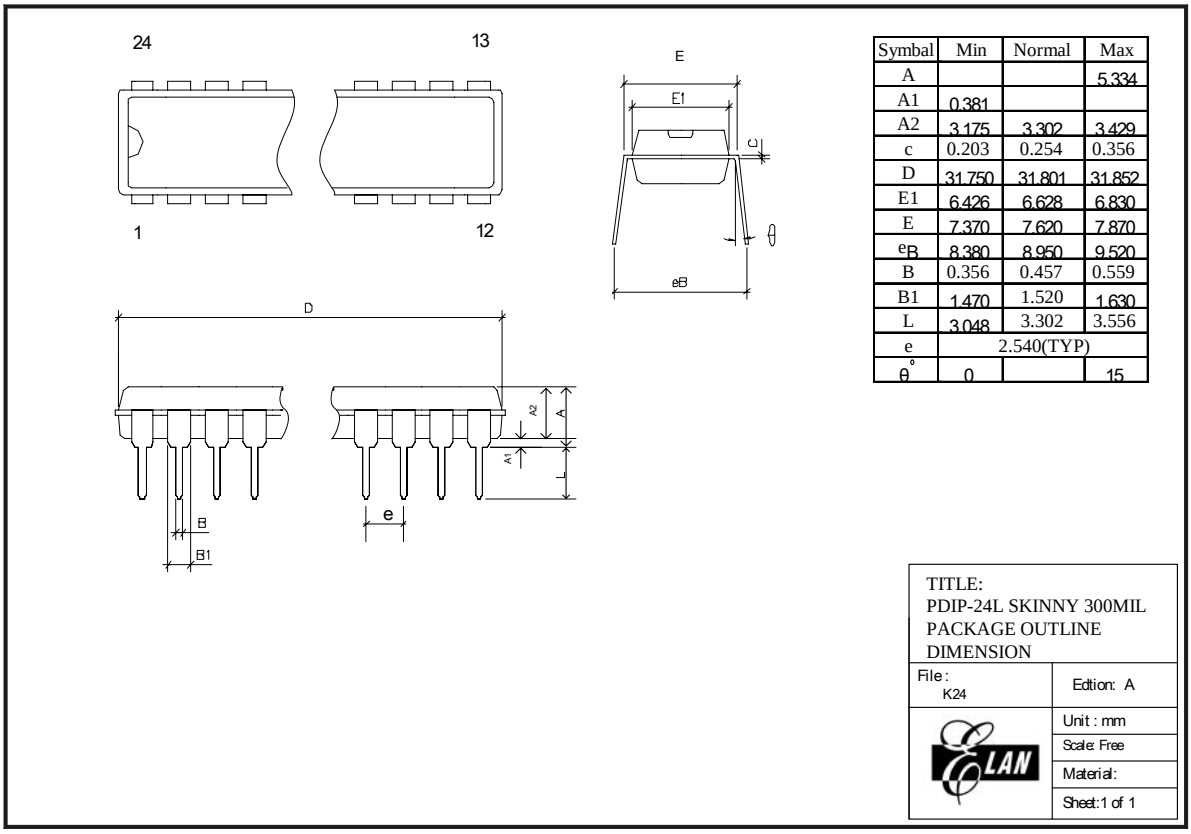
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78F564NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78F564NK24



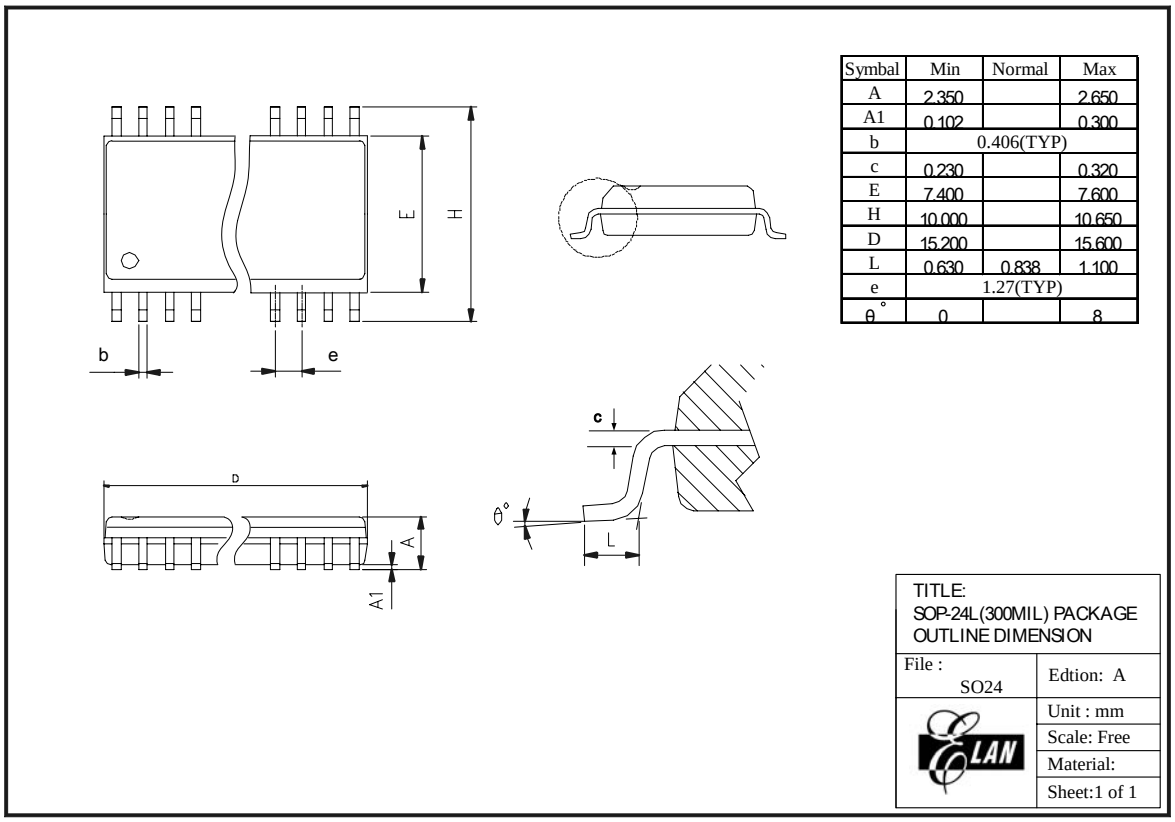
Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
e_B	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE:
PDIP-24L SKINNY 300MIL
PACKAGE OUTLINE
DIMENSION

File: K24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78F564N 24-pin Skinny DIP Package Type

B.2 EM78F564NSO24

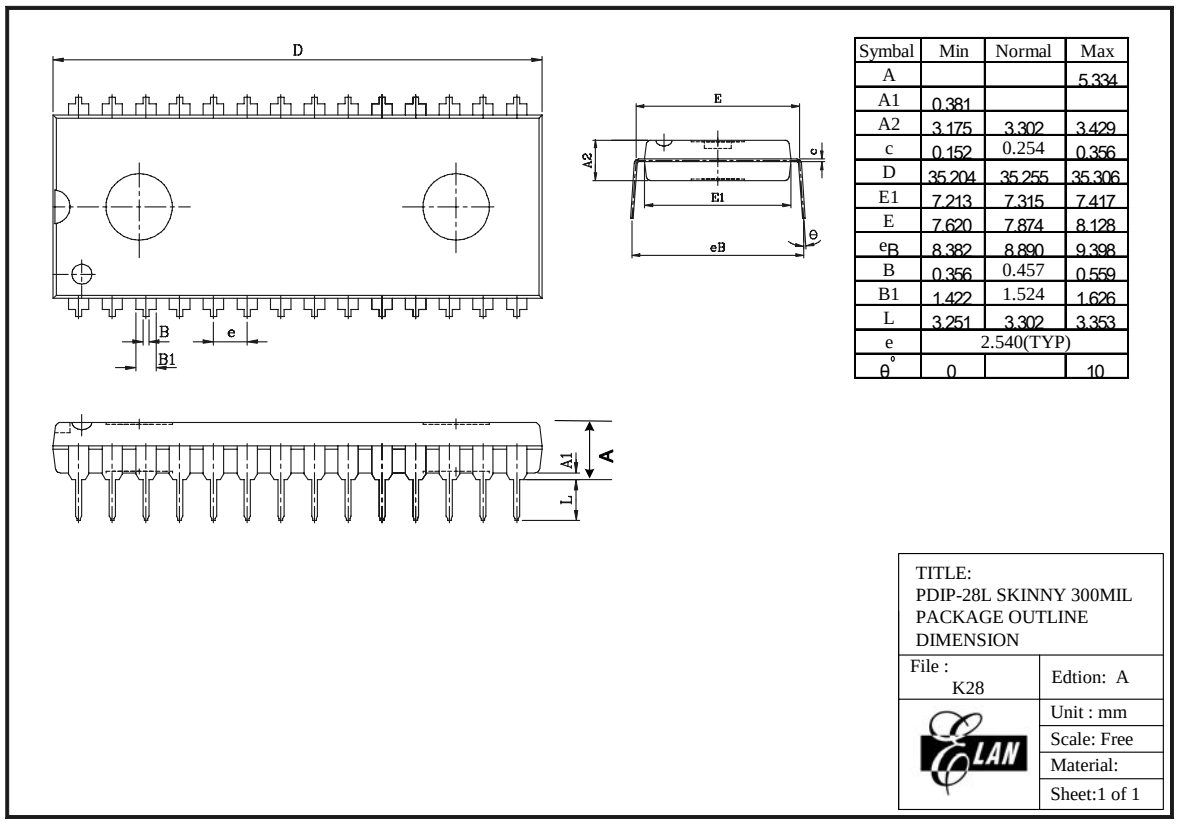


Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-24L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-2 EM78F564N 24-pin SOP Package Type

B.3 EM78F564NK28

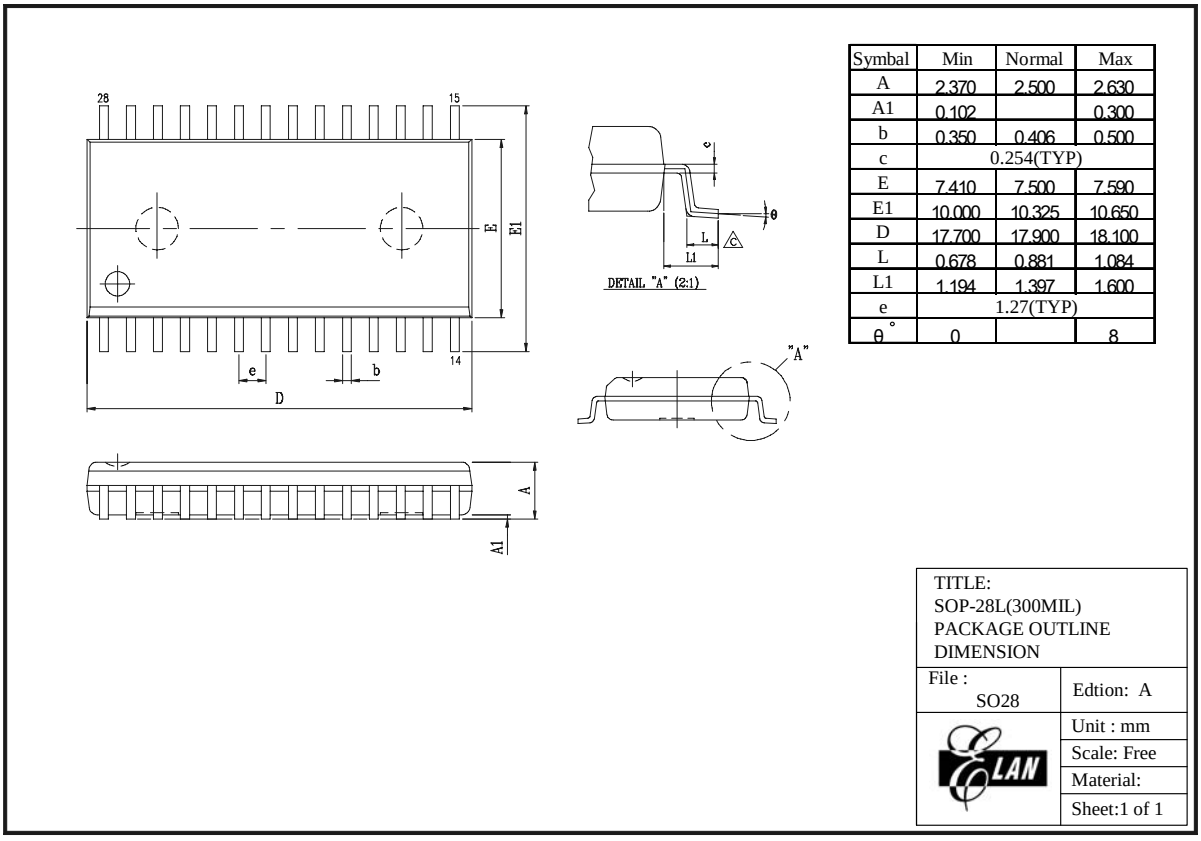


Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
e_B	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ°	0		10

TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-3 EM78F564N 28-pin Skinny DIP Package Type

B.4 EM78F564NSO28

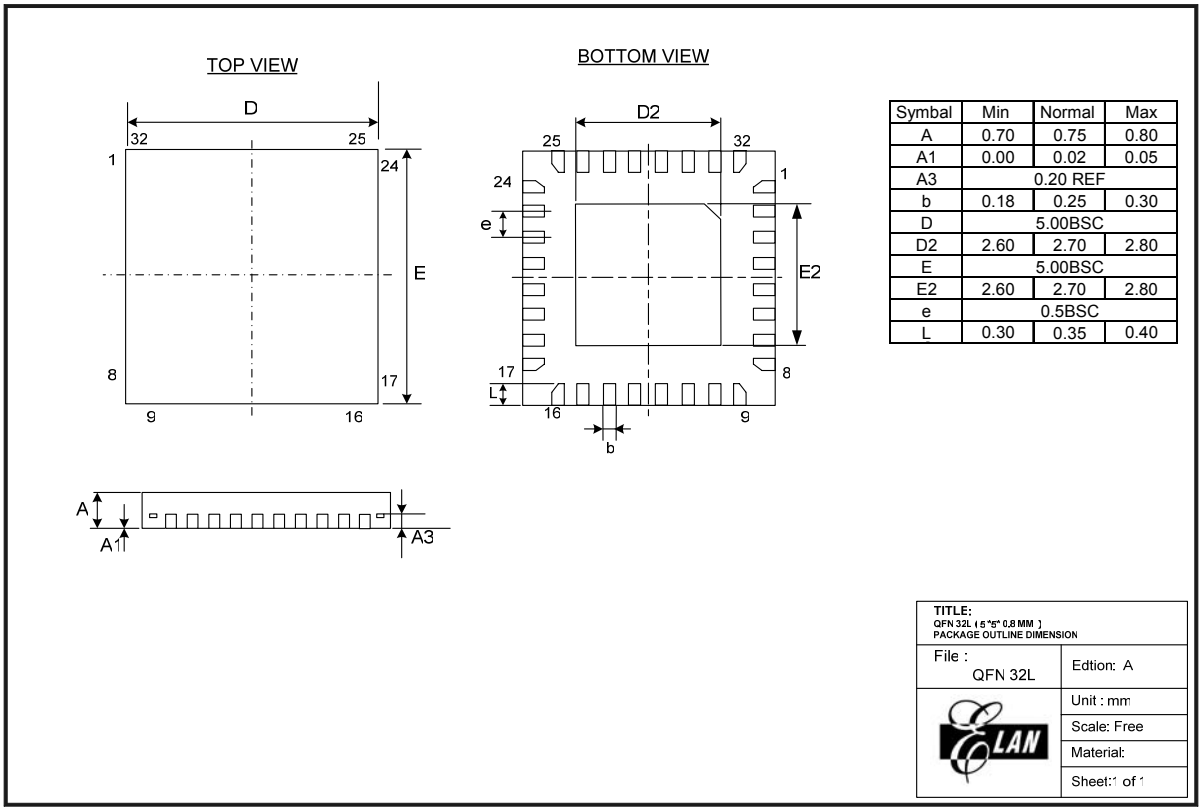


Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ °	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 EM78F564N 28-pin SOP Package Type

B.5 EM78F564NQN32



Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		5.00BSC	
D2	2.60	2.70	2.80
E		5.00BSC	
E2	2.60	2.70	2.80
e		0.5BSC	
L	0.30	0.35	0.40

TITLE:
QFN 32L (5*5*0.8 MM)
PACKAGE OUTLINE DIMENSION

File : QFN 32L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-5 EM78F564N 32-pin QFN Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60% , TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85% , TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥|± 3KV|	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ |± 300V|	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.