EM78P346N

8-Bit Microprocessor with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2007/05
1.0	Initial pre-released version	2007/12/25
1.1	Modified Type 1 and Type 0 description for code option	2008/10/31
1.2	Added Section 8.3 *Device Characteristics*	2011/04/21
1.3	1. Added Ordering and Manufacturing Information. 2. Added LVR specifications	2013/03/26
1.4	1. Modified the Pin Description Information. 2. Added package type EM78P346NASO20. 3. Added the Code Option “HLP” bit.	2014/09/15

Item	EM78P346N
Level Voltage Reset	**4.1V, 3.7V, 2.8V**
Crystal mode Operating frequency range	**DC ~ 16 MHz, 4.5V DC ~ 8 MHz, 3.0V DC ~ 4 MHz, 2.1V**
IRC mode Wake-up time (Sleep mode → Normal mode)	**10 µs Condition: 5V, 4 MHz**
Code Option	**With Code Option NRM**

1 General Description

The EM78P346N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has as an on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With its enhanced OTP-ROM feature, the device provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 144×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Four programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.3V
  - Three programmable Level Voltage Reset (LVR) : 4.1V, 3.7V, 2.4V
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - Three bidirectional I/O ports
  - Wake-up port : P6
  - 21 programmable pull-down I/O pins
  - 21 programmable pull-high I/O pins
  - 22 programmable open-drain I/O pins
  - Four programmable high-sink I/O pins
  - External interrupt : P50
- Operating voltage range:
  - 2.1V~5.5V at 0°C~70°C (commercial)
  - 2.3V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on two clocks):
  - Crystal mode: DC ~ 16 MHz, 4.5V
    DC ~ 8 MHz, 3V; DC ~ 4 MHz, 2.1V
  - RC mode: DC ~ 16 MHz, 4.5V;
    DC ~ 12 MHz, 4V; DC ~ 4 MHz, 2.1V
  - Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.3V~5.5V)	Process	Total
455kHz	±5%	±5%	±4%	±14%
1 MHz	±5%	±5%	±4%	±14%
4 MHz	±5%	±5%	±4%	±14%
16 MHz	±5%	±5%	±4%	±14%

- All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE346N Simulator. OTP is auto trimmed by ELAN Writer.
- Fast set-up time requires only 0.8 ms (HXT2, 4 MHz) in high Crystal and 32 CLKS in IRC mode from wake up to operating mode
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Three Pulse Width Modulation (PWM) with 10-bit resolution
  - One pair of comparator (offset voltage: 5mV)
  - One pair of OP (offset voltage: 5 mV)
  - Power-down (Sleep) mode
  - High EFT immunity (4 MHz, 4 clocks)
- Seven available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Comparator high/low interrupt
  - Low voltage detector interrupt
- Programmable free running Watchdog Timer
  - Watchdog Timer: 16.5ms ± 5% with Vdd =5V at 25°C, Temperature range ± 5% (-40°C ~+85°C)
  - Watchdog Timer: 18ms ± 5% with Vdd =3V at 25°C, Temperature range ± 5% (-40°C~+85°C)
  - Two clocks per instruction cycle
- Package Type:
  - 18-pin DIP 300mil : EM78P346ND18J/S
  - 18-pin SOP 300mil : EM78P346NSO18J/S
  - 20-pin DIP 300mil : EM78P346ND20J/S
  - 20-pin SOP 300mil : EM78P346NSO20J/S
  - 20-pin SOP 300mil : EM78P346NASO20J/S
  - 20-pin SSOP 209mil : EM78P346NSS20J/S
  - 24-pin skinny DIP 300mil : EM78P346NK24J/S
  - 24 pin SOP 300mil : EM78P346NSO24J/S
  - 24 pin SSOP 150mil : EM78P346NSS24J/S

Note: *These are Green products which do not contain hazardous substances.*

3 Pin Assignment

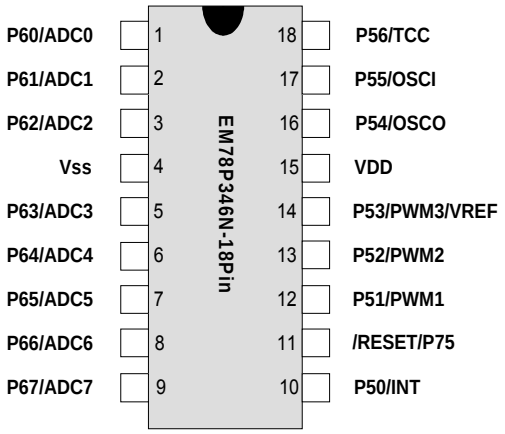


Figure 3-1 EM78P346ND18/SO18

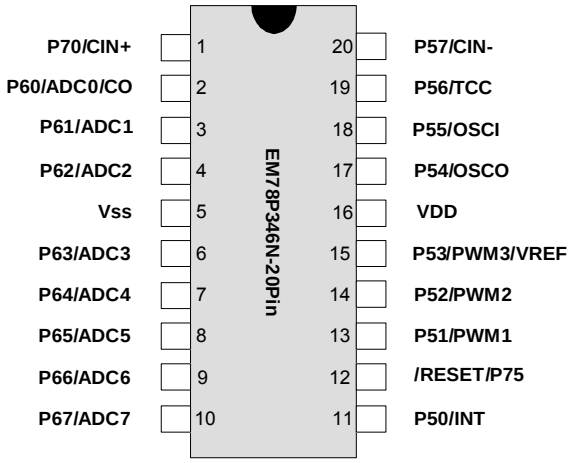


Figure 3-2 EM78P346ND20/SO20/SS20

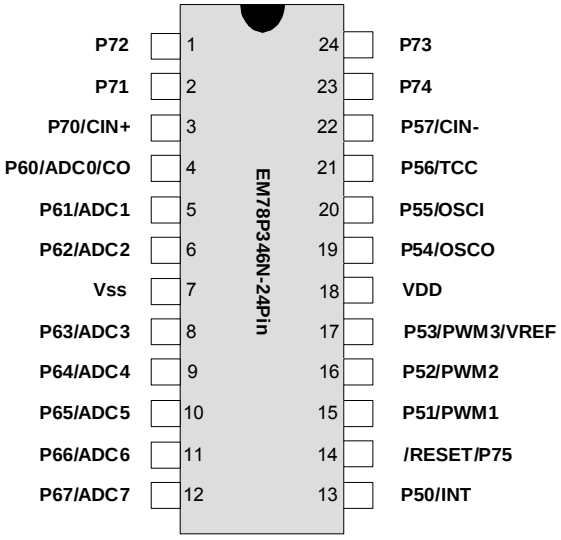


Figure 3-3 EM78P346NK24/SO24/SS24

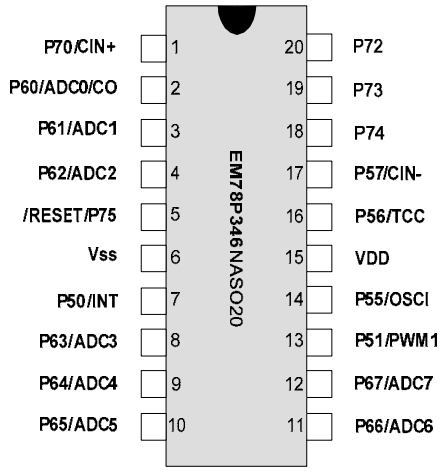


Figure 3-4 EM78P346NASO20

4 Pin Description

4.1 EM78P346ND18/SO18

Symbol	Pin No.	Type	Function
P50~P56	10, 12~14 16~18	I/O	7-bit General purpose input/output pins Default value at power-on reset
P60~P67	1~3 5~9	I/O	8-bit General purpose input/output pins Default value at power-on reset
P75	11	I/O	1-bit General purpose input/output pins Default value at power-on reset P75 is open drain for output port
INT	10	I	External interrupt pin triggered by a rising and falling edge
ADC0~ADC7	1~3 5~9	I	8-bit Analog to Digital Converter Defined by ADCON (R9)<0:2>
PWM1 PWM2 PWM3	12 13 14	O	Pulse width modulation outputs Defined by PWMCON (IOC80)<5:7>
VREF	14	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/RESET	11	I	General-purpose Input only If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
TCC	18	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
OSCI	17	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	16	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time.
VDD	15	–	Power supply
VSS	4	–	Ground

4.2 EM78P346ND20/SO20/SS20

Symbol	Pin No.	Type	Function
P50~P57	11, 13~15 17~20	I/O	8-bit General purpose input/output pins Default value at power-on reset
P60~P67	2~4 6~10	I/O	8-bit General purpose input/output pins Default value at power-on reset
P70, P75	1, 12	I/O	2-bit General purpose input/output pins Default value at power-on reset P75 is open drain for output port
INT	11	I	External interrupt pin triggered by a rising and falling edge
ADC0~ADC7	2~4 6~10	I	8-bit Analog to Digital Converter Defined by ADCON (R9)<0:2>
PWM1 PWM2 PWM3	13 14 15	O	Pulse width modulation outputs Defined by PWMCON (IOC80)<5:7>
VREF	15	I	External reference voltage for ADC Defined by ADCON (R9) <7>
CIN-, CIN+, CO	20 1 2	I I O	"-" : input pin of Vin- of the comparator "+" : input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (IOCA) <0:1>
/RESET	12	I	General-purpose Input only If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
TCC	19	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
OSCI	18	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	17	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time.
VDD	16	–	Power supply
VSS	5	–	Ground

4.3 EM78P346NK24/SO24/SS24/ASO20

Symbol	Pin No.	Type	Function
P50~P57	13, 15~17 19~22	I/O	8-bit General purpose input/output pins Default value at power-on reset
P60~P67	4~6 8~12	I/O	8-bit General purpose input/output pins Default value at power-on reset
P70~P75	3, 2, 1, 24 23, 14	I/O	6-bit General purpose input/output pins Default value at power-on reset P75 is open drain for output port
INT	13	I	External interrupt pin triggered by a rising and falling edge
ADC0~ADC7	4~6 8~12	I	8-bit Analog to Digital Converter Defined by ADCON (R9)<0:2>
PWM1 PWM2 PWM3	15 16 17	O	Pulse width modulation outputs Defined by PWMCON (IOC80)<5:7>
VREF	17	I	External reference voltage for ADC Defined by ADCON (R9) <7>
CIN- CIN+ CO	22 3 4	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (IOCA) <0:1>
/RESET	14	I	General-purpose Input only If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
TCC	21	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
OSCI	20	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	19	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time.
VDD	18	–	Power supply
VSS	7	–	Ground

5 Block Diagram

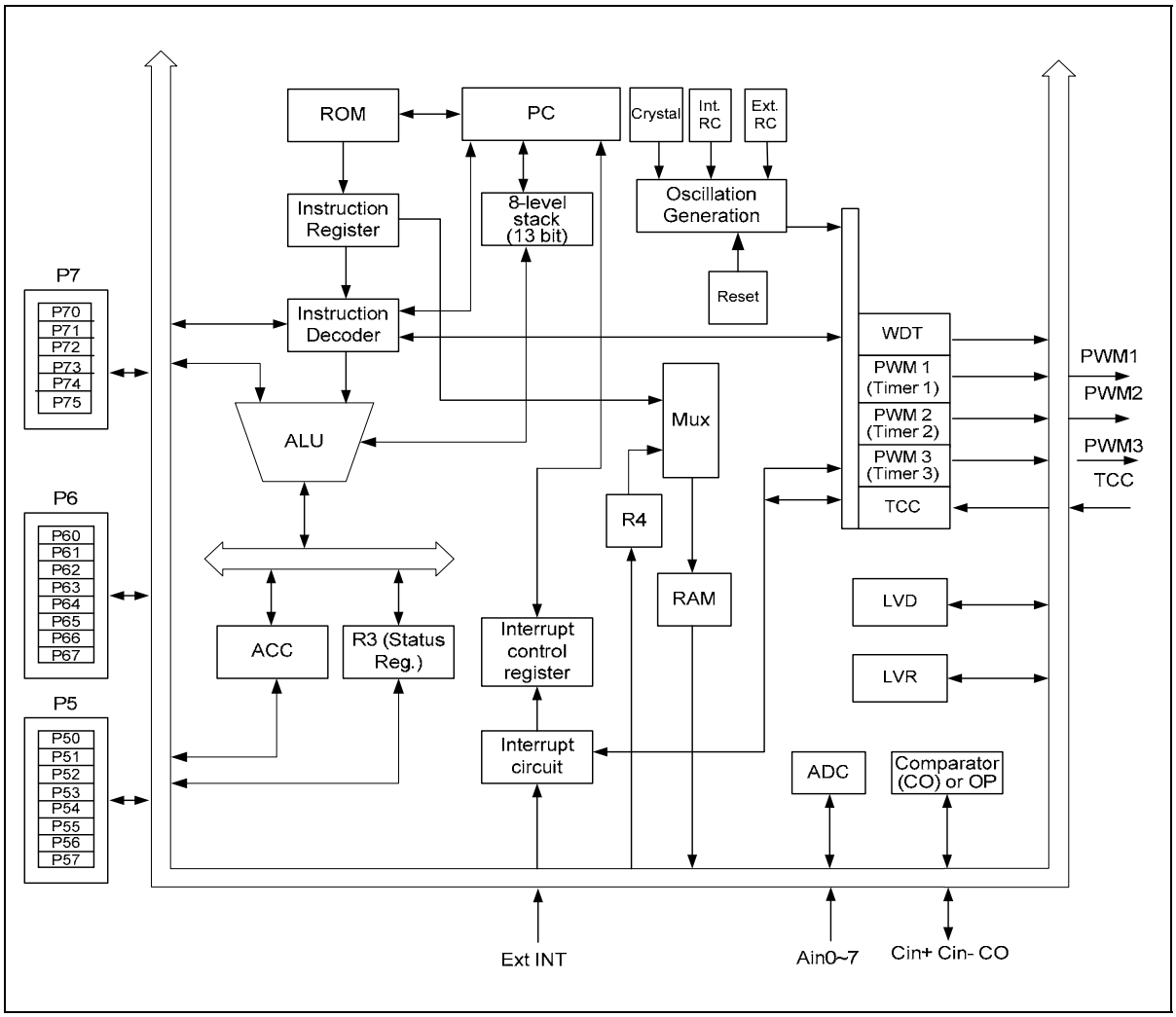


Figure 5 EM78P346N Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge through the TCC pin, or by the instruction cycle clock.
- The external signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increase the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

6.1.3 R2 (Program Counter) and Stack

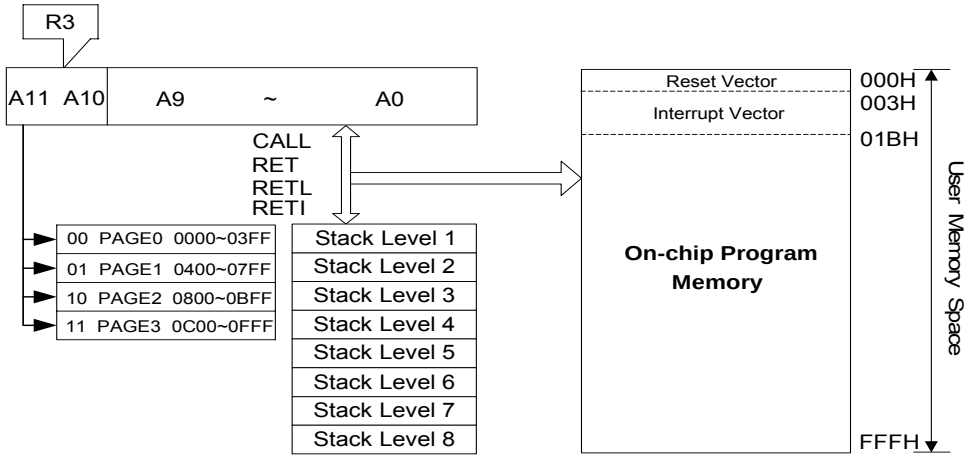


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 12-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration* (next section).
- The configuration structure generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will be incremented progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2, A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- In the case of EM78P346N, the most two significant bits (A11 and A10) will be loaded with the content of PS1 and PS0 in the status register (R3) upon execution of a "JMP", "CALL", or any other instruction set which write to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions that are written to R2. Note that these instructions need one or two instruction cycles as determined by the Code Option Register CYES bit.

6.1.3.1 Data Memory Configuration

Address	Bank 0 Registers	Bank 1 Registers	IOC Page 0 Registers	IOC Page 1 Registers
00	**R0** (Indirect Addressing Register)	Reserve	Reserve	Reserve
01	**R1** (Time Clock Counter)	Reserve	Reserve	Reserve
02	**R2** (Program Counter)	Reserve	Reserve	Reserve
03	**R3** (Status Register)	Reserve	Reserve	Reserve
04	**R4** (RAM Select Register)	Reserve	Reserve	Reserve
05	**R5** (Port 5)	**R5** (PRDxH: PWM1, 2, 3 high period)	**IOC50** (I/O Port Control Register)	**IOC51** (PRD1: PWM1 period)
06	**R6** (Port 6)	**R6** (LVD Control Register)	**IOC60** (I/O Port Control Register)	**IOC61** (PRD2: PWM2 period)
07	**R7** (Port 7)	**R7** (High Output Sink Current)	**IOC70** (I/O Port Control Register)	**IOC71** (PRD3: PWM3 period)
08	**R8** (ADC Input Select Register)	**R8** (Pull-down Control Register)	**IOC80** (PWM Control Register)	**IOC81** (DT1L: Duty cycle of PWM1)
09	**R9** (ADC Control Register)	**R9** (Pull-down Control Register)	**IOC90** (Timer Control Register)	**IOC91** (DT2L: Duty cycle of PWM2)
0A	**RA** (ADC Offset Calibration Register)	**RA** (Open-drain Control Register)	**IOCA0** (Comparator Control Register)	**IOCA1** (DT3L: Duty cycle of PWM3)
0B	**RB** (ADC Output Select Register)	**RB** (Open-drain Control Register)	**IOCB0** (Pull-down Control Register)	**IOCB1** (DTH: Duty cycle of PWM)
0C	**RC** (ADDATA1H: A/D data Bit 11~Bit 8)	**RC** (Pull-high Control Register)	**IOCC0** (Open-drain Control Register)	**IOCC1** (TIMER1L: PWM1 Timer)
0D	**RD** (ADDATA1L: A/D data Bit 7~Bit 0)	**RD** (Pull-high Control Register)	**IOCD0** (Pull-high Control Register)	**IOCD1** (TIMER2L: PWM2 Timer)
0E	**RE** (Wake-up Control Register)	**RE** (Option Control bits, Only for ICE)	**IOCE0** (WDT Control Register)	**IOCE1** (TIMER3L: PWM3 Timer)
0F	**RF** (Interrupt Status Register)	Reserve	**IOCF0** (Interrupt Mask Register)	**IOCF1** (TMRH: PWM Timer)
10 : 1F	General Registers			
20 : 3F	**Bank 0**	**Bank 1**	**Bank 2**	**Bank 3**

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCS	-	-	T	P	Z	DC	C

Bit 7 (IOCS): Select the Segment of the I/O control register.

0: Segment 0 (IOC50 ~ IOCF0) selected

1: Segment 1 (IOC51 ~ IOCF1) selected

Bit 6 ~ Bit 5: fixed to "0"

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power-on and reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to "1" during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7 and Bit 6: are used to select Banks 0 ~ 3.

Bit 5 ~ Bit 0: are used to select registers (Address**:** 00 ~ 3F) in the indirect address mode.

See table under Section 6.1.3.1 *Data Memory Configuration*.

6.1.6 Bank 0 R5 ~ R7 (Port 5 ~ Port 7)

R5 and R6 are I/O registers.

R7 is an I/O register. The upper 2 bits of R7 are fixed at 0.

6.1.7 Bank 0 R8 (AISR: ADC Input Select Register)

The AISR register defines the pins of Port 6 as analog inputs or as digital I/O, individually.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin

0: Disable ADC7, P67 acts as I/O pin

1: Enable ADC7, acts as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

0: Disable ADC6, P66 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin

0: Disable ADC5, P65 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0: Disable ADC4, P64 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0: Disable ADC3, P63 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0: Disable ADC2, P62 functions as I/O pin

1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0: Disable ADC1, P61 functions as I/O pin

1: Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0: Disable ADC0, P60 functions as I/O pin

1: Enable ADC0 to function as analog input pin

NOTE

Take note of the pin priority of the COS1 and COS0 bits of IOCA0 Control register when P60/ADE0 functions as analog input or as digital I/O. The Comparator/OP select bits are as shown in a table under Section 6.2.6, IOCA0 (CMPCON: Comparator Control Register).

The P60/ADE0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADE0	P60

6.1.8 Bank 0 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53

1: The Vref of the ADC is connected to P53/VREF

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. If P53/PWM3/VREF functions as VREF analog input pin, then PWM3E must be "0".

The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 and Bit 5 (CKR1 and CKR0): Prescalers of ADC oscillator clock rate

00 = 1: 16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: 8

CKR1 : CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Fosc/8	2 MHz

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit **cannot** be reset through software.

1: AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ADIS0): Analog Input Select

000 = ADIN0/P60

001 = ADIN1/P61

010 = ADIN2/P62

011 = ADIN3/P63

100 = ADIN4/P64

101 = ADIN5/P65

110 = ADIN6/P66

111 = ADIN7/P67

These bits can only be changed when the ADIF bit (see Section 6.1.14) and the ADRUN bit are both **low**.

6.1.9 Bank 0 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	“0”	“0”	“0”

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P346N	ICE346
0	0	0	0 LSB	0 LSB
0	0	1	2 LSB	2 LSB
0	1	0	4 LSB	4 LSB
0	1	1	6 LSB	6 LSB
1	0	0	8 LSB	8 LSB
1	0	1	10 LSB	10 LSB
1	1	0	12 LSB	12 LSB
1	1	1	14 LSB	14 LSB

Bit 2 ~ Bit 0: Unimplemented, read as ‘0’

6.1.10 Bank 0 RB (ADDATA: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared, and the ADIF bit (see Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register)*) is set.

RB is read only.

6.1.11 Bank 0 RC (ADDATA1H: ADC Converted Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	AD11	AD10	AD9	AD8

When AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register)*) is set.

RC is read only.

6.1.12 Bank 0 RD (ADDATA1L: ADC Converted Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14, *RE (Interrupt Status 2 and Wake-up Control Register)*) is set.

RD is read only

6.1.13 Bank 0 RE (WUCR: Wake- up Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P346N	"0"	"0"	"0"	"0"	ADWE	CMPWE	ICWE	"0"
ICE346 Simulator	C3	C2	C1	C0	ADWE	CMPWE	ICWE	"0"

Bit 7 ~ Bit 4:

[With EM78P346N]: Unimplemented, read as '0'

[With Simulator (C3~C0)]: IRC calibration bits in IRC oscillator mode. Under IRC oscillator mode of ICE346 simulator, these are the IRC calibration bits in IRC oscillator mode.

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) x F
0	0	0	1	(1-31.5%) x F
0	0	1	0	(1-27%) x F
0	0	1	1	(1-22.5%) x F
0	1	0	0	(1-18%) x F
0	1	0	1	(1-13.5%) x F
0	1	1	0	(1-9%) x F
0	1	1	1	(1-4.5%) x F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) x F
1	1	0	1	(1+9%) x F
1	1	0	0	(1+135%) x F
1	0	1	1	(1+18%) x F
1	0	1	0	(1+22.5%) x F
1	0	0	1	(1+27%) x F
1	0	0	0	(1+31.5%) x F

Note: *1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence, they are shown for reference only. Definite values depend on the actual process.*

2. Similar way of calculation is also applicable for low frequency mode.

Bit 3 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up

1: Enable ADC wake-up

When the ADC Complete status is used to enter the interrupt vector or to wake up the EM78P346N from sleep with AD conversion running, the ADWE bit must be set to “Enable“.

Bit 2 (CMPWE): Comparator wake-up enable bit

0: Disable Comparator wake-up

1: Enable Comparator wake-up

When the Comparator output status change is used to enter the interrupt vector or to wake-up the EM78P346N from sleep, the CMPWE bit must be set to “Enable“.

Bit 1 (ICWE): Port 6 input change to wake-up status enable bit

0: Disable Port 6 input change to wake-up status

1: Enable Port 6 input change to wake-up status

When the Port 6 Input Status Change is used to enter the interrupt vector or to wake-up the EM78P346N from sleep, the ICWE bit must be set to “Enable“.

Bit 0: Not implemented, read as ‘0’

6.1.14 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

NOTE

- *"1" means there's interrupt request; "0" means no interrupt occurs.*
- *RF can be cleared by instruction but cannot be set.*
- *IOCF0 is the interrupt mask register.*
- *Reading RF will result to "logic AND" of RF and IOCF0.*

Bit 7 (CMPIF): Comparator Interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 6 (PWM3IF): PWM3 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 3 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.15 Bank 1 R5 (PRDxH: PWM 1, 2, 3 High Period Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PRD3[9]	PRD3[8]	PRD2[9]	PRD2[8]	PRD1[9]	PRD1[8]

Bit 5 and Bit 4: Most Significant Bits of PWM 3 time period.

Bit 3 and Bit 2: Most Significant Bits of PWM 2 time period.

Bit 1 and Bit 0: Most Significant Bits of PWM 1 time period.

6.1.16 Bank 1 R6 (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0

NOTE

- *Bank 1 R6 <4> register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in Bank 1 R6 <4> to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag

LVDIF reset to “0” by software or hardware.

Bit 5 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 4: **0:** means no interrupt occurs.

1: means there’s interrupt request

Bit 4 (LVDIE): Low voltage Detector interrupt enable bit.

0: Disable Low voltage Detector interrupt.

1: Enable Low voltage Detector interrupt.

When the Low Voltage Detect low level state is used to enter the interrupt vector or enter next instruction, the LVDIE bit must be set to “Enable“.

Bit 3 (LVDWE): Low Voltage Detect wake-up enable bit.

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

When the Low Voltage Detect is used to enter the interrupt vector or to wake up the IC from sleep with Low Voltage Detect running, the LVDWE bit must be set to “Enable“.

Bit 2 (LVDEN): Low Voltage Detector enable bit

0: Disable Low voltage detector

1: Enable Low voltage detector

Bits 1~0 (LVD1:0): Low Voltage Detector level bits.

LVDEN Bank 0 <R8, 7>	LVD1, LVD0 <RA, 1, 0>	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.3V	0
		Vdd > 2.3V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	1

6.1.17 Bank 1 R7 (Output Sink Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE-	OSS3	OSS2	OSS1	OSS0

Bit 6 (TIMERSC): TCC, TMR1, TMR2, TMR3 clock source select

0: Fs. Fs is the sub frequency for WDT internal RC time base

1: Fm. Fm is the main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0: sub-oscillator (fs)

1: main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to activate after SLEP instruction.

0: IDLE="0"+SLEP instruction → sleep mode

1: IDLE="1"+SLEP instruction → idle mode

CPU Operation Mode

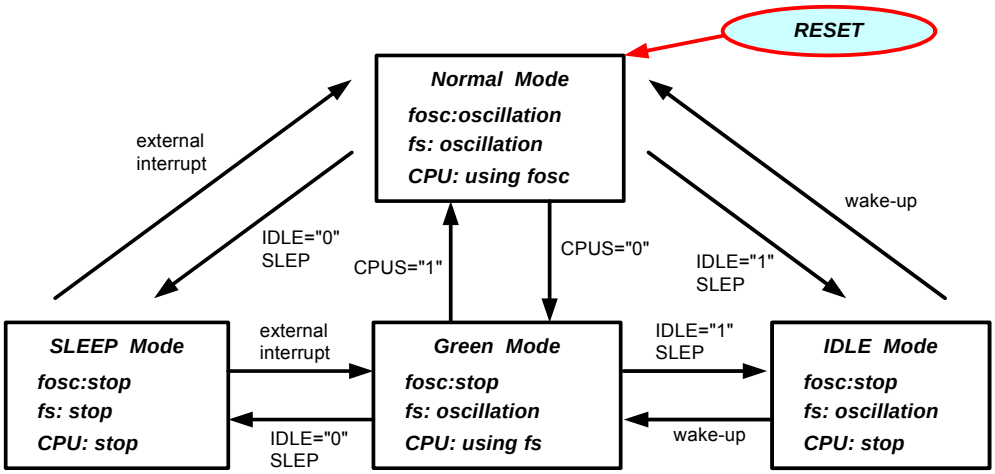


Figure 6-2 CPU Operation Mode

Bit 3 (OSS3): Output Sink Current Select for P67.

Bit 2 (OSS2): Output Sink Current Select for P66.

Bit 1 (OSS1): Output Sink Current Select for P51.

Bit 0 (OSS0): Output Sink Current Select for P50.

OSSx	VDD = 5V, Sink Current
0	20 mA (in GND+0.5V)
1	80 mA (in GND+1.5V)

6.1.18 Bank 1 R8 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

Bank 1 R8 register is both readable and writable.

Bit 7 (/PD57): Control bit used to enable pull-down of the P57 pin

0: Enable internal pull-down

1: Disable internal pull-down (Default)

Bit 6 (/PD56): Control bit used to enable pull-down of the P56 pin.

Bit 5 (/PD55): Control bit used to enable pull-down of the P55 pin.

Bit 4 (/PD54): Control bit used to enable pull-down of the P54 pin.

Bit 3 (/PD53): Control bit used to enable pull-down of the P53 pin.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

6.1.19 Bank 1 R9 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	/PD74	/PD73	/PD72	/PD71	/PD70

Bank 1 R9 register is both readable and writable

Bit 4 (/PD74): Control bit used to enable pull-down of the P74 pin.

0: Enable internal pull-down

1: Disable internal pull-down (Default)

Bit 3 (/PD73): Control bit used to enable pull-down of the P73 pin.

Bit 2 (/PD72): Control bit used to enable pull-down of the P72 pin.

Bit 1 (/PD71): Control bit used to enable pull-down of the P71 pin.

Bit 0 (/PD70): Control bit used to enable pull-down of the P70 pin.

6.1.20 Bank 1 RA (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD67	/OD66	/OD65	/OD64	/OD63	/OD62	/OD61	/OD60

Bank 1 RA register is both readable and writable.

Bit 7 (/OD67): Control bit used to enable open-drain of the P67 pin.

0: Enable open-drain output

1: Disable open-drain output

Bit 6 (/OD66): Control bit used to enable open-drain output of the P66 pin.

Bit 5 (/OD65): Control bit used to enable open-drain output of the P65 pin.

Bit 4 (/OD64): Control bit used to enable open-drain output of the P64 pin.

Bit 3 (/OD63): Control bit used to enable open-drain output of the P63 pin.

Bit 2 (/OD62): Control bit used to enable open-drain output of the P62 pin.

Bit 1 (/OD61): Control bit used to enable open-drain output of the P61 pin.

Bit 0 (/OD60): Control bit used to enable open-drain output of the P60 pin.

6.1.21 Bank 1 RB (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	/OD74	/OD73	/OD72	/OD71	/OD70

Bank 1 RB register is both readable and writable.

Bit 4 (/OD74): Control bit used to enable open-drain of the P74 pin.

0: Enable open-drain output

1: Disable open-drain output

Bit 3 (/OD73): Control bit used to enable open-drain output of the P73 pin.

Bit 2 (/OD72): Control bit used to enable open-drain output of the P72 pin.

Bit 1 (/OD71): Control bit used to enable open-drain output of the P71 pin.

Bit 0 (/OD70): Control bit used to enable open-drain output of the P70 pin.

6.1.22 Bank 1 RC (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH63	/PH62	/PH61	/PH60

Bank 1 RC register is both readable and writable.

Bit 7 (/PH57): Control bit used to enable the pull-high function of P57 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable pull-high of the P56 pin.

Bit 5 (/PH55): Control bit used to enable pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable pull-high of the P54 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

6.1.23 Bank 1 RD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	/PH74	/PH73	/PH72	/PH71	/PH70

Bank 1 RD register is both readable and writable.

Bit 7 (/PH74): Control bit used to enable pull-high of the P74 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin.

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin.

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin.

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin.

6.1.24 Bank 1 RE (Option Control bits, Only for ICE)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TYPE1	TYPE0	LVR1	LVR0	RCM1	RCM0	-	-

Bank 1 RE register is both readable and writable.

Bits 7~6 (TYPE1 ~ TYPE0): Type selection for EM78P346N.

TYPE1, TYPE0	Selection No.
11	EM78P346N-24Pin (Default)
10	EM78P346N-24Pin
01	EM78P346N-20Pin
00	EM78P346N-18Pin

Bits 5~4 (LVR1 ~ LVR0): Low Voltage Reset Enable bits.

LVR1, L VR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.7V	3.9V
00	4.1V	4.3V

Bit 3 and Bit 2 (RCM1, RCM0): IRC mode select bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	1
0	0	455kHz

6.1.25 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: interrupt occurs at a rising edge of the INT pin

1: interrupt occurs at a falling edge of the INT pin

Bit 6 (INT): Interrupt Enable flag. This bit is readable only.

0: masked by DISI or hardware interrupt

1: enabled by the ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock. If P56 is used as I/O pin, TS must be 0.

1: transition on the TCC pin

Bit 4 (TE): TCC signal edge

0: increment if the transition from low to high takes place on the TCC pin

1: increment if the transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: prescaler disable bit. TCC rate is 1:1.

1: prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: *Tcc time-out period [1/Fosc × prescaler × 256 (Tcc cnt) ×* ***1 (CLK=2)****]*

Tcc time-out period [1/Fosc × prescaler × 256 (Tcc cnt) × ***1 (CLK=4)****]*

6.2.3 IOC50 ~ IOC70 (I/O Port Control Register)

"**0**" defines the relative I/O pin as output

"**1**" puts the relative I/O pin into high impedance

IOC50, **IOC60**, and **IOC70** registers are all readable and writable.

NOTE

Using the EM78P346N-18Pin and EM78P346N-20Pin type Bit 10 of the Code Option register (Word 0) must be set to "0". Using the EM78P346N-18Pin type, user must set an extra Bit 7 of IOC50 and Bit 0 of IOC70 to "0". Then the pin status must be set to "0". Following the rules will have no additional power consumption.

6.2.4 IOC80 (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0

Bit 7 (PWM3E): PWM3 enable bit

0: PWM3 is off (default value), and its related pin carries out the P53 function.

1: PWM3 is on, and its related pin is automatically set to output.

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. IF P53/PWM3/VREF acts as VREF analog input pin, then PWM3E must be "0".

The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 (PWM2E): PWM2 enable bit

0: PWM2 is off (default value), and its related pin carries out the P52 function.

1: PWM2 is on, and its related pin is automatically set to output.

Bit 5 (PWM1E): PWM1 enable bit

0: PWM1 is off (default value), and its related pin carries out the P51 function.

1: PWM1 is on, and its related pin is automatically set to output.

Bit 4: Unimplemented, read as '0'

Bit 3 (T1EN): TMR1 enable bit

0: TMR1 is off (default value)

1: TMR1 is on

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale	ICE346 Prescale
0	0	0	1:1 (default)	1:1 (default)
0	0	1	1:2	1:2
0	1	0	1:4	1:4
0	1	1	1:8	1:8
1	0	0	1:16	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

6.2.5 IOC90 (TMRCON: Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0

Bit 7 (T3EN): TMR3 enable bit

0: TMR3 is off (default value)

1: TMR3 is on

Bit 6 (T2EN): TMR2 enable bit

0: TMR2 is off (default value)

1: TMR2 is on

Bit 5 ~ Bit 3 (T3P2 ~ T3P0): TMR3 clock prescale option bits

T3P2	T3P1	T3P0	Prescale	ICE346 Prescale
0	0	0	1:1 (default)	1:1 (default)
0	0	1	1:2	1:2
0	1	0	1:4	1:4
0	1	1	1:8	1:8
1	0	0	1:16	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 2: Bit 0 (T2P2 ~ T2P0): TMR2 clock prescale option bits

T2P2	T2P1	T2P0	Prescale	ICE346 Prescale
0	0	0	1:1 (default)	1:1 (default)
0	0	1	1:2	1:2
0	1	0	1:4	1:4
0	1	1	1:8	1:8
1	0	0	1:16	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

6.2.6 IOCA0 (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	CPOUT	COS1	COS0

Bit 7 ~ Bit 3: Unimplemented, read as '0'

Bit 2 (CPOUT): the result of the comparator output

Bit 1 ~ Bit 0 (COS1 ~ COS0): Comparator/OP Select bits

COS1	COS0	Function Description
0	0	Comparator and OP are not used. P60 functions as normal I/O pin.
0	1	Used as Comparator and P60 functions as normal I/O pin
1	0	Used as Comparator and P60 funcions as Comparator output pin (CO)
1	1	Used as OP and P60 functions as OP output pin (CO)

NOTE

- *The CO and ADEO of the P60/ADE0/CO pins cannot be used at the same time.*
- *The P60/ADE0/CO pin priority is as follows:*

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADE0	P60

6.2.7 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

IOCB0 register is both readable and writable

Bit 7 (/PD7): Control bit is used to enable the pull-down of the P67 pin

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable pull-down of the P66 pin

Bit 5 (/PD5): Control bit used to enable pull-down of the P65 pin

Bit 4 (/PD4): Control bit used to enable pull-down of the P64 pin

Bit 3 (/PD3): Control bit used to enable pull-down of the P63 pin

Bit 2 (/PD2): Control bit used to enable pull-down of the P62 pin

Bit 1 (/PD1): Control bit used to enable pull-down of the P61 pin

Bit 0 (/PD0): Control bit used to enable pull-down of the P60 pin

6.2.8 IOCC0 (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0

IOCC0 register is both readable and writable.

Bit 7 (OD7): Control bit used to enable open-drain output of the P57 pin.

0: Enable open-drain output

1: Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain output of the P56 pin.

Bit 5 (OD5): Control bit used to enable open-drain output of the P55 pin.

Bit 4 (OD4): Control bit used to enable open-drain output of the P54 pin.

Bit 3 (OD3): Control bit used to enable open-drain output of the P53 pin.

Bit 2 (OD2): Control bit used to enable open-drain output of the P52 pin.

Bit 1 (OD1): Control bit used to enable open-drain output of the P51 pin.

Bit 0 (OD0): Control bit used to enable open-drain output of the P50 pin.

6.2.9 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

IOCD0 register is both readable and writable.

Bit 7 (/PH7): Control bit used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH5): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH4): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH3): Control bit used to enable pull-high of the P53 pin.

Bit 2 (/PH2): Control bit used to enable pull-high of the P52 pin.

Bit 1 (/PH1): Control bit used to enable pull-high of the P51 pin.

Bit 0 (/PH0): Control bit used to enable pull-high of the P50 pin.

6.2.10 IOCE0 (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	PSWE	PSW2	PSW1	PSW0	“0”	“0”

Bit 7 (WDTE): Control bit is used to enable Watchdog Timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit is used to define the function of the P50 (/INT) pin

0: P50, normal I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P50 (Bit 0 of IOC50) must be set to "1"

NOTE

- *When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 5 (R5). Refer to Figure 6-5 (I/O Port and I/O Control Register Circuit for P50 (/INT)) under Section 6.4 (I/O Ports).*
- *EIS is both readable and writable.*

Bit 5 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit. WDT rate is 1:1

1: prescaler enable bit. WDT rate is set at Bit 4~Bit 2.

Bit 4 ~ Bit 2 (PSW2 ~ PSW0): WDT prescaler bits.

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 1 ~ Bit 0: Unimplemented, read as ‘0’

6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE	PWM3IE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

NOTE

- *IOCF0 register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-9 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 7 (CMPIE): CMPIF interrupt enable bit

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter next instruction, the CMPIE bit must be set to “Enable”.

Bit 6 (PWM3IE): PWM3IF interrupt enable bit

0: Disable PWM3 interrupt

1: Enable PWM3 interrupt

Bit 5 (PWM2IE):PWM2IF interrupt enable bit

0: Disable PWM2 interrupt

1: Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit

0: Disable PWM1 interrupt

1: Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When the ADC Complete status is used to enter an interrupt vector or to enter next instruction, the ADIE bit must be set to “Enable”.

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

If Port 6 Input Status Change Interrupt is used to enter an interrupt vector or to enter next instruction, the ICIE bit must be set to “Enable”.

Bit 0 (TCIE): TCIF interrupt enable bit.

0: Disable TCIF interrupt

1: Enable TCIF interrupt

6.2.12 IOC51 (PRD1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Time Period)

The contents of IOC51 are the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period. Most Significant Bits (Bits 9, 8) of the Period Cycle of PWM1 in R-BANK1 R5<1, 0>.

6.2.13 IOC61 (PRD2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Time Period)

The contents of IOC61 are the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period. Most Significant Bits (Bits 9, 8) of the Period Cycle of PWM2 in R-BANK1 R5<3, 2>.

6.2.14 IOC71 (PRD3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Time Period)

The contents of IOC71 are the time period (time base) of PWM3. The frequency of PWM3 is the reverse of the period. Most Significant Bits (Bit 9, 8) of Period Cycle of PWM3 in R-BANK1 R5<5, 4>.

6.2.15 IOC81 (DT1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

6.2.16 IOC91 (DT2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

6.2.17 IOCA1 (DT3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Duty Cycle)

A specified value keeps the output of PWM3 to remain high until the value matches with TMR3.

6.2.18 IOCB1 (DTH: Most Significant Bits of PWM Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
“0”	“0”	PWM3[9]	PWM3[8]	PWM2[9]	PWM2[8]	PWM1[9]	PWM1[8]

Bit 7 and Bit 6: Unimplemented, read as ‘0’.

Bit 5 and Bit 4 (PWM3 [9], PWM3 [8]): Most Significant Bits of PWM3 Duty Cycle.

Bit 3 and Bit 2 (PWM2 [9], PWM2 [8]): Most Significant Bits of PWM2 Duty Cycle.

Bit 1 and Bit 0 (PWM1 [9], PWM1 [8]): Most Significant Bits of PWM1 Duty Cycle.

6.2.19 IOCC1 (TMR1L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM1 Timer)

The contents of IOCC1 are read-only.

6.2.20 IOCD1 (TMR2L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM2 Timer)

The contents of IOCD1 are read-only.

6.2.21 IOCE1 (TMR3L: Least Significant Byte (Bit 7 ~ Bit 0) of PWM3 Timer)

The contents of IOCE1 are read-only.

6.2.22 IOCF1 (TMRH: Most Significant Bits of PWM Timer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	TMR3[9]	TMR3[8]	TMR2[9]	TMR2[8]	TMR1[9]	TMR1[8]

The contents of IOCF1 are read-only.

Bit 7 and Bit 6: Unimplemented, read as '0'.

Bit 5 and Bit 4 (TMR3 [9], TMR3 [8]): Most Significant Bits of PWM3Timer

Bit 3 and Bit 2 (TMR2 [9], TMR2 [8]): Most Significant Bits of PWM2Timer

Bit 1 and Bit 0 (TMR1 [9], TMR1 [8]): Most Significant Bits of PWM1Timer

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PWR0 ~ PWR2 bits of the IOCE0 register are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will increment by 1 at the main oscillator (without prescaler). Referring to Figure 6-3, if the TCC signal source is from the external clock input, TCC will increment by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK.

NOTE

The internal TCC will stop running when sleep mode occurs. However, during AD conversion, when TCC is set to "SLEP" instruction, if the ADWE bit of RE register is enabled, the TCC will keep on running.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. Refer to WDTE bit of IOCE0 register (Section 6.2.10)

6.2.10 ***IOCE0 (WDT Control Register)*** With no prescaler, the WDT time-out duration is approximately 18 ms.[1]

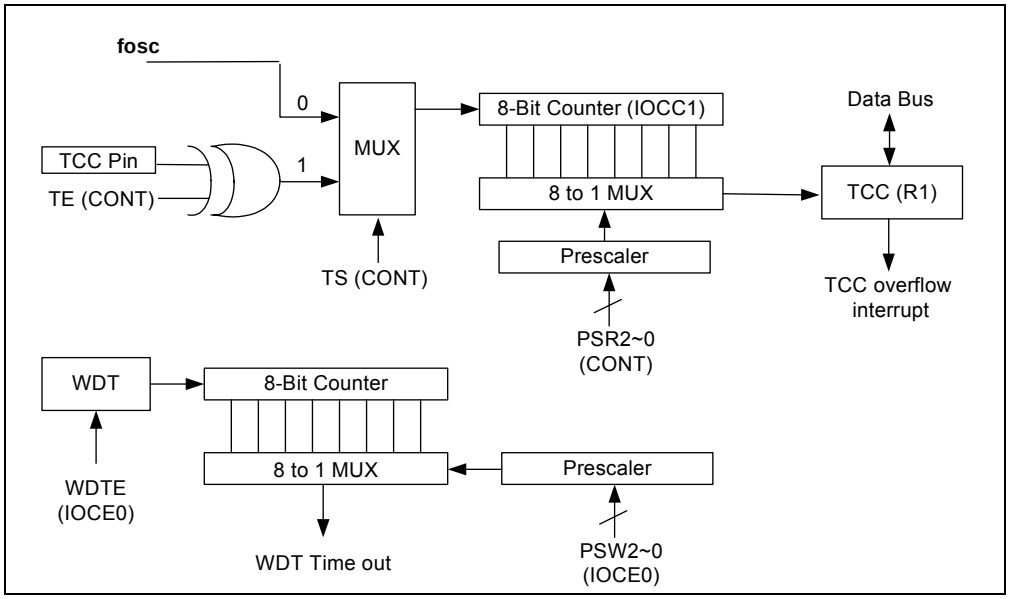
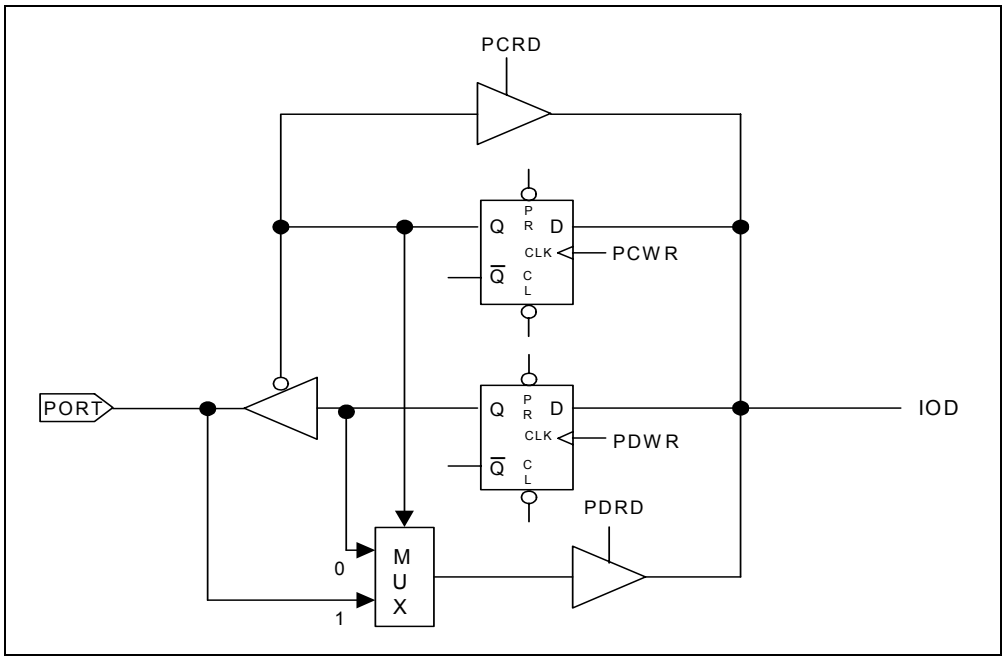


Figure 6-3 TCC and WDT Block Diagram

[1] VDD=5V, Setup time period = 16.5ms ± 5%.
VDD=3V, Setup time period = 18ms ± 5%.

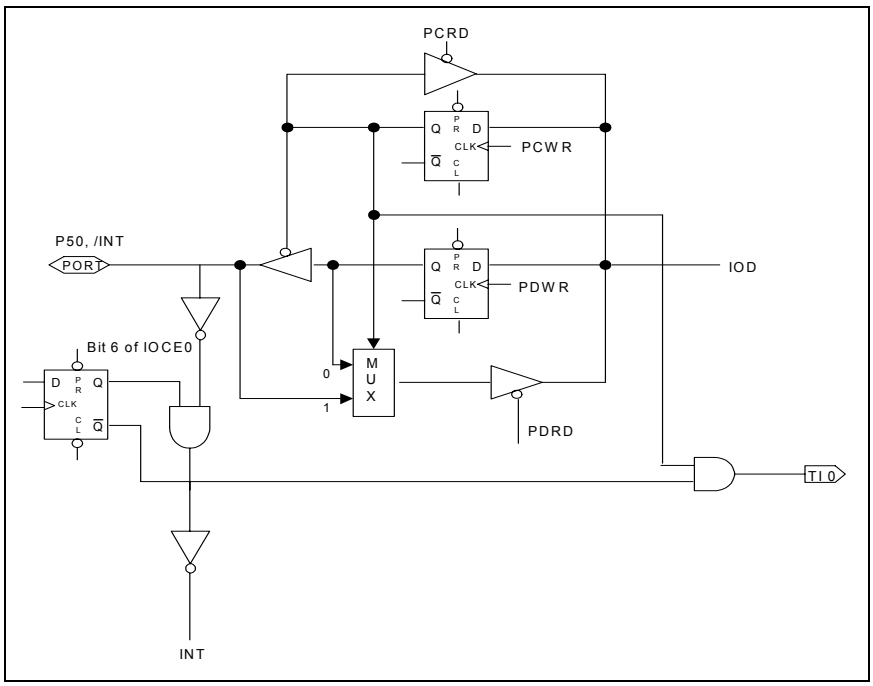
6.4 I/O Ports

The I/O registers (Port 5, Port 6, and Port 7) are bidirectional tri-state I/O ports. The Pull-high, Pull-down, and Open-drain functions can be set internally by IOCB0, IOCC0, and IOCD0 respectively. Port 6 features an input status change interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC50 ~ IOC70). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 6-4, 6-5, and 6-6 respectively. Port 6 with Input Change Interrupt/ Wake-up is shown in Figure 6-6.



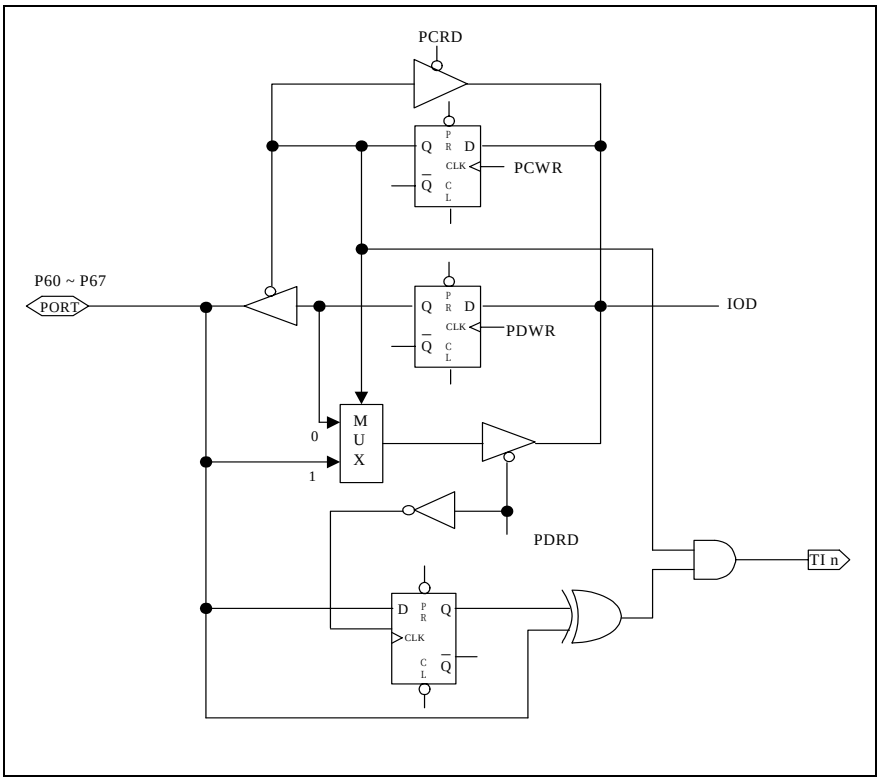
Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-4 /O Port and I/O Control Register Circuit for Port 5 and Port



Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-5 I/O Port and I/O Control Register Circuit for P50 (/INT)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-6 I/O Port and I/O Control Register Circuit for Port 6

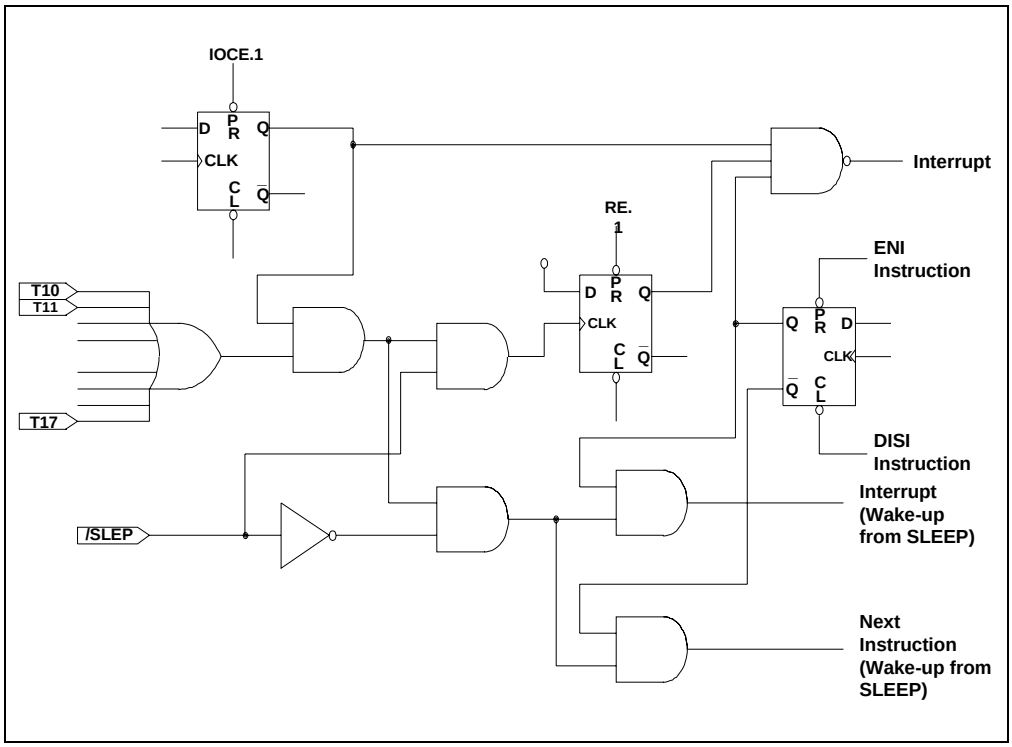


Figure 6-7 Port 6 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE=1)	4. Enable wake-up bit (Set RE ICWE=1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF0 ICIE=1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (006H)
	2. IF "DISI" → Next instruction

(3) Interrupt
(a) Before Port 6 pin change
1. Read I/O Port 6 (MOV R6, R6)
2. Execute "ENI" or "DISI"
3. Enable interrupt (Set IOCF0 ICIE = 1)
(b) After Port 6 pin changed (interrupt)
1. IF "ENI" → Interrupt vector (006H)
2. IF "DISI" → Next instruction

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events**:**

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18ms[2] after a reset is detected. When in LXT mode, the Reset Time is 2s~3s. Once a reset occurs, the following functions are performed (the initial Address is 000h).

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 and upper two bits of R4 are cleared.
- The CONT register bits are set to all "1" except for Bit 6 (INT flag).
- The IOCB0 register bits are set to all "1"
- The IOCC0 register bits are set to all "1"
- The IOCD0 register bits are set to all "1"
- Bit 7 of the IOCE0 register is set to "1", and Bits 6~0 are cleared
- Bits 0~6 of RF register and Bits 0~6 of IOCF0 register are cleared

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator, TCC, Timer 1, Timer 2, and Timer 3 are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 6 input status changed (if ICWE is enabled)

Case 4 Comparator output status change (if CMPWE is enabled)

Case 5 AD conversion completed (if ADWE is enabled)

Case 6 Low Voltage Detector (if LVDWE is enabled)

[2] VDD=5V, WDT Time-out period = 16.5ms ± 5%.
VDD=3V, WDT Time-out period = 18ms ± 5%.

The first two cases (Cases 1 and 2) will cause the EM78P346N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3~Case 6 are considered a continuation of program execution and a global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x06 (Case 3), 0x0F (Case 4), 0x0C (Case 5), and 0x1B (Case 6) after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up.

Only one of Cases 1 to 6 can be enabled before entering into sleep mode. That is:

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P346N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details. In High Crystal mode, wake-up time is 0.8ms (HXT2, 4MHz), no matter what the oscillator type or mode is (except when it's in low Crystal mode). In low Crystal mode, wake-up time is 2s~3s.

Case [b] If Port 6 Input Status Change is used to wake up the EM78P346N and the ICWE bit of the RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P346N can be awakened only with Case 3. Wake-up time is dependent on oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators). In High Crystal mode, wake-up time is 0.8ms (HXT2, 4 MHz), no matter what the oscillator type or mode is (except when it's in low Crystal mode). In low Crystal mode, wake-up time is 2s~3s.

Case [c] If Comparator output status change is used to wake up the EM78P346N and the CMPWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P346N can be awakened only with Case 4.

Wake-up time is dependent on oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators). In High Crystal mode, wake-up time is 0.8ms (HXT2, 4MHz), no matter what the oscillator type or mode is (except when it's in low Crystal mode). In low Crystal mode, wake-up time is 2s~3s.

Case [d] If AD conversion completed status is used to wake up the EM78P346N and the ADWE bit of the RE register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P346N can be awakened only with Case 5. The wake-up time is 15 TAD (ADC clock period).

Case [e] If Low voltage detector is used to wake up the EM78P346N and LVDWE bit of Bank 0-RE register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P346N can be awakened only with Case 6.

Wake-up time is dependent on the oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators). In High Crystal mode, wake-up time is 0.8ms (HXT2, 4 MHz), no matter what the oscillator type or mode is (except when it's in low Crystal mode). In low Crystal mode, wake-up time is 2s~3s.

If Port 6 Input Status Change Interrupt is used to wake up the EM78P346N (as in Case [b] above), the following instructions must be executed before SLEP:

```
BC              R3, 7               ; Select Segment 0
MOV             A, @001110xxb       ; Select WDT prescaler and Disable WDT
IOW             IOCE0
WDTC                                ; Clear WDT and prescaler
MOV             R6, R6              ; Read Port 6
ENI (or DISI)                       ; Enable (or disable) global interrupt
MOV             A, @00000x1xb       ; Enable Port 6 input change wake-up bit
MOV             RE
MOV             A, @00000x1xb       ; Enable Port 6 input change interrupt
IOW             IOCF0
SLEP                                ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P346N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BC              R3, 7               ; Select Segment 0
MOV             A, @xxxxxx10b       ; Select a comparator and P60 act as CO pin
IOW             IOCA0
MOV             A, @001110xxb       ; Select WDT prescaler and Disable WDT
IOW             IOCE0
WDTC                                ; Clear WDT and prescaler
ENI (or DISI)                       ; Enable (or disable) global interrupt
MOV             A, @000001xxb       ; Enable comparator output status change
                                    ; wake-up bit
MOV             RE
MOV             A, @000001xxb       ; Enable comparator output status change
IOW             IOCF0               ; interrupt
SLEP                                ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories under Wake-up and Interrupt modes are summarized below.

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	×	Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enabled) or next instruction	Interrupt (if interrupt enabled) or next instruction
Port 6 pin change	If enable ICWE bit Wake-up+ interrupt (if interrupt enabled) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enabled) or next instruction	Interrupt (if interrupt enabled) or next instruction
TCC overflow interrupt	×	Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enabled) or next instruction	Interrupt (if interrupt enabled) or next instruction
AD conversion complete interrupt	If enable ADWE bit Wake-up + interrupt (if interrupt enabled) + next instruction **Fs and Fm don't stop**	If enable ADWE bit Wake-up + interrupt (if interrupt enabled) + next instruction **Fs and Fm don't stop**	× **Fs and Fm don't stop**	Interrupt (if interrupt enabled) or next instruction
Comparator interrupt	If enable CMPWE bit Wake-up + interrupt (if interrupt enabled) + next instruction	If enable CMPWE bit Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enabled) or next instruction	Interrupt (if interrupt enabled) or next instruction
PWMX (PWM1, PWM2, PWM3) (When TimerX matches PRDX)	×	Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enabled) or next instruction
Low Voltage Detector interrupt	If Enable LVDWE bit Wake-up + interrupt (if interrupt enabled) + next instruction	If Enable LVDWE bit Wake-up + interrupt (if interrupt enabled) + next instruction	Interrupt (if interrupt enabled) or next instruction	Interrupt (if interrupt enabled) or next instruction
WDT Time out	Reset	Reset	Reset	Reset
Low Voltage Reset	Reset	Reset	Reset	Reset

After wake up:

1. If interrupt is enabled → interrupt+ next instruction

2. If interrupt is disabled → next instruction

Signal	Sleep Mode	Normal Mode
TCC Overflow	N/A	**DISI + IOCF0 (TCIE) Bit 0 = 1**
		Next Instruction+ Set RF (TCIF) = 1
		ENI + IOCF0 (TCIE) Bit 0 = 1
		Interrupt Vector (0x09)+ Set RF (TCIF) = 1
Port 6 Input Status Change	**RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 0**	**IOCF0 (ICIE) Bit 1 = 0**
	Oscillator, TCC and TIMERX are stopped. Port 6 input status change wake up is invalid.	Port 6 input status change interrupt is invalid
	RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 1	
	Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status change wake up is invalid.	
	RE (ICWE) Bit 1 = 1, IOCF0 (ICIE) Bit 1 = 0	
	Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	
	RE (ICWE) Bit 1 = 1, DISI + IOCF0 (ICIE) Bit 1 = 1	**DISI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (ICIF) = 1
	RE (ICWE) Bit 1=1, ENI + IOCF0 (ICIE) Bit 1 = 1	**ENI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Interrupt Vector (0x06)+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x06)+ Set RF (ICIF)=1
INT Pin	N/A	**DISI + IOCF0 (EXIE) Bit 2 = 1**
		Next Instruction+ Set RF (EXIF) = 1
		ENI + IOCF0 (EXIE) Bit 2 = 1
		Interrupt Vector (0x03)+ Set RF (EXIF)=1
AD Conversion	**RE (ADWE) Bit3=0, IOCF0 (ADIE) Bit 3 = 0**	**IOCF0 (ADIE) Bit 1 = 0**
	Clear R9 (ADRUN) = 0, ADC is stopped, AD conversion wake up is invalid. Oscillator, TCC and TIMERX are stopped.	AD conversion interrupt is invalid.
	RE (ADWE) Bit 3 = 0, IOCF0 (ADIE) Bit 3 = 1	
	Set RF (ADIF) = 1, R9 (ADRUN) = 0, ADC is stopped, AD conversion wake up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (ADWE) Bit 3 = 1, IOCF0 (ADIE) Bit 3 = 0	
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	
	RE (ADWE) Bit 3 = 1, DISI + IOCF0 (ADIE) Bit 3 = 1	**DISI + IOCF0 (ADIE) Bit 3 = 1**
	Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	Next Instruction+ RF (ADIF) = 1
	RE (ADWE) Bit 3 = 1, ENI + IOCF0 (ADIE) Bit 3 = 1	**ENI + IOCF0 (ADIE) Bit 3 = 1**
	Wake-up+ Interrupt Vector (0x0C)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	Interrupt Vector (0x0C)+ Set RF (ADIF) = 1
PWMX (PWM1, PWM2, PWM3) (When TimerX matches PRDX)	N/A	**DISI + IOCF0 (PWMXIE)=1**
		Next Instruction+ Set RF (PWMXIF) = 1
		ENI + IOCF0 (PWMXIE)=1
		Interrupt Vector (0x012 or 0x15 or 0x18)+ Set RF (PWMXIF) = 1

Signal	Sleep Mode	Normal Mode
Comparator (Comparator Output Status Change)	**RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 7 = 0**	**IOCF0 (CMPIE) Bit 7 = 0**
	Comparator output status chang wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	Comparator output status change interrupt is invalid.
	RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 7 = 1	
	Set RF (CMPIF) = 1, Comparator output status change wake up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2 = 1, IOCF0 (CMPIE) Bit 7 = 0	
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2=1, DISI + IOCF0 (CMPIE) Bit 7 = 1	**DISI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Next Instruction+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (CMPIF) = 1
	RE (CMPWE) Bit 2 = 1, ENI + IOCF0 (CMPIE) Bit 7 = 1	**ENI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Interrupt Vector (0x012 or 0x15 or 0x18)+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x012 or 0x15 or 0x18)+ Set RF (CMPIF) = 1
Low Voltage Detector	**Bank 1-R6 (LVDWE) Bit 3 = 0, Bank1-R6 (LVDIE) Bit 4 = 0**	**Bank 1-R6 (LVDIE) Bit 3 = 0**
	Low voltage detector is invalid. Oscillator, TCC and TIMERX are stopped.	Low voltage detector is invalid.
	Bank 1-R6 (LVDWE) Bit 3 = 0, Bank 1-R6 (LVDIE) Bit 4 = 1	**Bank 1-R6 (LVDIE) Bit 4 = 0**
	Set Bank 0-RE (LVDIF) Bit 6 =1, Low voltage detector is invalid. Oscillator, TCC and TIMERX are stopped.	
	Bank 1-R6 (LVDWE) Bit 3 = 1, Bank 1-R6 (LVDIE) Bit 4 = 0	
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	
	Bank 1-R6 (LVDWE) Bit 3 = 1, DISI+ Bank 1-R6 (LVDIE) Bit 4 = 1	**DISI + Bank 1-R6 (LVDIE) Bit 4 = 1**
	Wake-up+ Next Instruction+ Set Bank 1 - R6 (LVDIF) Bit 3 = 1, Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set Bank 1-R6 (LVDIF) Bit 3 = 1
	Bank 1-R6 (LVDWE) Bit 3 = 1, ENI+ Bank 1-R6 (LVDIE) Bit 4 = 1	**ENI + Bank 1-R6 (LVDIE) Bit 4 =1**
	Wake-up+ Interrupt Vector (0x1B)+ Set Bank 1-R6 (LVDIF) Bit 3 = 1, Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x1B)+ Set Bank 1-R6 (LVDIF) Bit 3 = 1
WDT Time Out IOCE (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

6.5.1.2 Register Initial Values after Reset

The following summarizes the initialized values for registers.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Type	18p / 20p / 24p	–	–	–	–	–	–	–
		Power-on	0	1	1	1	1	1	1	1
		/RESET & WDT	0	1	1	1	1	1	1	1
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	–	–	C75	C74	C73	C72	C71	C70
		Type	–	–	–	18p / 20p	24p	18p / 20p	24p	18p / 20p	24p	18p / 20p	24p	18p / 20p	24p
		Power-on	0	0	1	0	1	0	1	0	1	0	1	0	1
		/RESET & WDT	0	0	1	0	1	0	1	0	1	0	1	0	1
		Wake-up from Pin Change	P	P	P	0	P	0	P	0	P	0	P	0	P
N/A	IOC80 (PWMCON)	Bit Name	PWM3E	PWM2E	PWM1E	–	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET &WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC90 (TMRCON)	Bit Name	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0 (CMPCON)	Bit Name	–	–	–	–	–	CPOUT	COS1	COS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0 (PDCR)	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCC0 (ODCR)	Bit Name	/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0 (PHCR)	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0 (WDTCR)	Bit Name	WDTE	EIS	PSWE	PSW2	PSW1	PSW0	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF0 (IMR)	Bit Name	CMPIE	PMW3IE	PMW2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (PRD1L)	Bit Name	PRD1[9]	PRD1[8]	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 (PRD2L)	Bit Name	PRD2[9]	PRD2[8]	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (PRD3L)	Bit Name	PRD3[9]	PRD3[8]	PRD3[7]	PRD3[6]	PRD3[5]	PRD3[4]	PRD3[3]	PRD3[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (DT1L)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (DT2L)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCA1 (DT3L)	Bit Name	DT3[7]	DT3[6]	DT3[5]	DT3[4]	DT3[3]	DT3[2]	DT3[1]	DT3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
N/A	IOCB1 (DT1H, 2H, 3H)	Bit Name	–	–	DT3[9]	DT3[8]	DT2[9]	DT2[8]	DT1[9]	DT1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC1 (TMR1L)	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD1 (TMR2L)	Bit Name	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE1 (TMR3L)	Bit Name	TMR3[7]	TMR3[6]	TMR3[5]	TMR3[4]	TMR3[3]	TMR3[2]	TMR3[1]	TMR3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF1 (TMR1H, 2H, 3H)	Bit Name	–	–	TMR3[9]	TMR3[8]	TMR2[9]	TMR2[8]	TMR1[9]	TMR1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from P Change	Jump to Address 0x08 or continue to execute next instruction							
0x03	R3 (SR)	Bit Name	IOCS	–	–	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	BS7	BS6	–	–	–	–	–	–
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 0 R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 0 R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	Bank 0 R7	Bit Name	-	-	P75	P74	P73	P72	P71	P70
		Power-on	0	0	1	1	1	1	1	1
		/RESET & WDT	0	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	Bank 0 R8 (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9	Bank 0 R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WD	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xA	Bank 0 RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WD	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xB	Bank 0 RB (ADDDATA)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WD	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xC	Bank 0 RC (ADDATA1H)	Bit Name	–	–	–	–	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WD	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xD	Bank 0 RD (ADDATA1L)	Bit Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WD	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 0 RE (WUCR)	Bit Name	–	–	–	–	ADWE	CMPWE	ICWE	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WD	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	Bank 0 RF (ISR)	Bit Name	CMPIF	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x5	Bank 1 R5 (PRDxL)	Bit Name	–	–	PRD3[9]	PRD3[8]	PRD2[9]	PRD2[8]	PRD1[9]	PRD1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x6	Bank 1 R6 (LVDCR)	Bit Name	–	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0
		Power-on	0	0	0	0	0	0	1	1
		/RESET & WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	Bank 1 R7 (OSSCR)	Bit Name	–	TIMERSC	CPUS	IDLE	OSS3	OSS 2	OSS 1	OSS 0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x8	Bank 1 R8 (PDCR)	Bit Name	/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	Bank 1 R9 (PDCR)	Bit Name	–	–	–	/PD74	/PD73	/PD72	/PD71	/PD70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xA	Bank 1 RA (ODCR)	Bit Name	/OD67	/OD66	/OD65	/OD64	/OD63	/OD62	/OD61	/OD60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xB	Bank 1 RB (ODCR)	Bit Name	–	–	–	/OD74	/OD73	/OD72	/OD71	/OD70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xC	Bank 1 RC (PHCR)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xD	Bank 1 RD (PHCR)	Bit Name	–	–	–	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 1 RE (OC, only for ICE)	Bit Name	TYPE1	TYPE0	LVR1	LVR0	RCM1	RCM0	–	–
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10~ 0x3F	R10 ~ R3F	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: ***"–"*** *= not used* ***"P"*** *= previous value before reset*
"u" *= unknown or don't care* ***"t"*** *= check "Reset Type" Table in Section 6.5.2*

6.5.1.3 Controller Reset Block Diagram

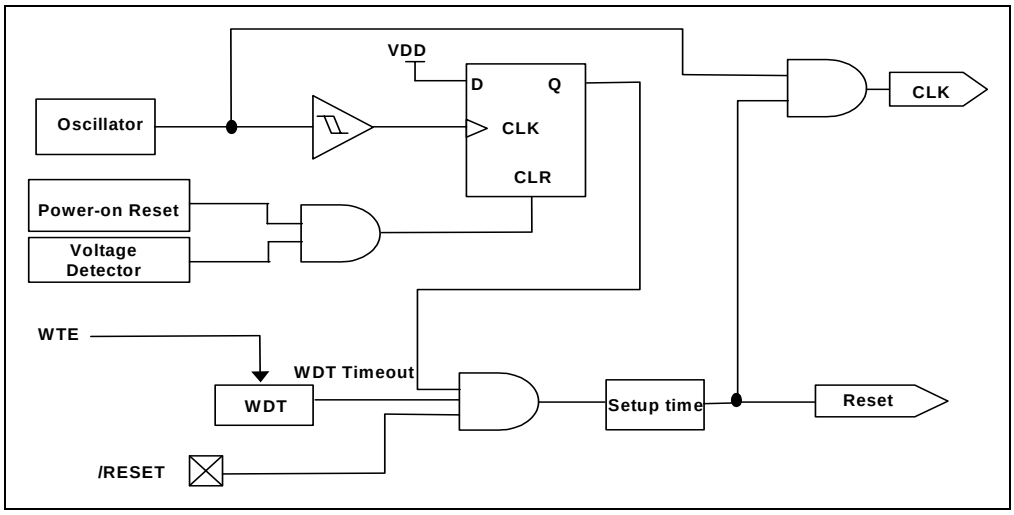


Figure 6-8 Controller Reset Block Diagram

6.5.2 T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operation mode	*P	*P
/RESET wake-up during Sleep mode	1	0
LVR during Operation mode	*P	*P
LVR wake-up during Sleep mode	1	0
WDT during Operation mode	0	1
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

**P: Previous status before reset*

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

**P: Previous value before reset*

6.6 Interrupt

The EM78P346N has six interrupts as listed below:

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External interrupt [(P50, /INT) pin]
4. Analog to Digital conversion completed
5. When TMR1/TMR2/TMR3 matches with PRD1/PRD2/PRD3 respectively in PWM
6. When the comparators output changes (for EM78P346N-20 Pin and 24 Pin only)
7. Low voltage detector Interrupt

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Port 6 Input Status Change Interrupt will wake up the EM78P346N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When wake up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than 8 system clock time) is eliminated as noise. However, under Low Crystal oscillator (LXT) mode the noise rejection circuit will be disabled. Edge selection is possible with INTE of CONT. When an interrupt is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H. Refer to the Word 1 Bits 8~7 (Section 6.13.2, *Code Option Register (Word 1)*) for digital noise rejection definition.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from interrupt vector address. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or of the ENI execution. Note that the result of RF will be the logic AND of RF and IOCF0 (refer to the figure). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

During the power source unstable situation, such as external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. At the time wherein the Vdd is unsettled, the voltage supply may be below working voltage. When the system supply voltage Vdd is below the working voltage, the IC kernel must keep all register status automatically.

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from Address 009, 012, 015, and 018H (TCC, Timer 1, Timer 2, and Timer 3 respectively).

When an interrupt is generated during Low Voltage Detection (if enabled), the next instruction will be fetched from Address 01 by the Low Voltage Detector.

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers will be saved by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

During a power source unstable situation, such as external power noise interference or EMS test condition, such will cause the power to vibrate fiercely. At the time Vdd is unsettled, the voltage supply may be below the working voltage. When the system voltage supply Vdd is below the working voltage, the IC kernel must keep all register status automatically.

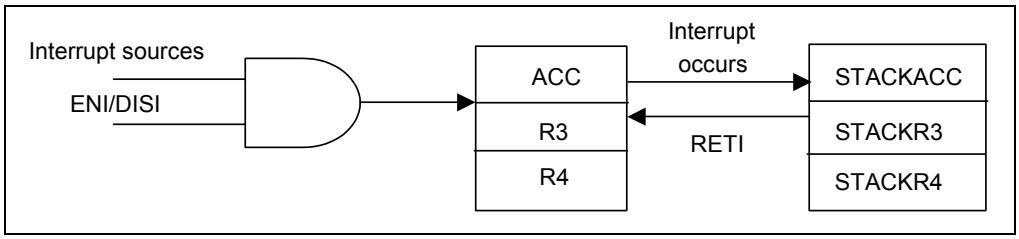


Figure 6-9 Interrupt Backup Diagram

In EM78P346N, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority*
003H	External interrupt	2
006H	Port 6 pin change	3
009H	TCC overflow interrupt	4
00CH	AD conversion complete interrupt	5
00FH	Comparator interrupt	6
012H	Timer 1 (PWM1) overflow interrupt	7
015H	Timer 2 (PWM2) overflow interrupt	8
018H	Timer 3 (PWM3) overflow interrupt	9
01BH	Low Voltage Detector interrupt	1

**Priority: 1 = highest ; 9 = lowest* priority

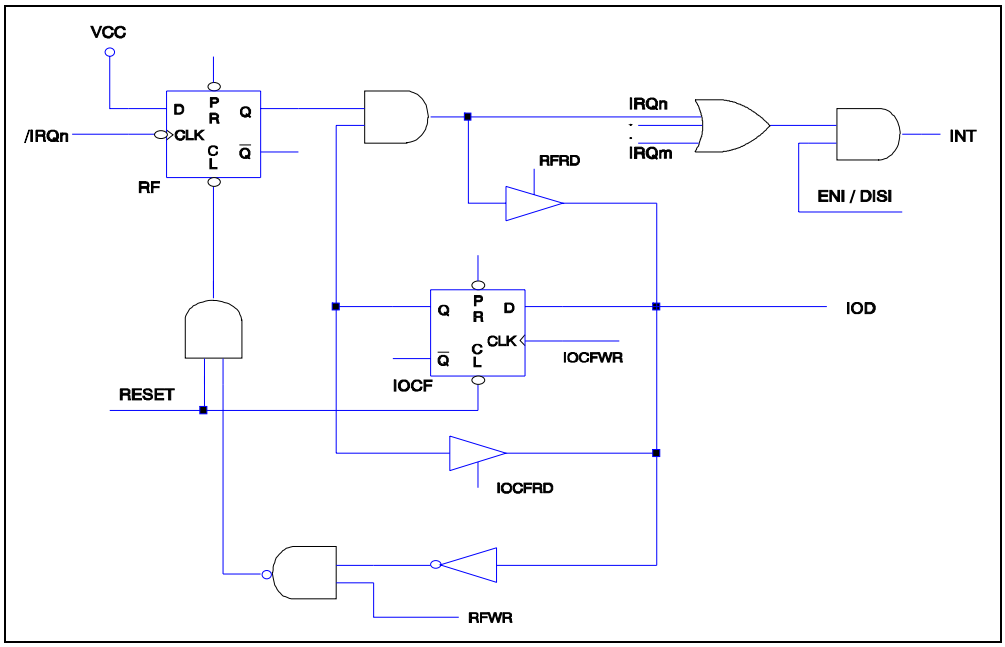


Figure 6-10 Interrupt Input Circuit

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, and ADOC/RA), three data registers (ADDATA1/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register bits. Connecting to the external VREF is more accurate than connecting to the internal VDD.

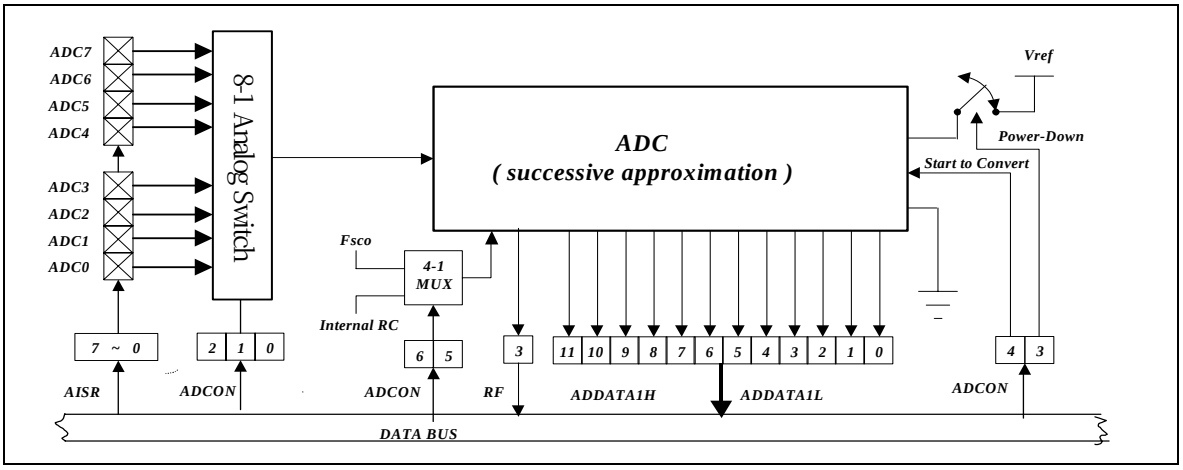


Figure 6-11 Analog-to-Digital Conversion Functional Block Diagram

6.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

6.7.1.1 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1
*Init_Value	0	0	0	0	0	0	0

The **AISR** register individually defines the Port 6 pins as analog inputs or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P67 pin
0: Disable ADC7, P67 functions as I/O pin
1: Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin
0: Disable ADC6, P66 functions as I/O pin
1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin
0: Disable ADC5, P65 functions as I/O pin
1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin
0: Disable ADC4, P64 functions as I/O pin
1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin
0: Disable ADC3, P63 functions as I/O pin
1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin
0: Disable ADC2, P63 functions as I/O pin
1: Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin
0: Disable ADC1, P61 acts as I/O pin
1: Enable ADC1 acts as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin
0: Disable ADC0, P60 functions as I/O pin
1: Enable ADC0 to function as analog input pin

NOTE

Take Note of the pin priority of the COS1 and COS0 bits of IOCA0 Control register when P60/ADE0 functions as analog input or as digital I/O. The Comparator/OP select bits are as shown in a table under Section 6.2.6.

The P60/ADE0/CO pin priority is as follows:

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADE0	P60

6.7.1.2 R9 (ADCON: ADC Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

**Init_Value: Initial value at power-on reset*

The **ADCON** register controls the operation of the AD conversion and determines which pin should be currently active.

Bit 7 (VREFS): The input source of the Vref of the ADC

0: The Vref of the ADC is connected to Vdd (default value), and the P53/VREF pin carries out the function of P53

1: The Vref of the ADC is connected to P53/VREF

NOTE

The P53/PWM3/VREF pin cannot be applied to PWM3 and VREF at the same time. If P53/PWM3/VREF functions as VREF analog input pin, then PWM3E must be "0".

The P53/PWM3/VREF pin priority is as follows:

P53/PWM3/VREF Pin Priority		
High	Medium	Low
VREF	PWM3	P53

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of ADC oscillator clock rate

00 = 1:16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1:CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Fosc/8	2 MHz

Bit 4 (ADRUN): ADC starts to RUN

0: reset on completion of the conversion. This bit cannot be reset though software.

1: an AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: switch off the resistor reference to conserve power even while the CPU is operating

1: ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = AN6/P66

111 = AN7/P67

These bits can only be changed when the ADIF bit and the ADRUN bit are both LOW.

6.7.1.3 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0: disable Calibration

1: enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits.

VOF[2]	VOF[1]	VOF[0]	EM78P346N	ICE346
0	0	0	0LSB	0LSB
0	0	1	2LSB	2LSB
0	1	0	4LSB	4LSB
0	1	1	6LSB	6LSB
1	0	0	8LSB	8LSB
1	0	1	10LSB	10LSB
1	1	0	12LSB	12LSB
1	1	1	14LSB	14LSB

Bit 2 ~ Bit 0: Unimplemented**,** read as '0'.

6.7.2 ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)

When AD conversion is completed, the result is loaded to the ADDATA, ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

6.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.7.4 AD Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P346N, the conversion time per bit is about 4μs. The table below shows the relationship between Tct and the maximum operating frequencies.

CKR1:CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4 μs)	15×4μs=60 μs (16.7kHz)
01	Fosc/4	1 MHz	250kHz (4 μs)	15×4μs=60 μs (16.7kHz)
10	Fosc/64	16 MHz	250kHz (4 μs)	15×4μs=60 μs (16.7kHz)
11	Fosc/8	2 MHz	250kHz (4 μs)	15×4μs=60 μs (16.7kHz)

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, Timer 1, Timer 2, Timer 3, and AD conversion.

AD Conversion is considered completed as determined by**:**

1. The ADRUN bit of R9 register is cleared to “0”.
2. Waking up from AD conversion (where it remains in operation during sleep mode).

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.7.6 Programming Process/Considerations

6.7.6.1 Programming Process

Follow these steps to obtain data from the ADC**:**

1. Write to the eight bits (ADE7: ADE0) on the R8 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R9/ADCON register to configure the AD module**:**
   a) Select ADC input channel (ADIS2**:**ADIS0)
   b) Define AD conversion clock rate (CKR1**:**CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for the ADRUN bit to be cleared to “0”.
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If the ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.7.6.2 Sample Demo Programs

A. Define a General Register

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
PORT6 == 6
RE== 0XE          ; Wake-up control resister
RF== 0XF          ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5      ; Control Register of Port 5
IOC60 == 0X6      ; Control Register of Port 6
CINT  == 0XF      ; Interrupt Control Register
```

C. ADC Control Register

```
ADDATA == 0xB     ; The contents are the results of ADC
AISR == 0x08      ; ADC Input select register
ADCON == 0x9      ;  7     6    5    4      3    2     1     0
                  ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

D. Define Bits in ADCON

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

E. Program Starts

```
ORG 0             ; Initial address
JMP INITIAL

ORG 0x08          ; Interrupt vector
;
;
;(User program section)
;
;
CLR RF               ; To clear the ADIF bit
BS ADCON, ADRUN      ; To start to execute the next AD conversion
                     ; if necessary
RETI
INITIAL:
MOV A,@0B00000001    ; To define P60 as an analog input
MOV AISR,A
MOV A,@0B00001000    ; To select P60 as an analog input channel,
                     ; and AD power on
MOV ADCON,A          ; To define P60 as an input pin and set
                     ; clock rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1   ; To define P50 as an input pin, and the others
IOW PORT6            ; are dependent on applications
MOV A, @0BXXXX1XXX   ; Enable the ADWE wake-up function of ADC, "X"
                     ; by application
MOV RE,A
MOV A, @0BXXXX1XXX   ; Enable the ADIE interrupt function of ADC,
                     ; "X" by application
IOW C_INT
ENI                  ; Enable the interrupt function

BS ADCON, ADRUN      ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

POLLING:
JBC ADCON, ADRUN     ; To check the ADRUN bit continuously;
JMP POLLING          ; ADRUN bit will be reset as AD conversion
                     ; is completed
;
;
; (User program section)
;
;
```

6.8 Dual Sets of PWM (Pulse Width Modulation)

6.8.1 Overview

In PWM mode, PWM1, PWM2, and PWM3 pins produce up to a 10-bit resolution PWM output (see. the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure 6-12 (*PWM Output Timing*) depicts the relationships between a time period and a duty cycle.

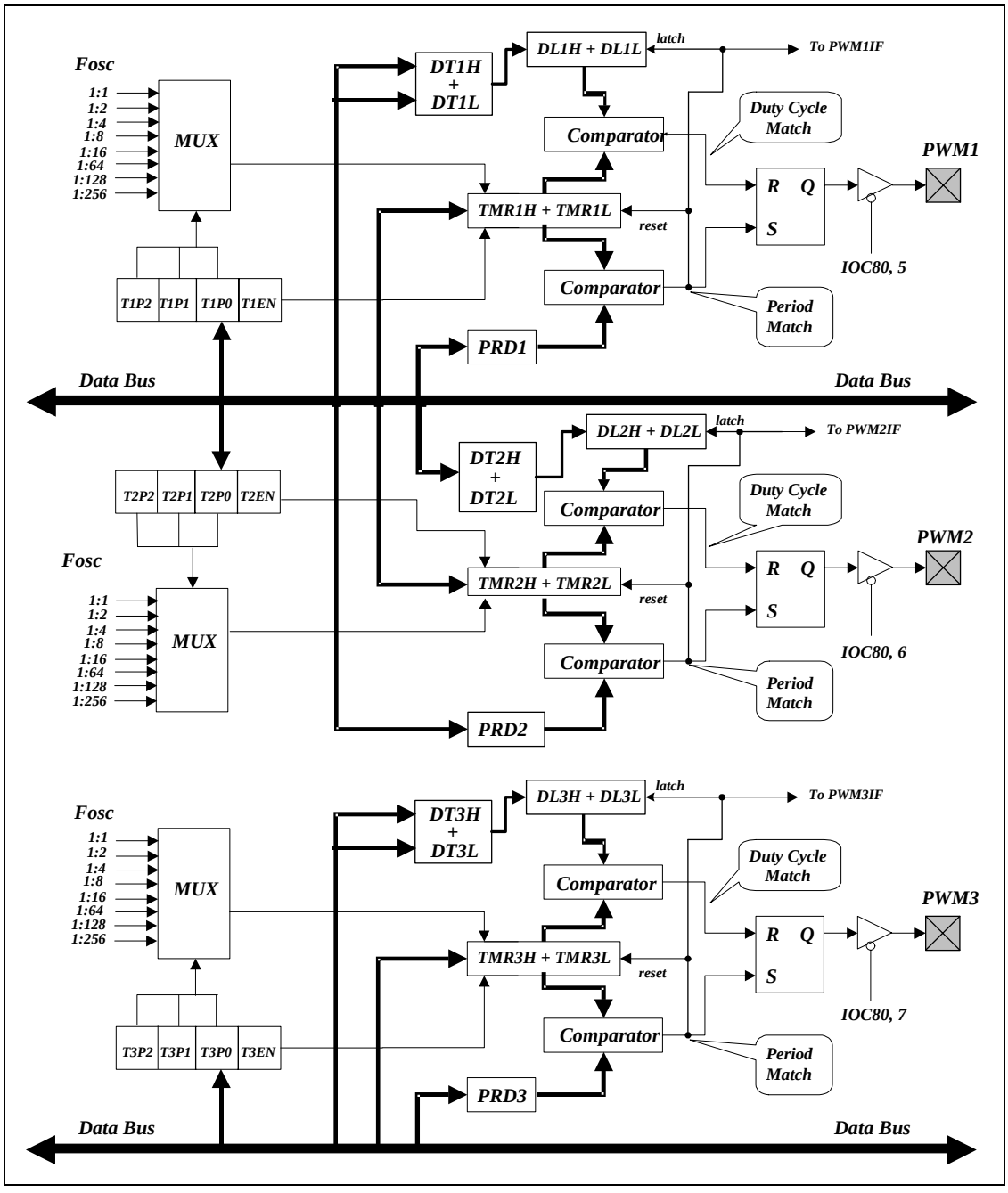


Figure 6-12 Three PWMs Functional Block Diagram

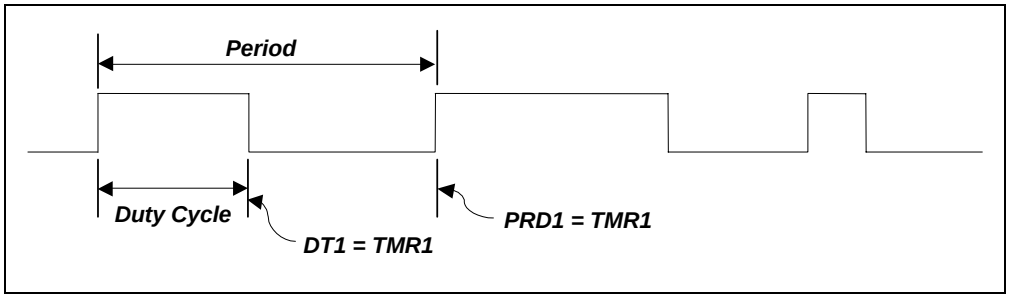


Figure 6-13 PWM Output Timing

6.8.2 Increment Timer Counter (TMRX: TMR1H/TWR1L, TMR2H /TWR2L, or TMR3H/TWR3L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, they can be turned off for power saving by setting the T1EN bit [IOC80<3>], T2EN bit [IOC90<6>] or T3EN bit [IOC90<7>] to “0”.

6.8.3 PWM Time Period (PRDX: PRD1 or PRD2)

The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle**:**

- TMRX is cleared
- The PWMX pin is set to 1
- The PWM duty cycle is latched from DT1/DT2/DT3 to DL1/DL2/DL3

NOTE

The PWM output will not be set, if the duty cycle is 0

- The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

Then

$$Period = (49 + 1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5\,\mu s$$

6.8.4 PWM Duty Cycle (DTX: DT1H/ DT1L, DT2H/ DT2L and DT3H/DT3L; DLX: DL1H/DL1L, DL2H/DL2L and DL3H/DL3L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of PRDX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle**:**

$$Duty\ cycle\ =\ (DTX)\ \times\ \left(\frac{1}{F_{OSC}}\right)\ \times\ (TMRX\ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

Then

$$Duty\ cycle\ =\ (10)\ \times\ \left(\frac{1}{4M}\right)\ \times\ 1\ =\ 2.5\,\mu s$$

6.8.5 Comparator X

Changing the output status while a match occurs will set the TMRXIF flag at the same time.

6.8.6 PWM Programming Process/Steps

Load PRDX with the PWM time period.

1. Load DTX with the PWM Duty Cycle.
2. Enable interrupt function by writing IOCF0, if required.
3. Set PWMX pin to be output by writing a desired value to IOC80.
4. Load a desired value to IOC51 with TMRX prescaler value and enable both PWMX and TMRX.

6.9 Timer

6.9.1 Overview

Timer 1 (TMR1), Timer 2 (TMR2), and Timer 3 (TMR3) (TMRX) are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1, Timer 2, and Timer 3 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, Timer 1, Timer 2 and Timer 3 will keep on running.

6.9.2 Functional Description

The following figure shows the TMRX block diagram followed by descriptions of its signals and blocks**:**

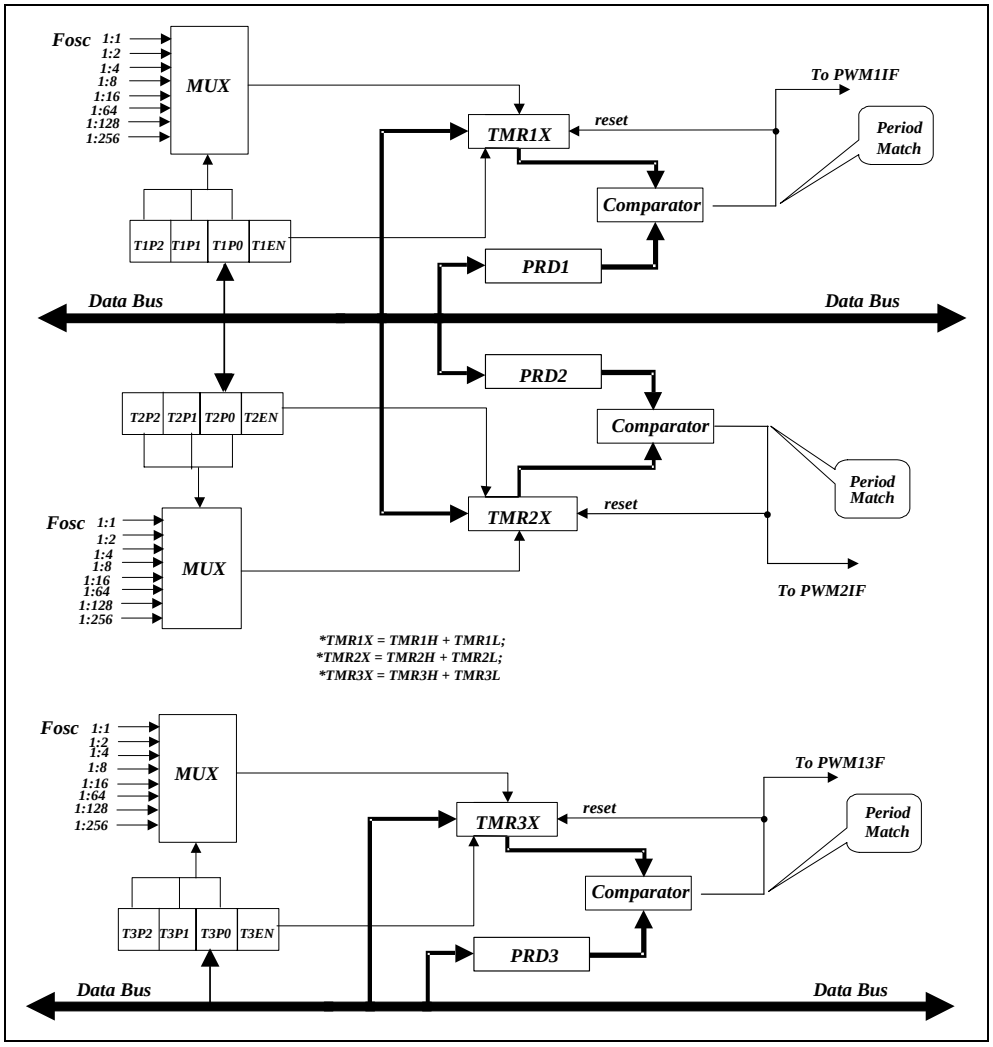


Figure 6-14 TMRX Block Diagram

Fosc: Input clock.

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0 / T3P2, T3P1 and T3P0): The options 1:1, 1:2, 1:4, 1:8, 1:16, 1:64, 1:128, and 1:256 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X, TMR2X and TMR3X (TMR1H/TWR1L, TMR2H/TMR2L, & TMR3H/TMR3L): Timer X register; TMRX is increased until it matches with PRDX, and then is reset to 1 (default valve).

PRDX (PRD1, PRD2 and PRD3): PWM time period register.

Comparator X (Comparator 1 and Comparator 2): Reset TMRX while a match occurs. The TMRXIF flag is set at the same time.

6.9.3 Programming the Related Registers

When defining TMRX, refer to the related registers of its operation as shown in the table below. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 ~ Bit 5 of the PWMCON register must be set to '0'.

6.9.3.1 Related Control Registers of TMR1, TMR2, and TMR3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC80	PWMCON/IOC80	PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0
IOC90	TMRCON/IOC90	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0

6.9.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration
2. Enable interrupt function by writing IOCF0, if required
3. Load a desired TMRX prescaler value to PWMCON and TMRCON and enable TMRX and disable PWMX

6.10 Comparator

The EM78P346N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up EM78P346N from sleep mode. The comparator circuit diagram is depicted in the figure below.

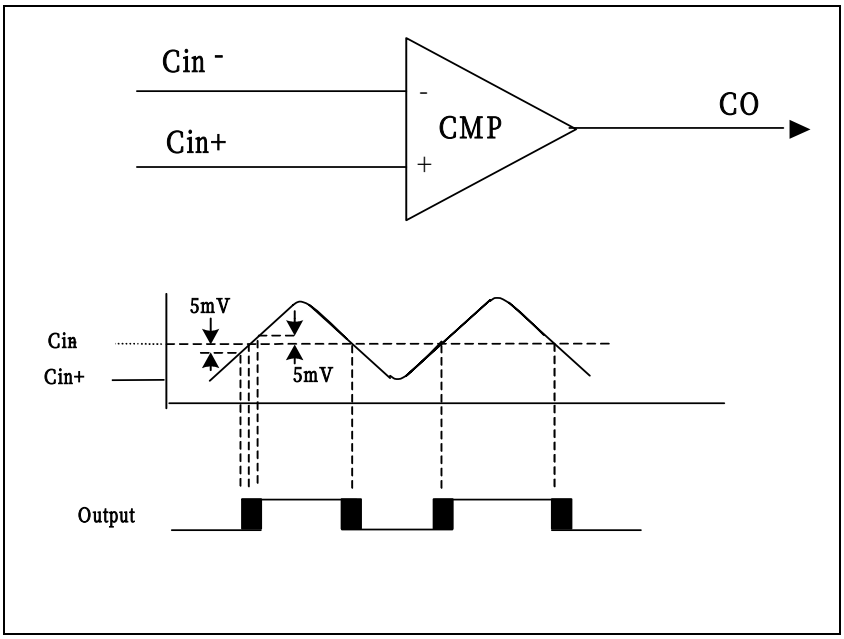


Figure 6-15 Comparator Circuit Diagram and Operating Mode

6.10.1 External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.10.2 Comparator Outputs

- The compared result is stored in the CMPOUT of IOCA0.
- The comparator outputs are sent to CO (P60) by programming Bit 1, Bit 0<COS1, COS0> of the IOCA0 register to <1, 0>. See Section 6.2.6, *IOCA0 (CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

NOTE

- *The CO and ADEO of the P60/ADE0/CO pins cannot be used at the same time.*
- *The P60/ADE0/CO pin priority is as follows:*

P60/ADE0/CO Priority		
High	Medium	Low
CO	ADE0	P60

The following figure shows the Comparator Output block diagram.

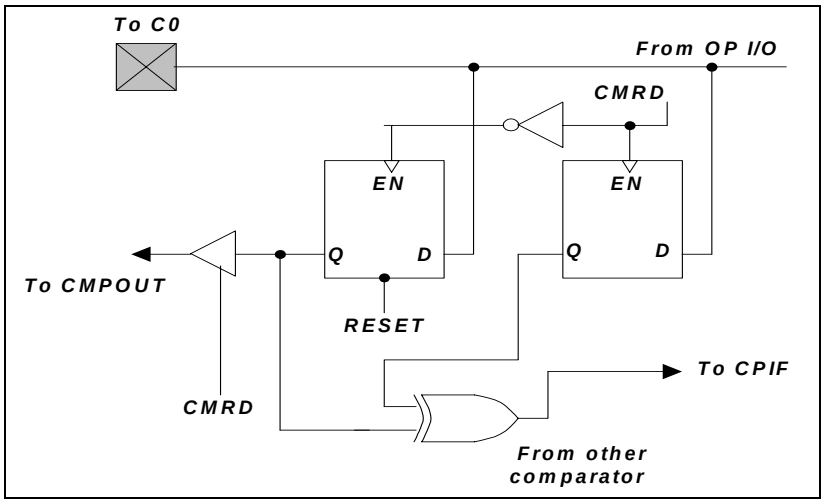


Figure 6-16 Comparator Output Configuration

6.10.3 Using Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output. In this case, the Schmitt trigger function can be disabled for power saving purposes, by setting Bit 1, Bit 0<COS1, COS0> of the IOCA0 register to <1, 1>. See Section 6.2.6, *IOCA0 (CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

6.10.4 Comparator Interrupt

- CMPIE (IOCF0.7) must be enabled for the "ENI" instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOCA0<2>.
- CMPIF (RF.7), the comparator interrupt flag, can only be cleared by software.

6.10.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78P346N can be operated in four different oscillator modes, such as High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator mode (IRC). One of the four modes can be selected by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P54/OSCO funcions as P54	0	0	0
ERC[1] (External RC oscillator mode); P54/OSCO functions as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P54/OSCO functions as P54	0	1	0
IRC[2] (Internal RC oscillator mode); P54/OSCO funtions as OSCO	0	1	1
LXT1 (Frequency range of LXT1 mode is 1MHz ~ 100kHz)	1	0	0
HXT1 (Frequency range of HXT mode is 12 MHz ~ 6 MHz)	1	0	1
LXT2 (Frequency range of XT mode is 32kHz)	1	1	0
HXT2 (Frequency range of XT mode is 6 MHz ~ 1 MHz.) (default)	1	1	1

[1] *In ERC mode, OSCI is used as oscillator pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4.*
[2] *In IRC mode, P55 is normal I/O pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4.*

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1	4
	4.5	16

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P346N can be driven by an external clock signal through the OSCO pin as illustrated below.

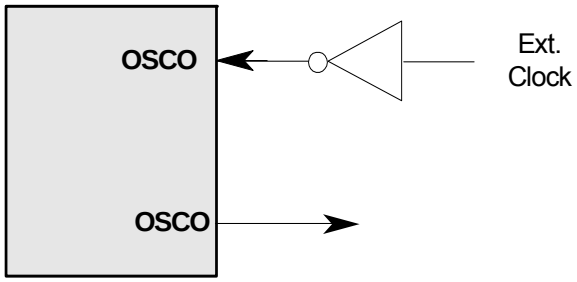


Figure 6-17 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-17 depicts such a circuit. The same applies to the HXT mode and the LXT mode.

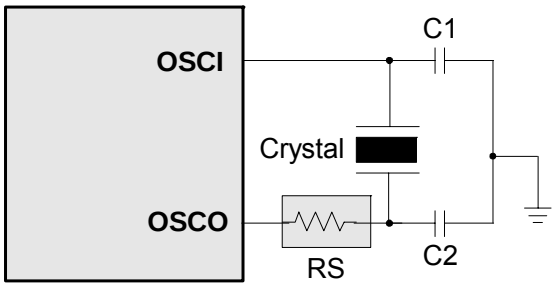


Figure 6-18 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.11.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-19 at right) could offer an effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

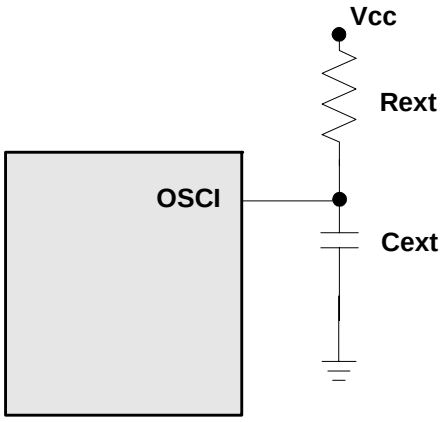


Figure 6-19 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be no less than 20 pF, and the value of Rext should not be greater than 1 MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot correctly discharge the capacitance current.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB is layout, have certain effect on the system frequency.

RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 Pf	3.3k	3.5 MHz	3.0 MHz
	5.1k	2.4 MHz	2.2 MHz
	10k	1.27 MHz	1.24 MHz
	100k	140kHz	143kHz
100 Pf	3.3k	1.21 MHz	1.18 MHz
	5.1k	805kHz	790kHz
	10k	420kHz	418kHz
	100k	45kHz	46kHz
300 Pf	3.3k	550kHz	526kHz
	5.1k	364kHz	350kHz
	10k	188kHz	185kHz
	100k	20kHz	20kHz

Note: *[1]: Measured based on DIP packages.*
[2]: The values are for design reference only.
[3]: The frequency drift is ± 30%

6.11.4 Internal RC Oscillator Mode

The EM78P346N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 1 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P346N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage (2.3V~3.9V~5.5V)	Process	Total
4 MHz	±5%	±5%	±4%	±14%
16 MHz	±5%	±5%	±4%	±14%
1 MHz	±5%	±5%	±4%	±14%
455kHz	±5%	±5%	±4%	±14%

These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

Table 1 Calibration Selection for Internal RC Mode

C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.1
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64

C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.9
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

* *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.12 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes to a steady state. The EM78P346N has a built-in Power-on Voltage Detector (POVD) with detection level range of 1.7V to 1.9V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.12.1 External Power-on Reset Circuit

The circuits shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow the Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Since the current leakage from the /RESET pin is approximately ± 5 μA, it is recommended that R should not be greater than 40K. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

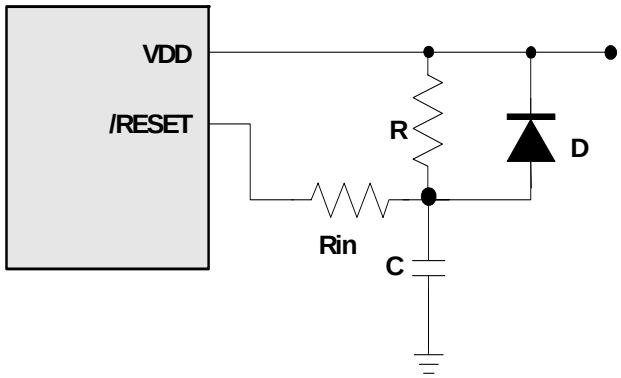


Figure 6-20 External Power-on Reset Circuit

6.12.2 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-21 and Figure 6-22 show how to create a protection circuit against residual voltage.

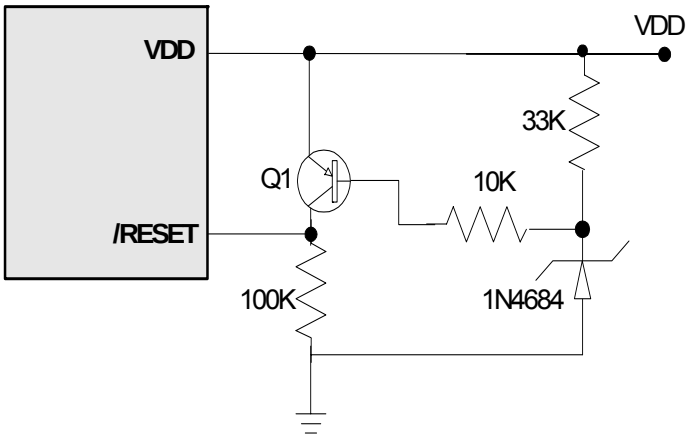


Figure 6-21 Residual Voltage Protection Circuit 1

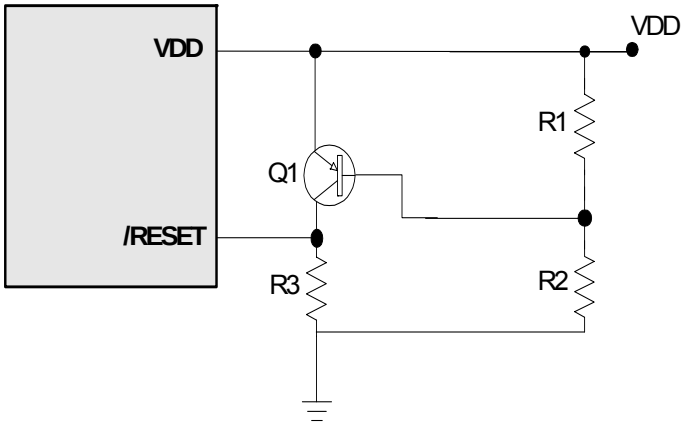


Figure 6-22 Residual Voltage Protection Circuit 2

6.13 Code Option

The EM78P346N has two Code option words and one Customer ID word that are not a part of the normal program memory.

Word 0	Word1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.13.1 Code Option Register (Word 0)

Word 0											
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2~0
Mnemonic	LVR1	LVR0	TYPE1	TYPE0	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	Protect
0	Low	Low	Low	Low	2 clocks	Enable	Low	Low	Low	Low	Enable
1	High	High	High	High	4 clocks	Disable	High	High	High	High	Disable

Bits 12~11 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.7V	3.9V
00	4.1V	4.3V

Bits 10~9 (TYPE1 ~ TYPE0): Type selection for EM78P346N.

TYPE1, TYPE0	Selection No.
11	EM78P346N-24Pin (Default)
10	EM78P346N-24Pin
01	EM78P346N-20Pin
00	EM78P346N-18Pin

Bit 8 (CLKS): Instruction time period option bit

0: Two oscillator time periods

1: Four oscillator time periods (default)

Refer to Section 6.15 for Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0: Enable

1: Disable (default)

Bits 6, 5 and 4 (OSC2, OSC1 and OSC0): Oscillator Modes Selection bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P54/OSCO functions as P54	0	0	0
ERC[1] (External RC oscillator mode); P54/OSCO functions as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P54/OSCO functions as P54	0	1	0
IRC[2] (Internal RC oscillator mode); P54/OSCO functions as OSCO	0	1	1
LXT1 (Frequency range of LXT1, mode is 1 MHz ~ 100kHz)	1	0	0
HXT1 (Frequency range of HXT mode is 16 MHz ~ 6 MHz)	1	0	1
LXT2 (Frequency range of XT mode is 32kHz)	1	1	0
HXT2 (Frequency range of XT mode is 6 MHz ~ 1 MHz) (default)	1	1	1

[1] *In ERC mode, OSCI is used as oscillator pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4.*

[2] *In IRC mode, P54 is normal I/O pin. OSCO/P54 is defined by Code Option Word 0 Bit 6 ~ Bit 4.*

Bit 3 (HLP): Power Consumption Selection

0: Low power consumption, apply to working frequency at 4MHz or below 4MHz

1: High power consumption, apply to working frequency above 4MHz

Bits 2 ~ 0 (Protect): Protect Bit

0: Enable

1: Disable

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	–	–	–	RCOUT	NRHL	NRE	–	C3	C2	C1	C0	RCM1	RCM0
0	–	–	–	Open_drain	8 / fc	Disable	–	Low	Low	Low	Low	Low	Low
1	–	–	–	System_clk	32 / fc	Enable	–	High	High	HIgh	High	High	High

Bit 12: fixed to "0"

Bits 11~10: Not used, set to "1" all the time

Bit 9 (RCOUT): System clock output enable bit in IRC or ERC mode

0: OSCO pin is open drain

1: OSCO output system clock (default)

Bit 8 (NRHL): Noise rejection high/low pulses defined bit. INT pin is a falling edge trigger

0: Pulses equal to 8/fc [s] is regarded as signal

1: Pulses equal to 32/fc [s] is regarded as signal (default)

NOTE

The noise rejection function is turned off under the LXT and sleep mode.

Bit 7 (NRE): Noise Rejection Enable

0: Disable noise rejection

1: Enable noise rejection (default). However under Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 6: Fixed to 0

Bits 5, 4, 3 and Bit2 (C3, C2, C1, and C0): Calibrator of internal RC mode. These bits must always be set to "1" only (auto calibration)

C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.1
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.9
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

* *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

Bit 1 and Bit 0 (RCM1 and RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	16
0	1	1
0	0	455kHz

6.13.3 Code Option and Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	NRM	RESETENB	–	×	×	×	×	×	×	×
0	–	–	–	MOD2	/RESET	–	Low	Low	Low	Low	Low	Low	Low
1	–	–	–	MOD1	P75	–	High	High	High	HIgh	High	High	High

Bits 12 ~ 11, 7: fixed to “1”

Bit 10: fixed to “0”

Bit 9 (NRM): Noise Reject Mode

0: Noise Reject Mode 2, for multi-time circuit usage, such as key scan and LED output

1: Noise Reject Mode 1. For General input or output usage **(Default)**

Bit 8 (RESETENB): Reset enable bit

0: P75/RESET is set as /RESET

1: P75/RESET is set as P75 (default)

Bits 6 ~ 0: Customer’s ID code

6.14 Low Voltage Detector

During the power source unstable situation, such like external power noise interference or EMS test condition, it will cause the power vibrate fierce. At the time Vdd is unsettled, the supply voltage may be below the working voltage. When system supply voltage Vdd is below the working voltage, the IC kernel must keep all register status automatically.

6.14.1 Low Voltage Reset

LVR property is set at Code Option Word 0, Bits 10, 9 detailed operation mode is as follows:

Word 0												
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
LVR1	LVR0	Type1	Type0	CLKS	ENWDTE	OSC2	OSC1	OSC0	HLP	PR2	PR1	PR0

Bits 12~11 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.7V	3.9V
00	4.1V	4.3V

6.14.2 Low Voltage Detector

LVD property setting at Registers RA, RE and detailed operation mode is as follows:

6.14.2.1 Bank 1 R6 (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0

NOTE

- *Bank 1 R6<4> register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the Bank 1 R6<4> to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag

LVDIF is reset to “0” by software or hardware.

Bit 5 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 4 of Bank 1 R6: 0: No interrupt occurs

1: there's interrupt request

Bit 4 (LVDIE): Low voltage Detector interrupt enable bit.

0: Disable Low voltage Detector interrupt.

1: Enable Low voltage Detector interrupt.

When detect low level voltage state is used to enter an interrupt vector or enter the next instruction, the LVDIE bit must be set to "Enable".

Bit 3 (LVDWE): Low Voltage Detect wake-up enable bit

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter interrupt vector or to wake-up IC from sleep with Low Voltage Detect running, the LVDWE bit must be set to "Enable".

Bit 2 (LVDEN): Low Voltage Detector Enable bit.

0: Disable Low voltage detector

1: Enable Low voltage detector

Bits 1~0 (LVD1:0): Low Voltage Detector level bits.

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.3V	0
		Vdd > 2.3V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	XX	NA	0

6.14.3 Programming Process

Follow these steps to obtain data from the LVD**:**

1. Write to the two bits (LVD1: LVD0) on the Bank 1-R6 (LVDCR) register to define the LVD level.
2. Set the LVDWE bit, if the wake-up function is employed.
3. Set the LVDIE bit, if the interrupt function is employed.
4. Write "ENI" instruction, if the interrupt function is employed.
5. Set LVDEN bit to 1
6. Write "SLEP" instruction or Polling /LVD bit.
7. Clear the interrupt flag bit (LVDIF) when Low Voltage Detected occurs.

The internal LVD module uses the internal circuit, and when the code option is set to enable the LVD module, the current consumption will increase to about 5 μA.

During sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detection point, the LVDIF bit will be set and the device will wake up from Sleep mode. The LVD interrupt flag is still set as the prior status.

When the system resets, the LVD flag will be cleared.

Figure 6-23 shows the LVD module to detect the external voltage situation.

When Vdd drops not below VLVD, LVDIF is kept at “0”. When Vdd drops below VLVD, LVDIF is set to “1”. If global ENI is enabled, LVDIF will be set to “1”, the next instruction will branch to an interrupt vector. The LVD interrupt flag is cleared to “0” by software.

When Vdds drops below VRESET and it is less than 80 μs, the system will keep all the register status and the system halts but oscillation is active. When Vdd drops below VRESET and it is more than 80 μs, a system reset will occur. Refer to Section 6.5.1 for detailed RESET description.

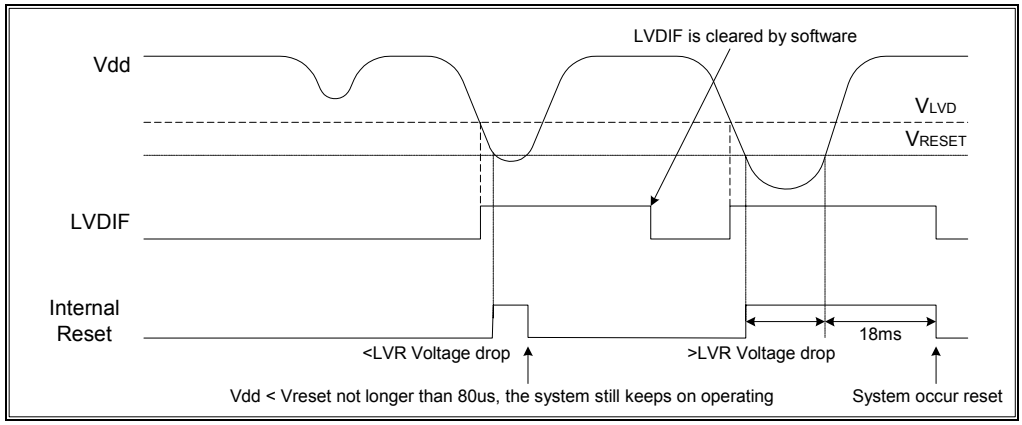


Figure 6-23 LVD Waveform Diagram

6.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, these instructions need one or two instruction cycles as determined by Code Option Register CYES bit.

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The following symbols are used in the Instruction Set table:

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bits 6 and 7 in R4 determine the selected register bank.

b *= Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1000 kkkk	1E9K	BANK k	K→R4(7:6)	None
1 1110 1000 kkkk	1EAK	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
1 1110 1000 kkkk	1EBK	LJMP k	Next instruction : k kkkk kkkk kkkk k→PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: [1] *This instruction is applicable to IOC50~IOCF0, IOC51 ~ IOCF1 only.*

[2] *This instruction is not recommended for RF operation.*

[3] *This instruction cannot operate under RF.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.5V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

Ta = 25°C, VDD = 5.0V, VSS = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768k	4	16	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	760	950	1140	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	–	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC,INT	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC,INT	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = 0.9VDD	–	-10	–	mA
IOL1	Output Low Voltage (Ports 5, 6,7)	VOL = 0.1VDD	–	20	–	mA
IOL2	Output Low Voltage (Ports 50, 51,66, 67)	VOL = 1.5V	–	70	–	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LVR1	Low voltage reset level	Ta= 25°C	2.11	2.4	2.69	V
		Ta= -40~85°C	1.84	2.4	2.95	V
LVR2	Low voltage reset level	Ta= 25°C	3.3	3.7	4.12	V
		Ta= -40~85°C	2.9	3.7	4.49	V
LVR3	Low voltage reset level	Ta= 25°C	3.66	4.1	4.53	V
		Ta= -40~85°C	3.26	4.1	4.91	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	-50	-75	-240	μA
IPL	Pull-low current	Pull-low active, Input pin at VDD	25	40	210	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	–	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	–	28	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), Output pin floating, WDT enabled	–	–	30	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	3.5	mA

■ **Internal RC Electrical Characteristics (Ta=25°C, VDD=5V, VSS=0V)**

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
16 MHz	25°C	5V	15.36 MHz	16 MHz	16.64 MHz
1 MHz	25°C	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25°C	5V	436.8kHz	455kHz	473.2kHz

■ **Internal RC Electrical Characteristics (Ta=-40~85°C, VDD=2.2V~5.5V, VSS=0V)**

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40°C ~85°C	2.2V~5.5V	3.44 MHz	4 MHz	4.56 MHz
16 MHz	-40°C ~85°C	2.2V~5.5V	13.76 MHz	16 MHz	18.24 MHz
1 MHz	-40°C ~85°C	2.2V~5.5V	0.86 MHz	1 MHz	1.14 MHz
455kHz	-40°C ~85°C	2.2V~5.5V	391.3kHz	455kHz	518.7kHz

8.1 AD Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=-40 to 85°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from Vdd)	750	850	1000	μA
	Ivref			-10	0	+10	μA
IAI2	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from VREF)	500	600	820	μA
	IVref			200	250	300	μA
IOP		OP current	VDD=5.0V, OP used Output voltage swing from 0.2V to 4.8V	450	550	650	μA
RN1		Resolution	ADREF=0, Internal VDD VDD=5.0V, VSS = 0.0V	–	9	–10	Bits
RN2		Resolution	ADREF=1, External VREF VDD=VREF=5.0V, VSS = 0.0V	–	11	12	Bits
LN1		Linearity error	VDD=2.5 to 5.5V Ta=25°C	0	±4	±8	LSB
LN2		Linearity error	VDD=2.5 to 5.5V Ta=25°C	0	±2	±4	LSB
DNL		Differential nonlinear error	VDD=2.5 to 5.5V Ta=25°C	0	±0.5	±0.9	LSB
FSE1		Full scale error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	±4	±8	LSB
FSE2		Full scale error	VDD=VREF=5.0V, VSS = 0.0V	±0	±2	±4	LSB
OE		Offset error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	±2	±4	LSB
ZAI		Recommended impedance of the analog voltage source	–	0	8	10	KΩ
TAD		ADC clock duration	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	4	–	–	μs
TCN		AD conversion time	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	15	–	15	TAD
ADIV		ADC OP input voltage range	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0	–	V_{AREF}	V
ADOV		ADC OP output voltage swing	VDD=V_{AREF}=5.0V, V_{ASS} =0.0V, RL=10KΩ	0	0.2	0.3	V
				4.7	4.8	5	
ADSR		ADC OP slew rate	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0.1	0.3	–	V/μs
PSR		Power Supply Rejection	VDD=5.0V±0.5V	±0	–	±2	LSB

Note: *1. These parameters are hypothetical (not tested) and are provided for design reference only.*

2. There is no current consumption when ADC is off other than minor leakage current.

3. AD conversion result will not decrease when an increase of input voltage and no missing code will result.

4. These parameters are subject to change without further notice.

8.2 Comparator (OP) Characteristics

Vdd = 5.0V, Vss=0V, Ta=-40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/μs
Vos	Input offset voltage	RL=5.1K, (Note 1)	1	5	10	mV
IVR	Input voltage range	Vdd =5.0V, V_{SS} = 0.0V	0	–	5	V
OVS	Output voltage swing	Vd =5.0V, V_{SS} = 0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Iop	Supply current of OP	–	250	350	500	μA
Ico	Supply current of Comparator	–	–	300	–	μA
PSRR	Power-supply Rejection Ratio for OP	Vdd= 5.0V, V_{SS} = 0.0V	50	60	70	dB
Vs	Operating range	–	2.5	–	5.5	V

Note: *1. These parameters are hypothetical (not tested) and are provided for design reference only.*

2. These parameters are subject to change without further notice.

8.3 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristic illustrated herein are not guaranteed for it accuracy. In some graphs, the data maybe out of the specified warranted operating range.

All the tests base on conditions described in DC/AC characteristics table. For full understanding, user should refer to the figures and tables provided.

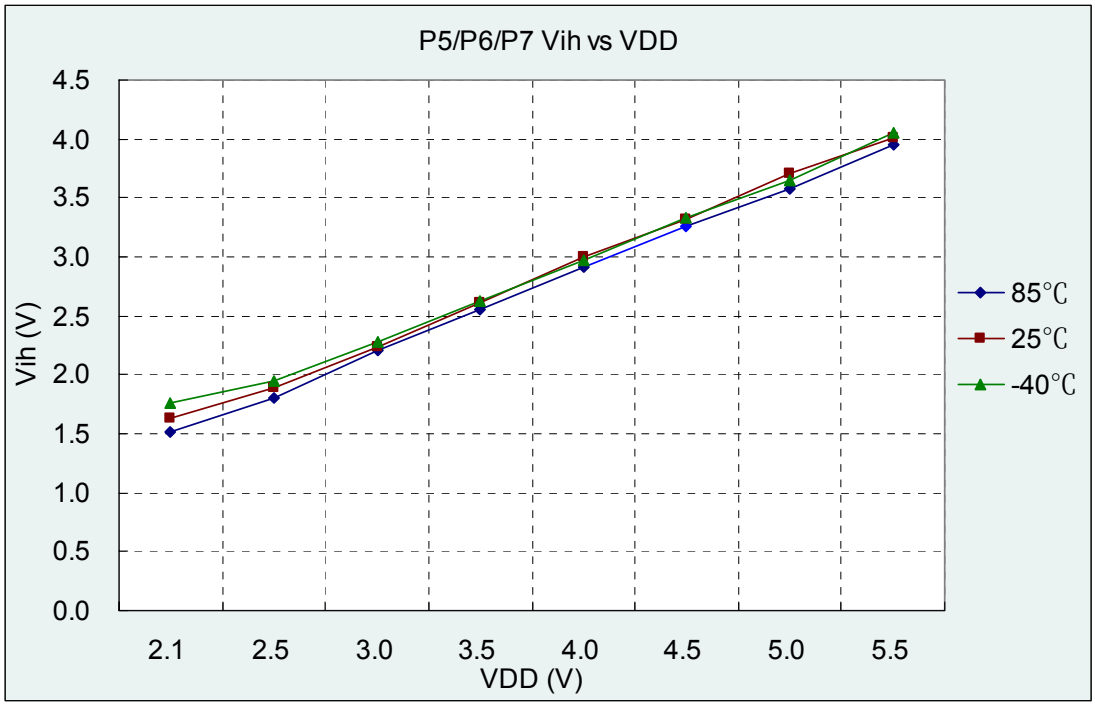


Figure 8-1 VIH vs. VDD

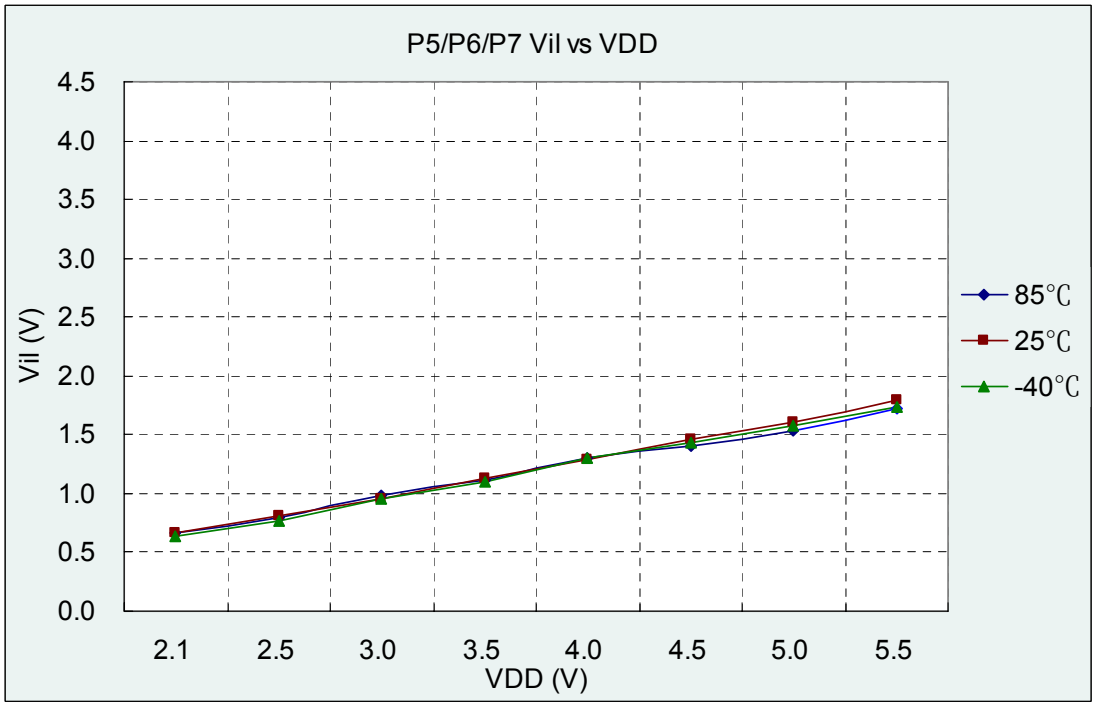


Figure 8-2 VIL vs. VDD

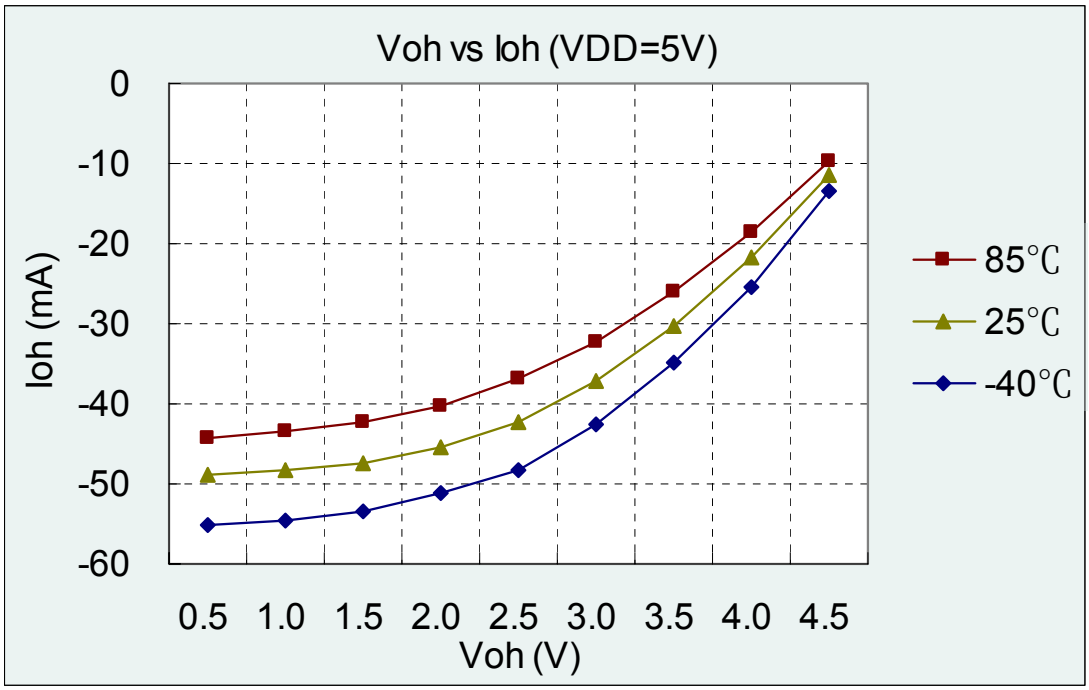


Figure 8-3 VOH vs. IOH (VDD=5V)

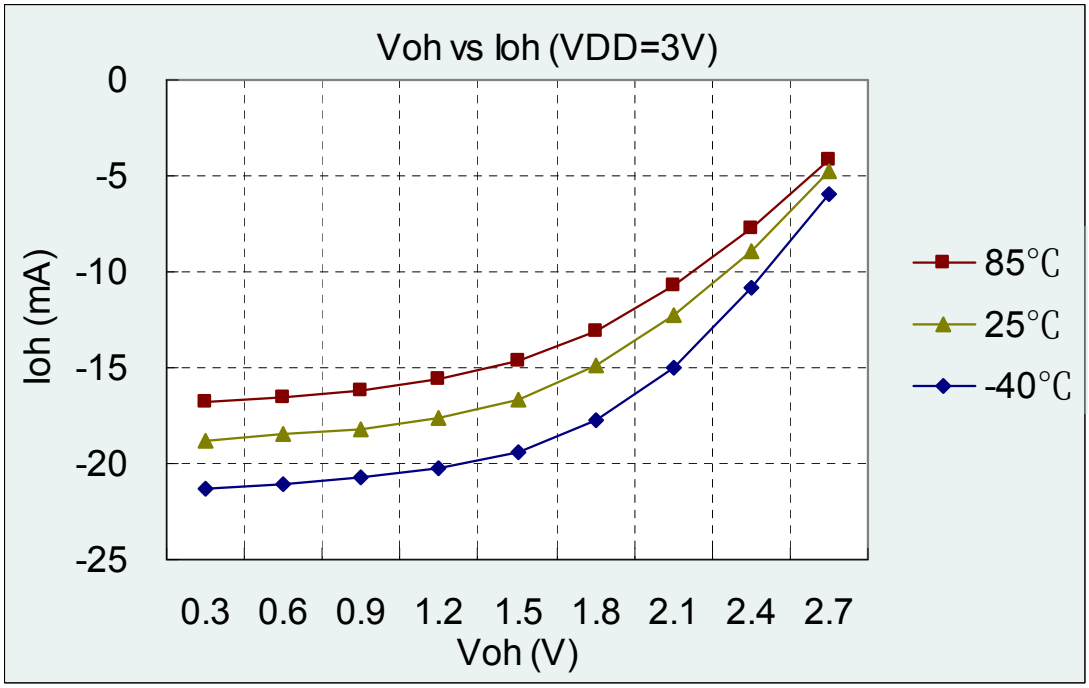


Figure 8-4 VOH vs. IOH (VDD=3V)

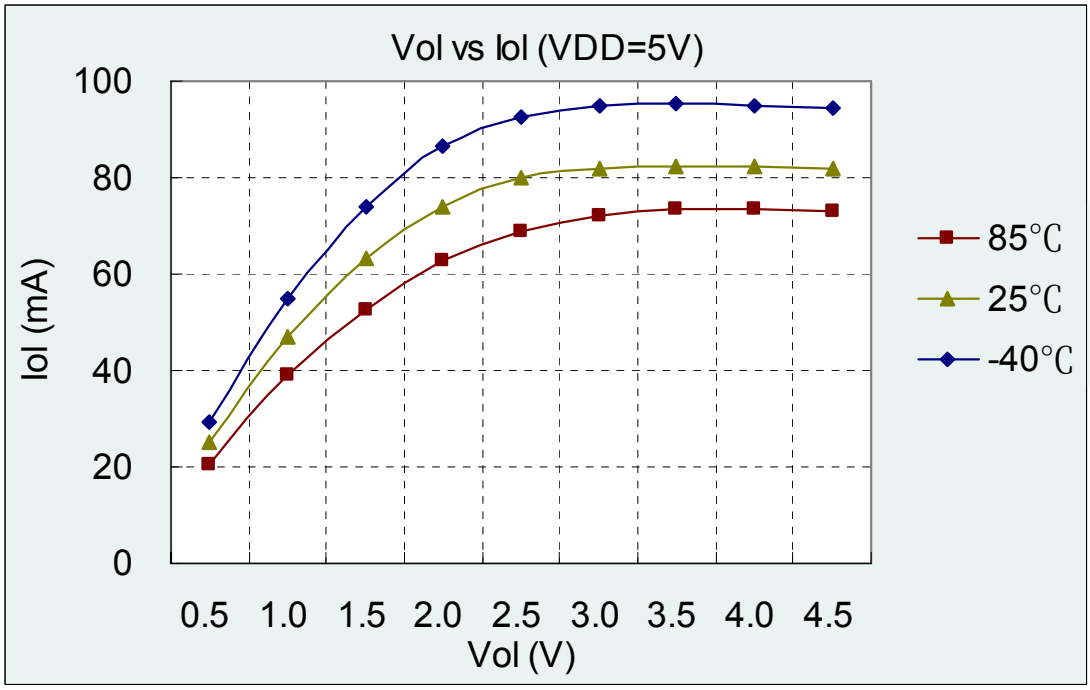


Figure 8-5 VOL vs. IOL (VDD=5V)

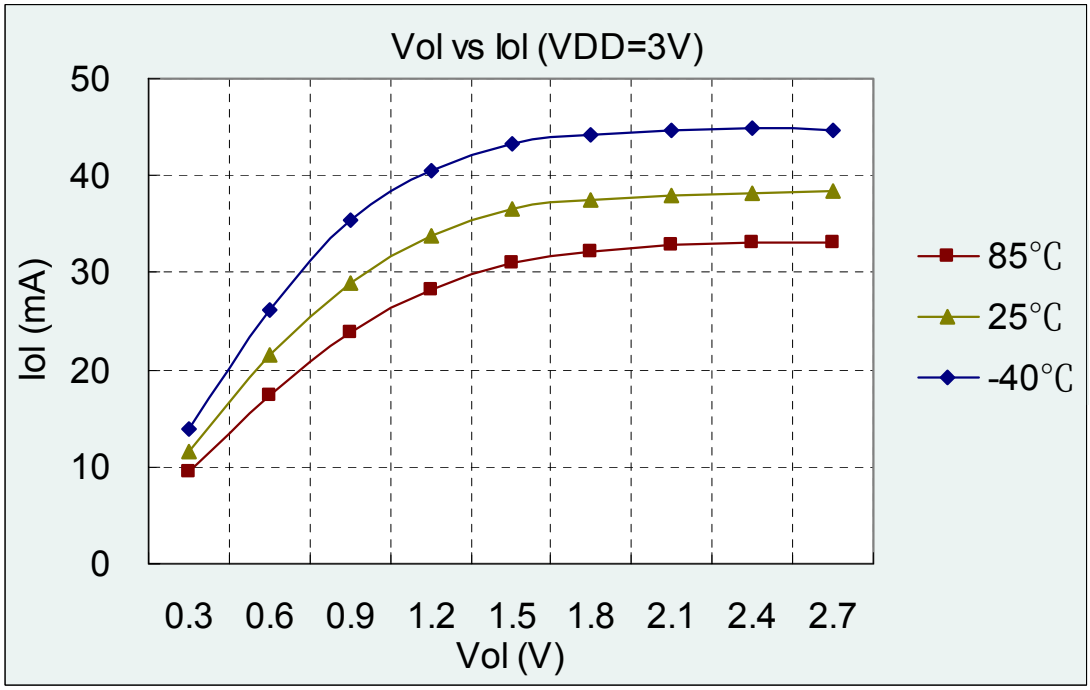


Figure 8-6 VOL vs. IOL (VDD=3V)

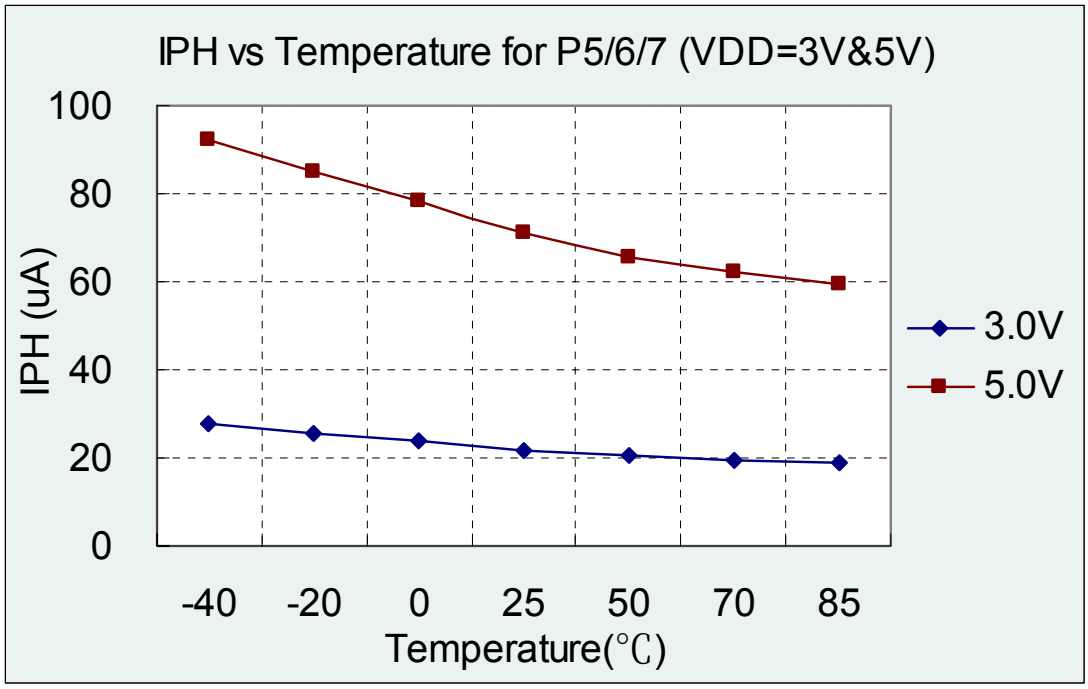


Figure 8-7 IPH vs. Temperature

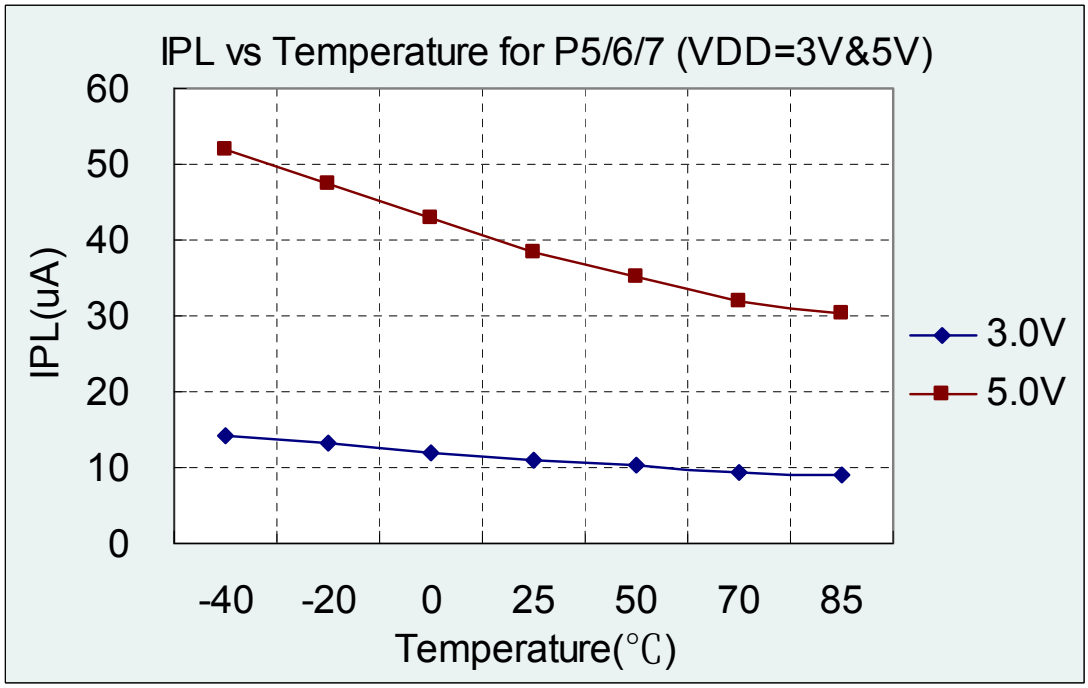


Figure 8-8 IPL vs. Temperature

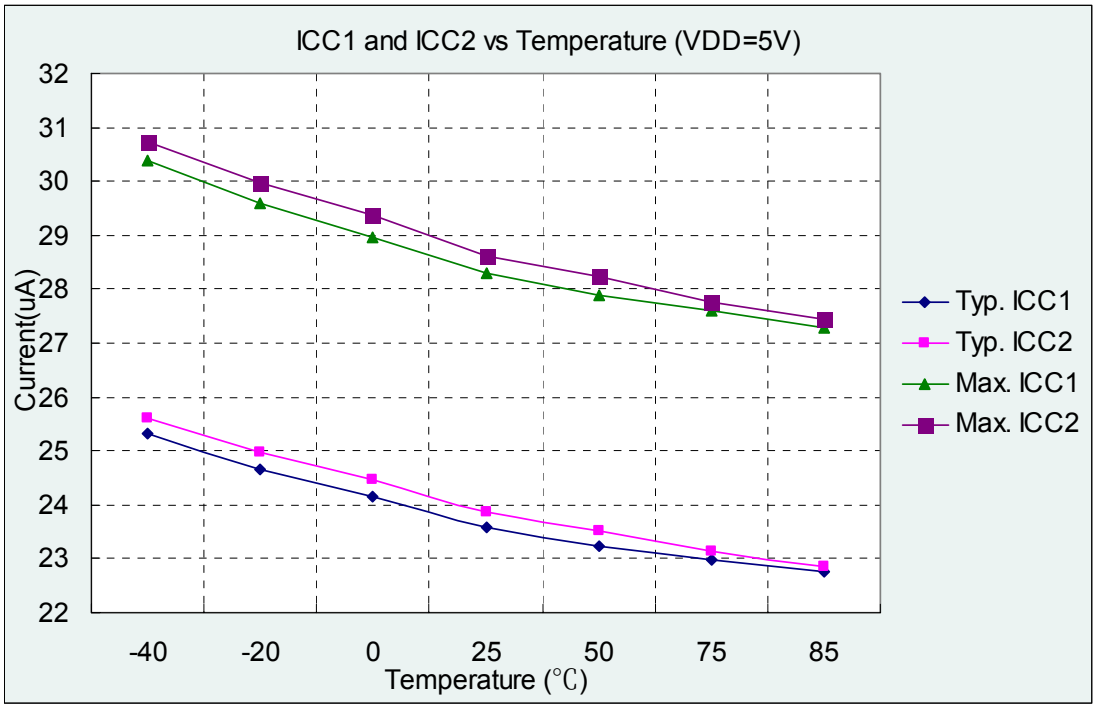


Figure 8-9 ICC1 and ICC2 vs. Temperature (VDD=5V)

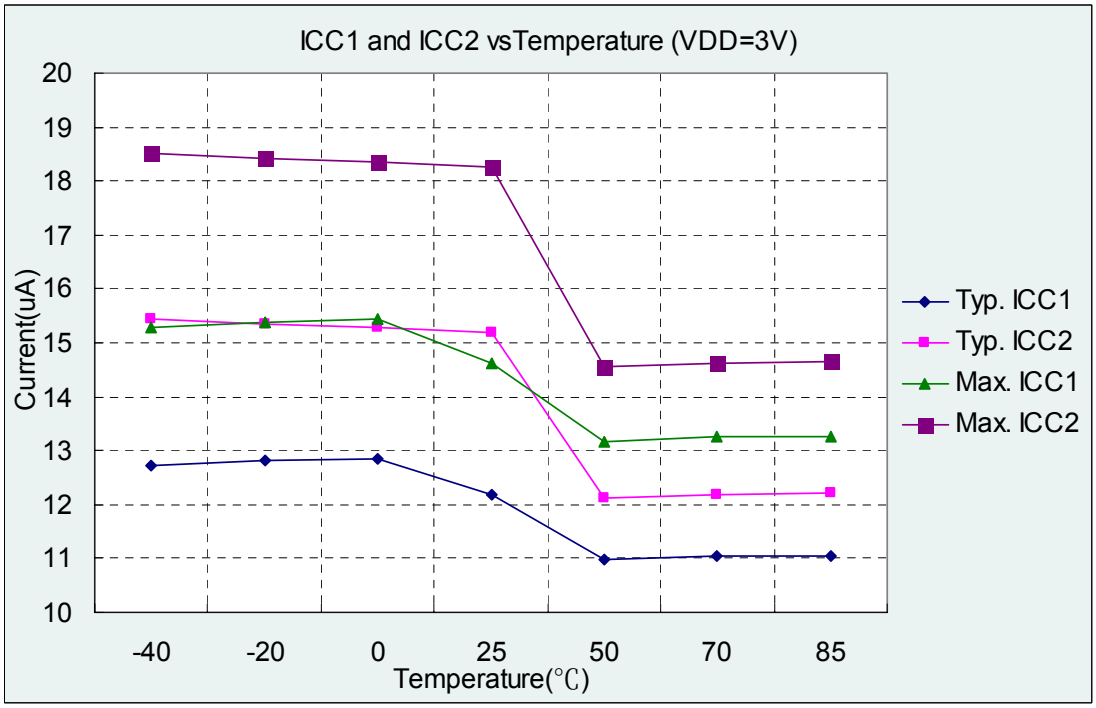


Figure 8-10 ICC1 and ICC2 vs. Temperature (VDD=3V)

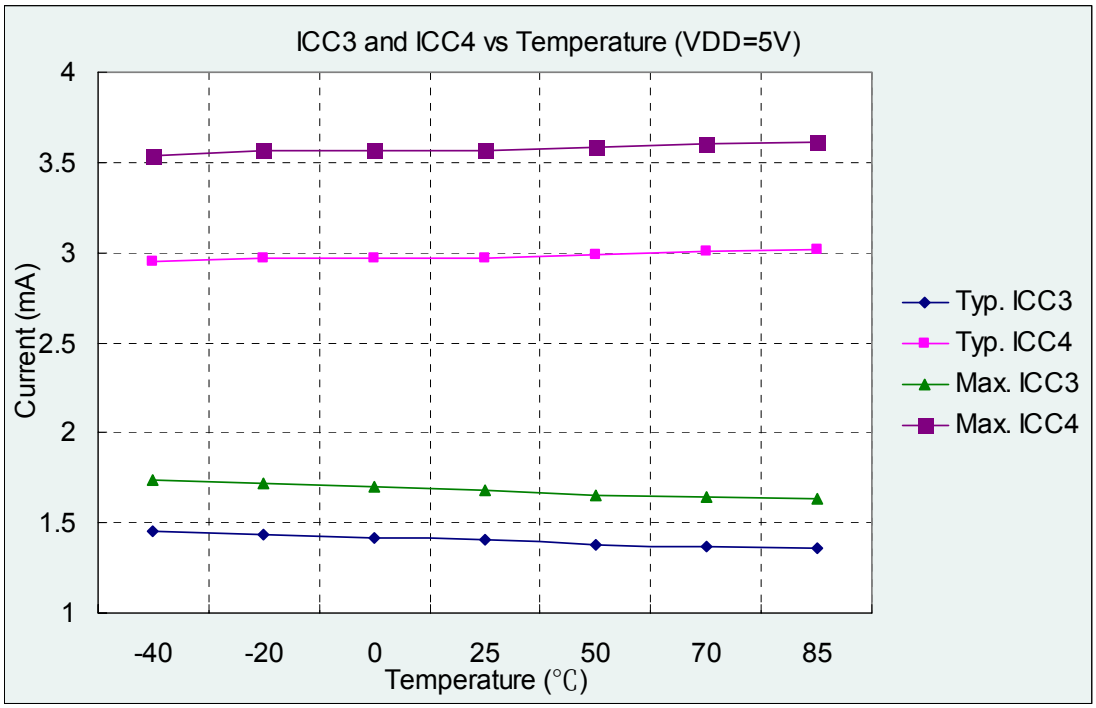


Figure 8-11 ICC3 and ICC4 vs. Temperature (VDD=5V)

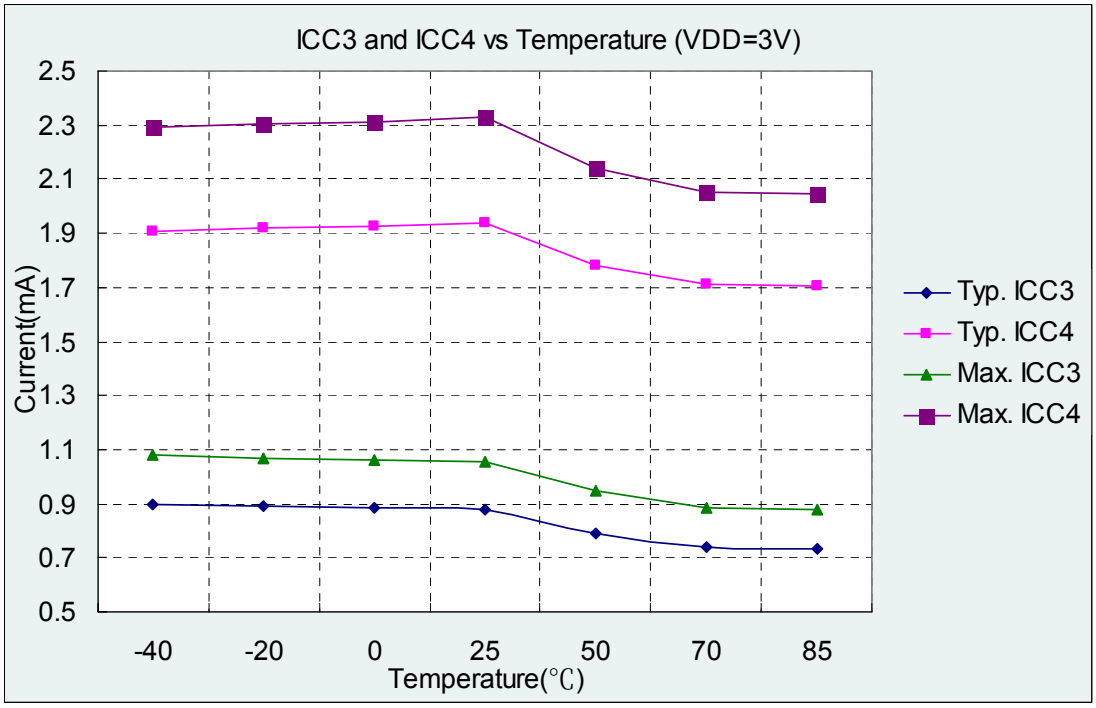


Figure 8-12 ICC3 and ICC4 vs. Temperature (VDD=3V)

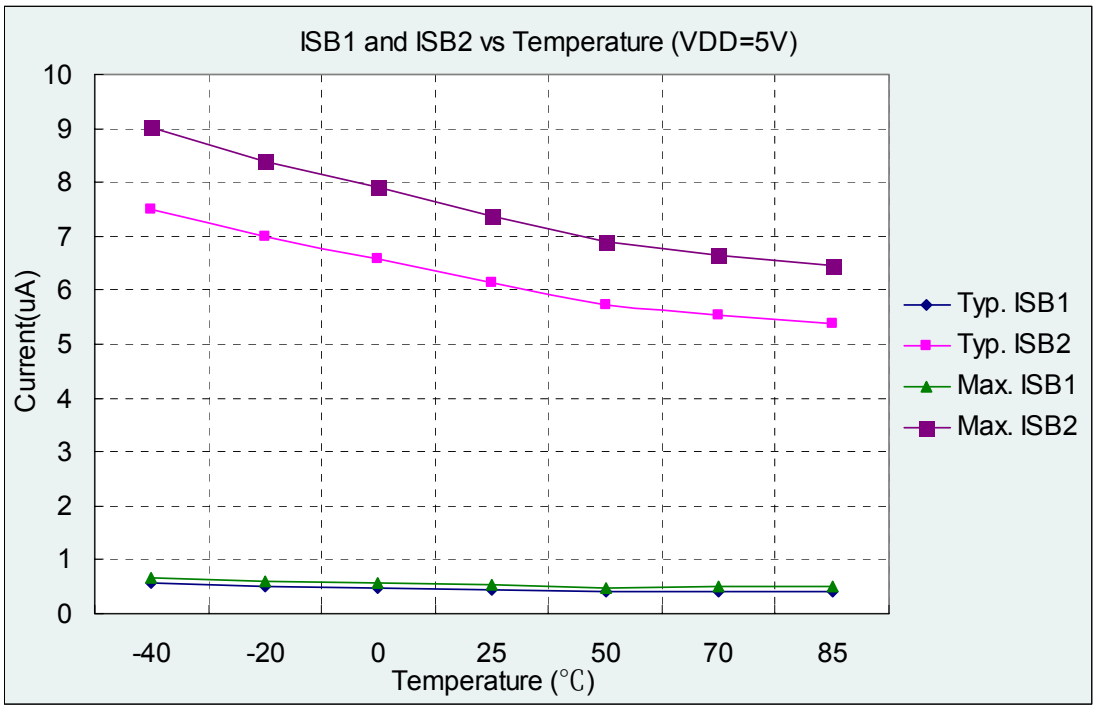


Figure 8-13 ISB1 and ISB2 vs. Temperature (VDD=5V)

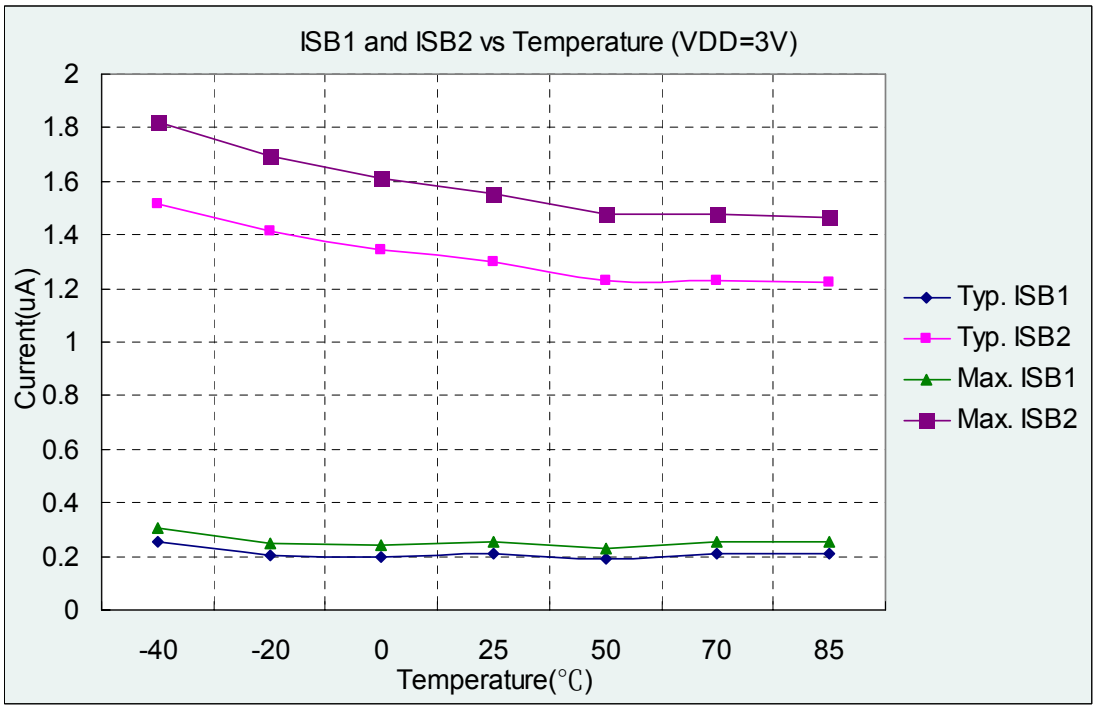


Figure 8-14 ISB1 and ISB2 vs. Temperature (VDD=3V)

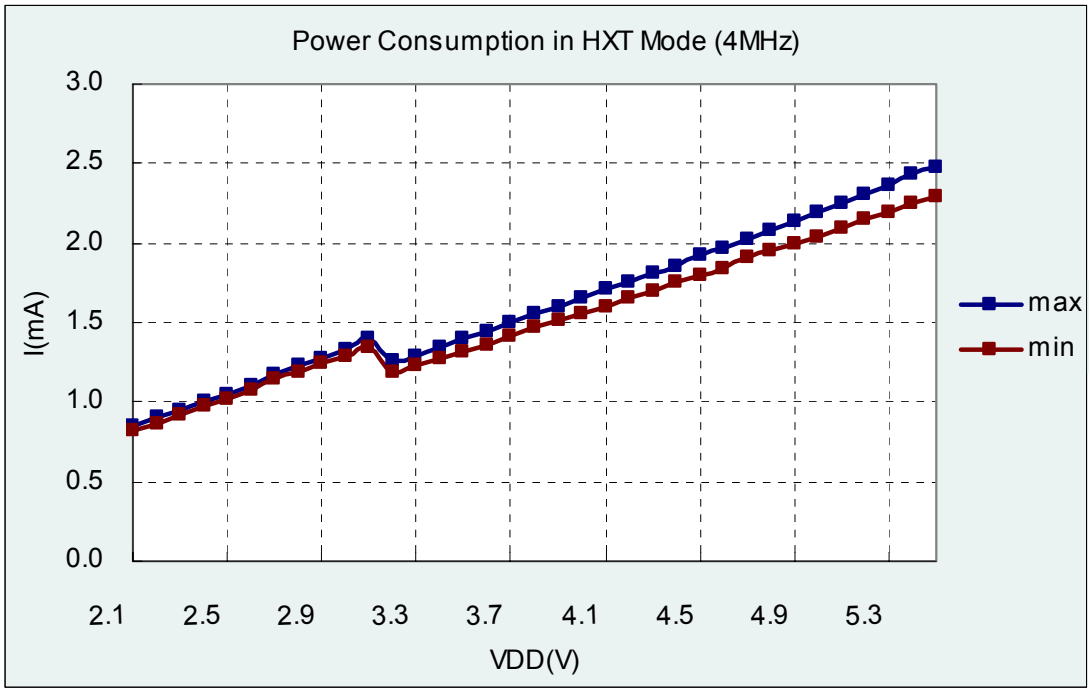


Figure 8-15 I-V Curve (XTAL 4 MHz)

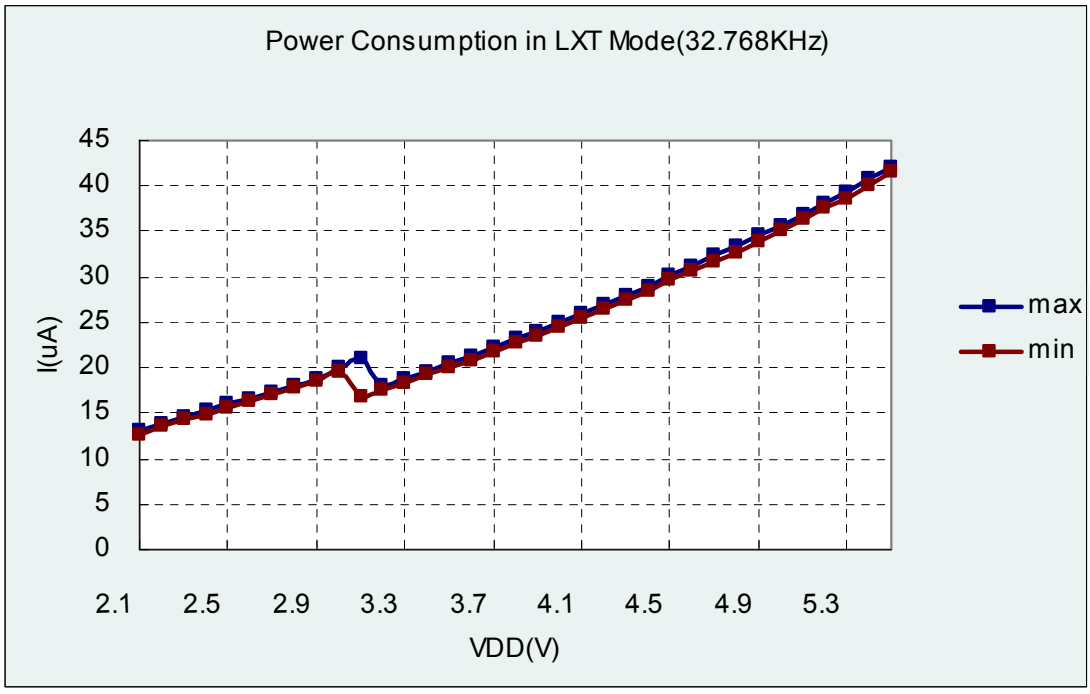


Figure 8-16 I-V Curve (XTAL 32.768kHz)

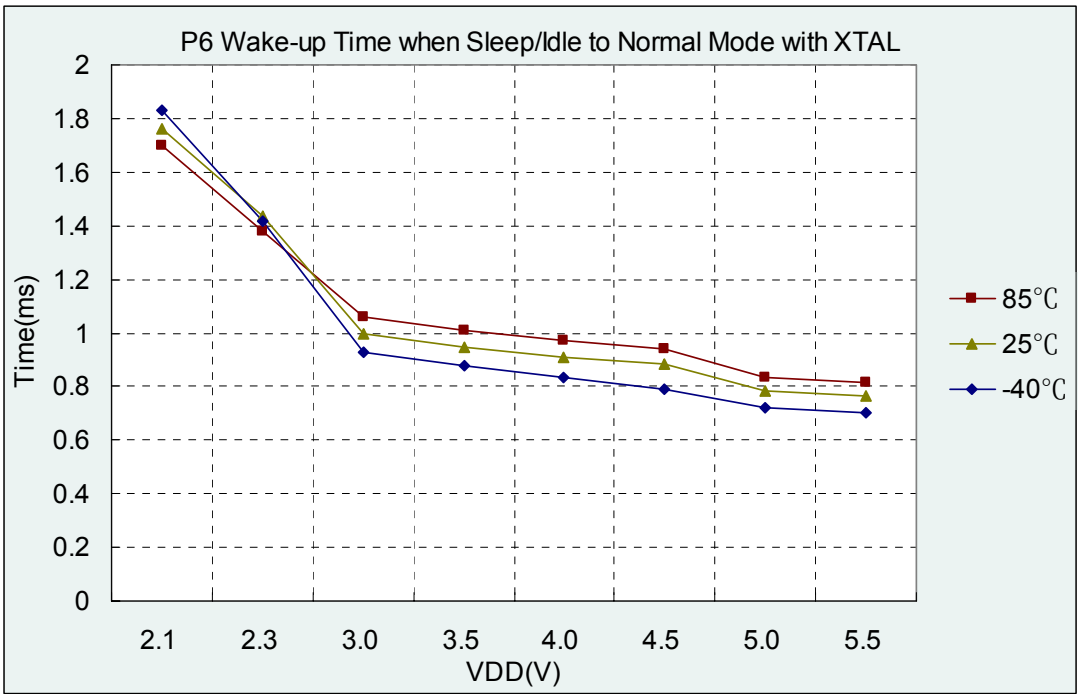


Figure 8-17 P6 Wake-up Time vs. VDD (XTAL Sleep/Idle → Normal)

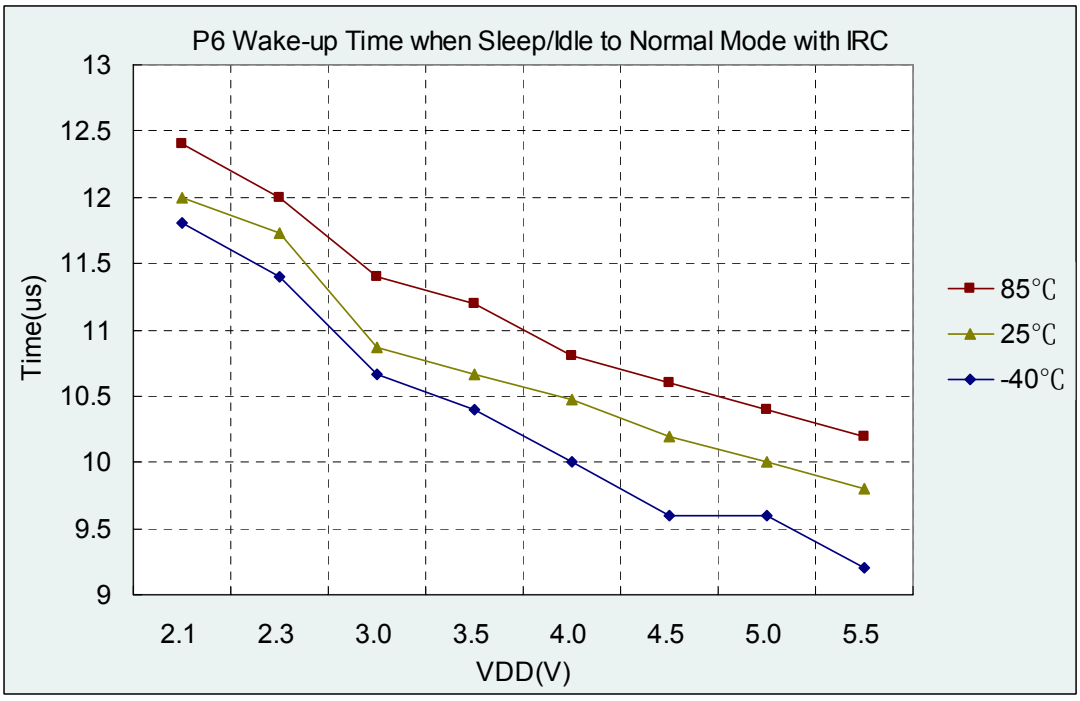


Figure 8-18 P6 Wake-up time vs. VDD (IRC Sleep/Idle → Normal)

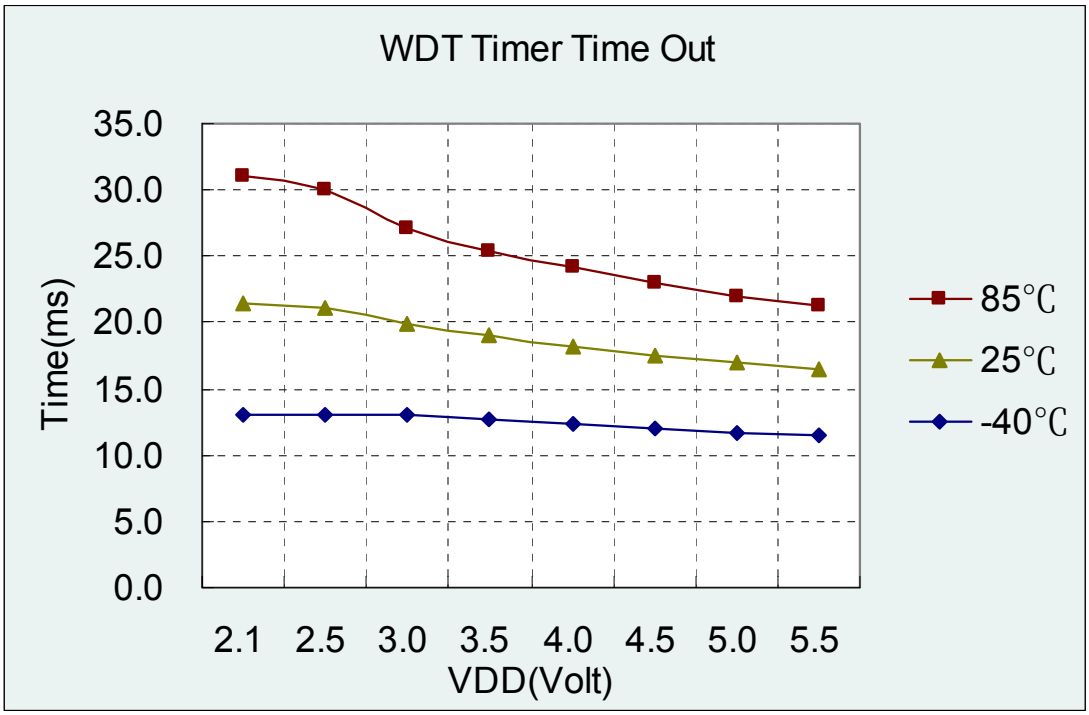


Figure 8-19 WDT (Sub Frequency = 16kHz) vs. VDD

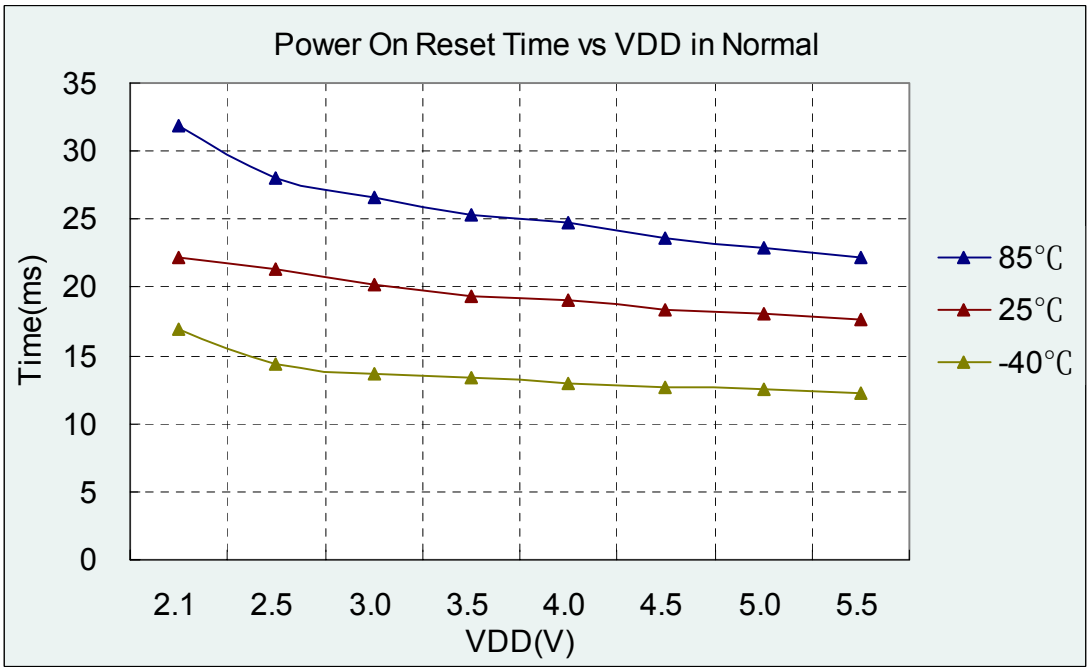


Figure 8-20 Power-on Reset Time vs. VDD

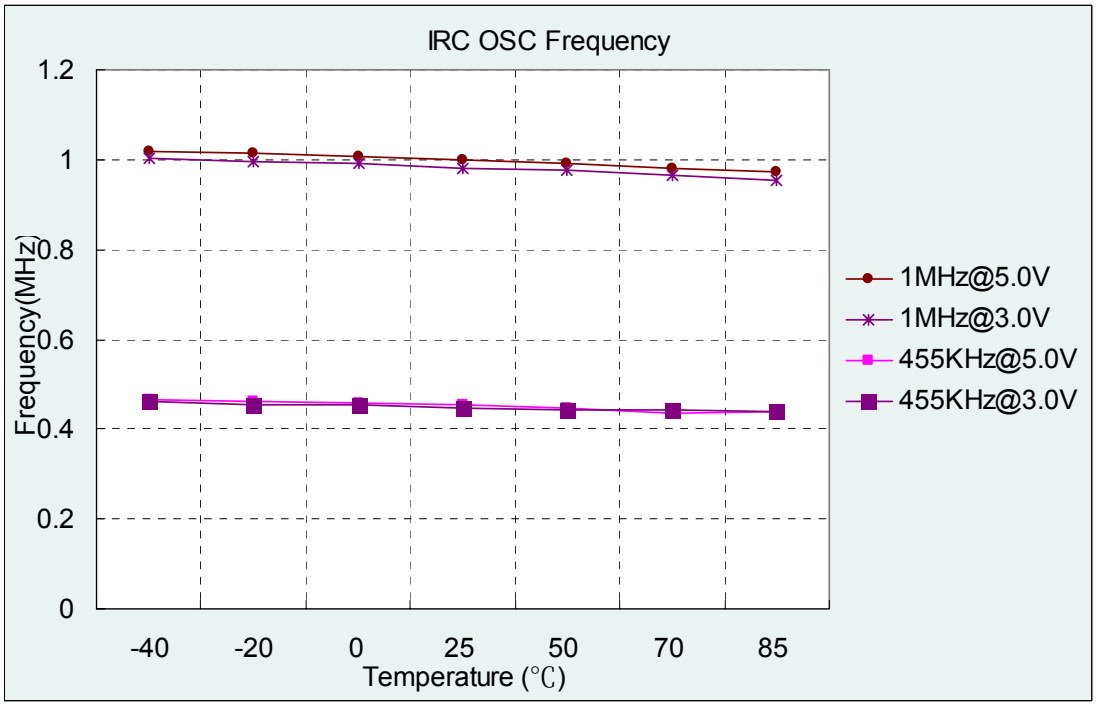


Figure 8-21 IRC (455k and 1 MHz) vs. Temperature (VDD=5V and 3V)

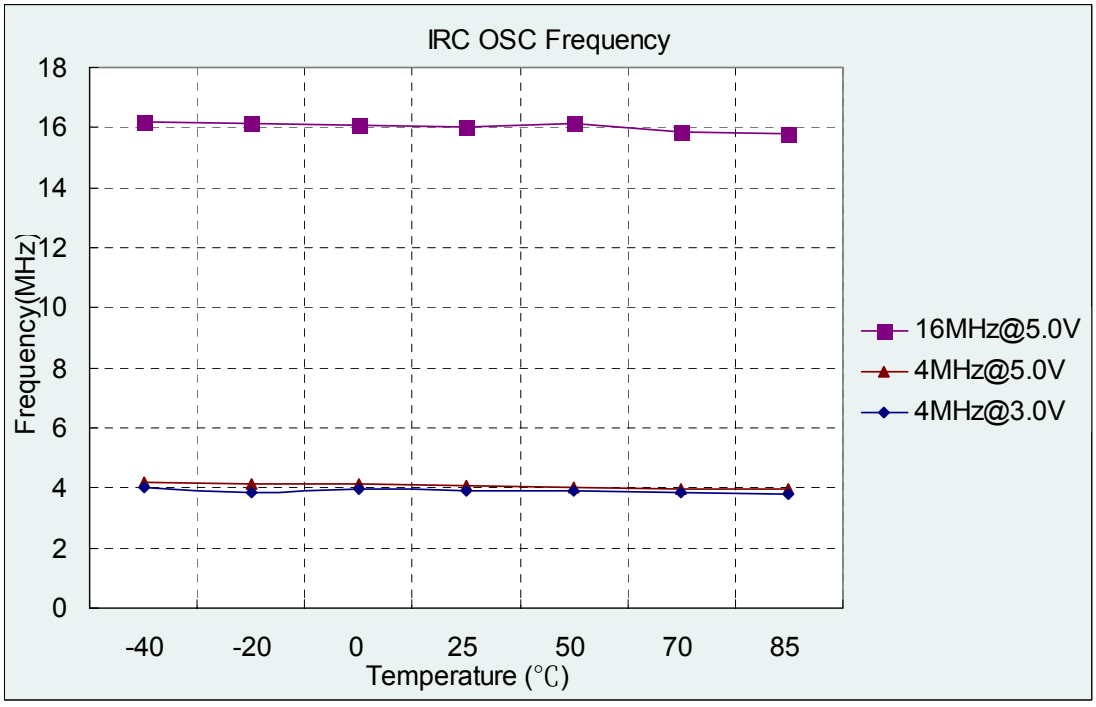


Figure 8-22 IRC (4M and 16 MHz) vs. Temperature (VDD=5V and 3V)

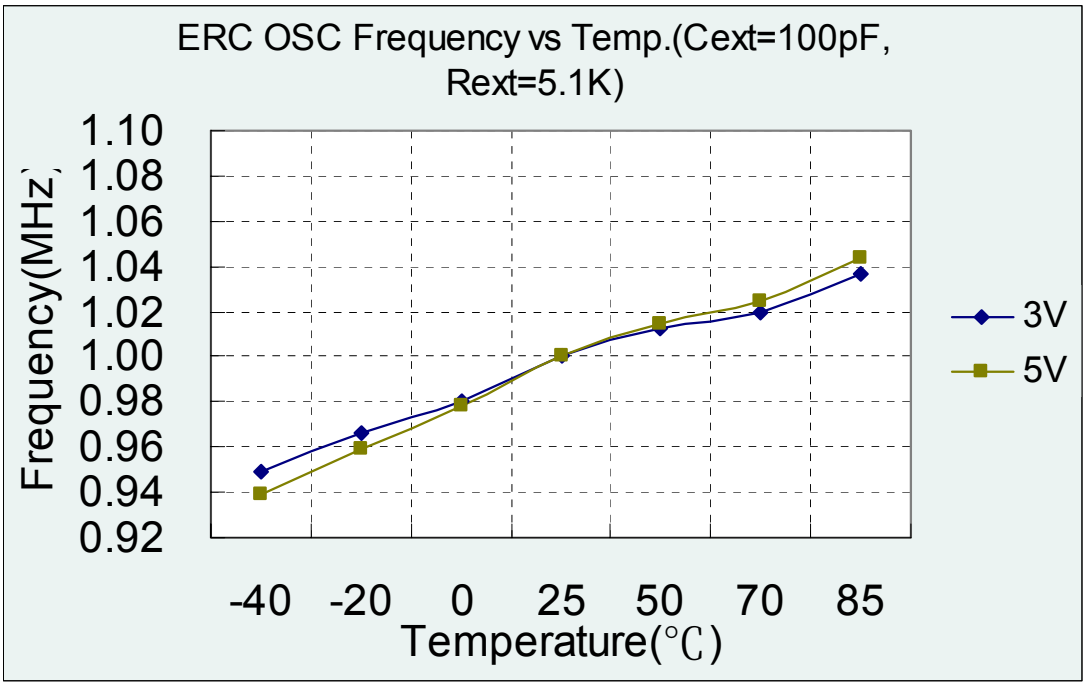


Figure 8-23 ERC OSC Frequency vs. Temperature

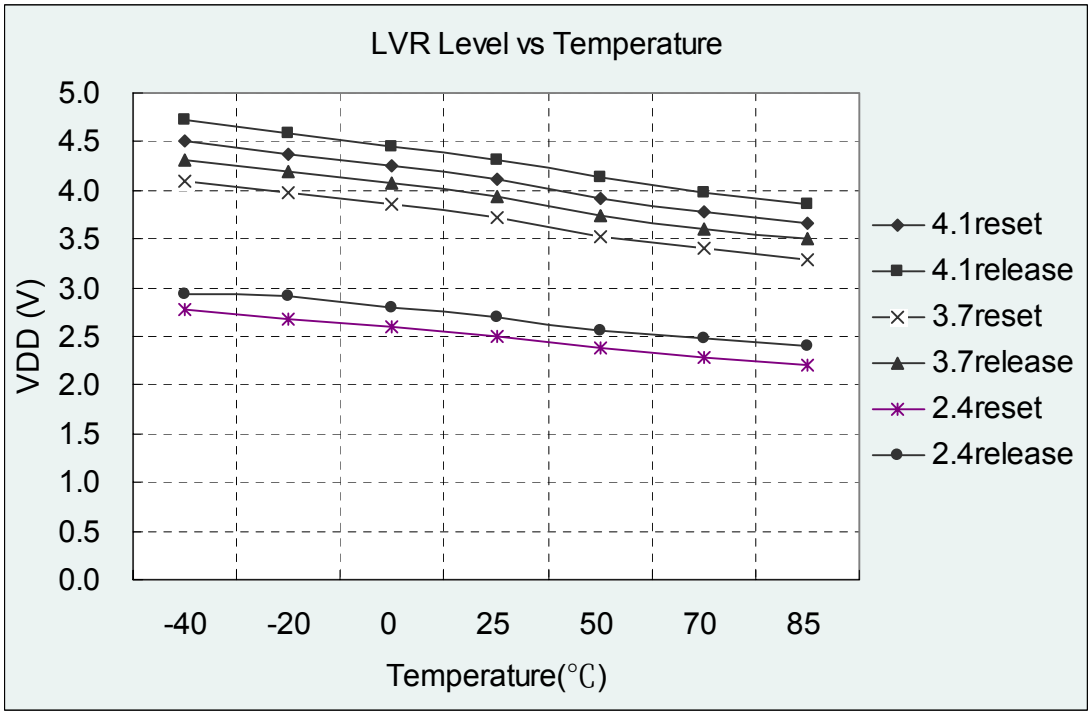


Figure 8-24 LVR Level vs. Temperature

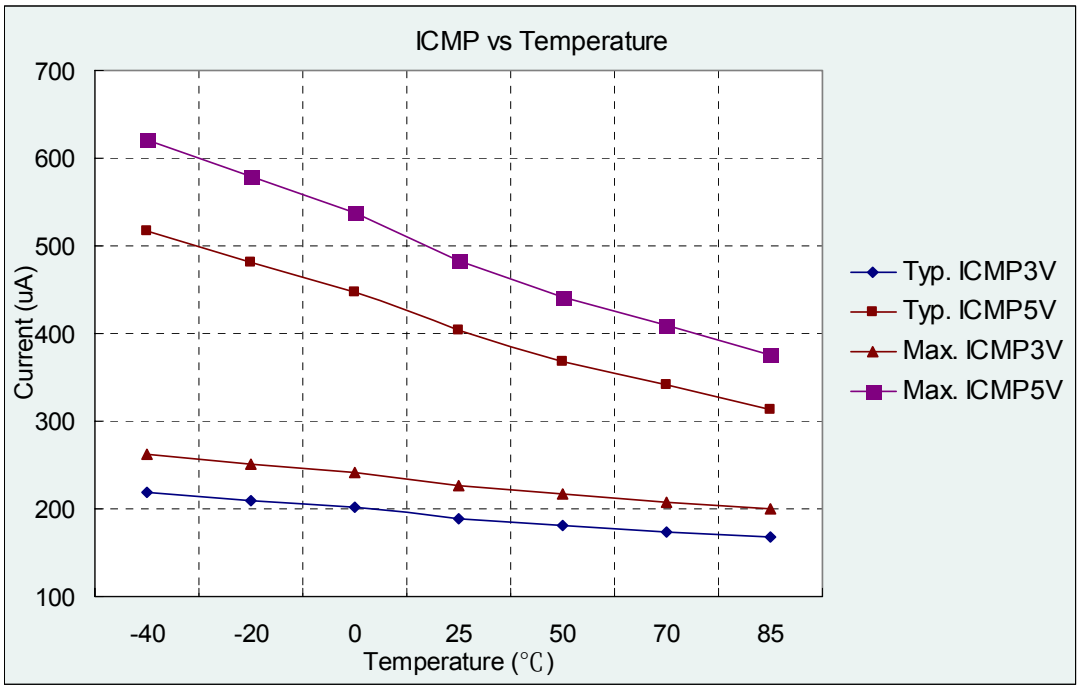


Figure 8-25 ICMP vs. Temperature

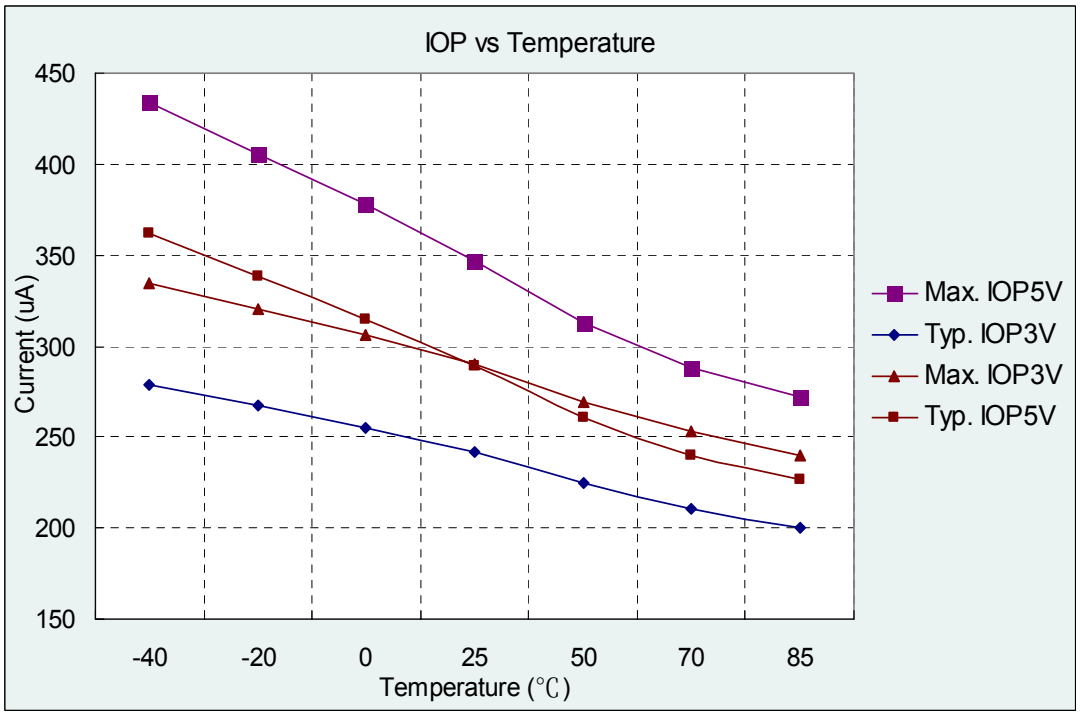


Figure 8-26 IOP vs. Temperature

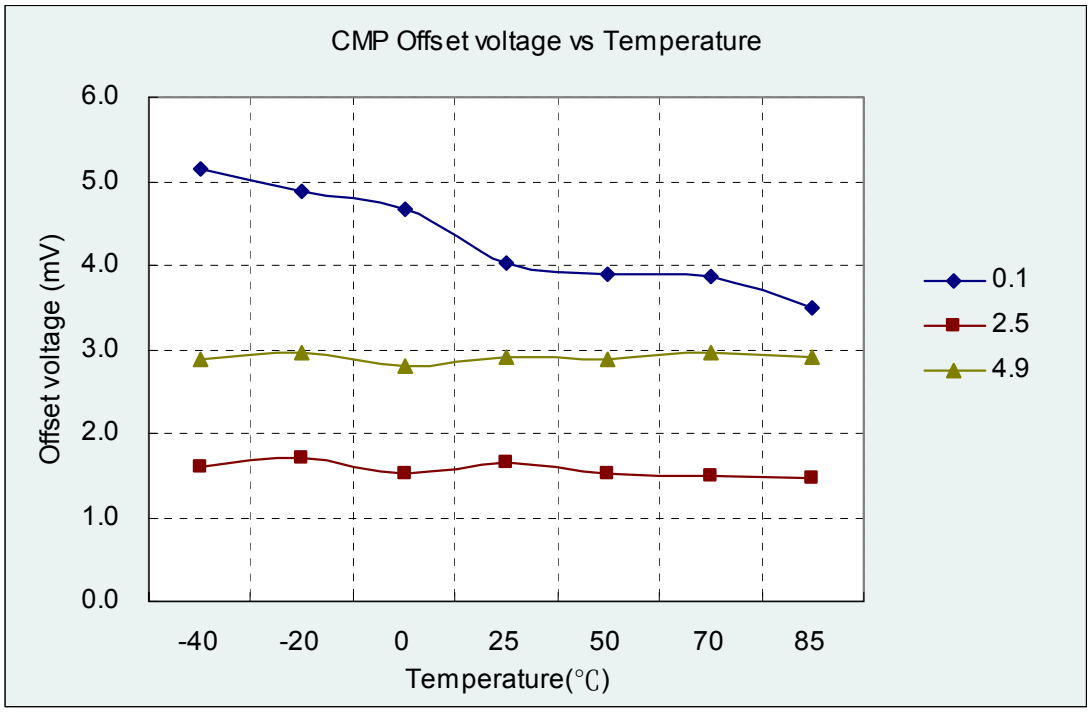


Figure 8-27 CMP Offset Voltage vs. Temperature

(Maximum Absolute Value when V+/V- at 0.1V/2.5V/4.9V)

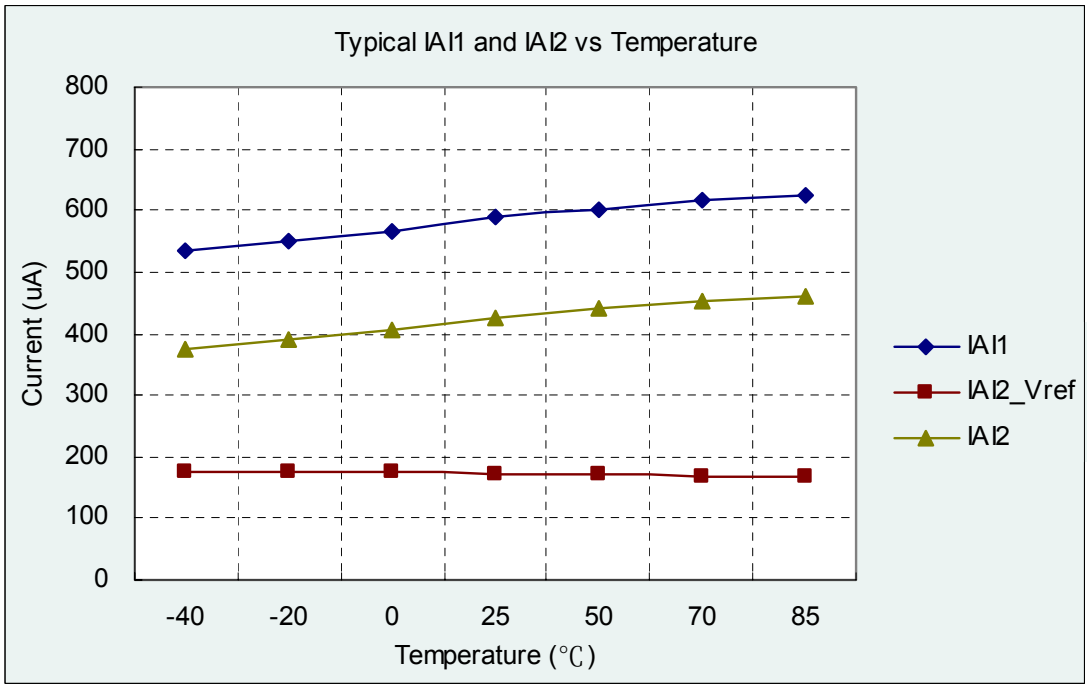


Figure 8-28 IAI1 and IAI2 vs. Temperature (Typical)

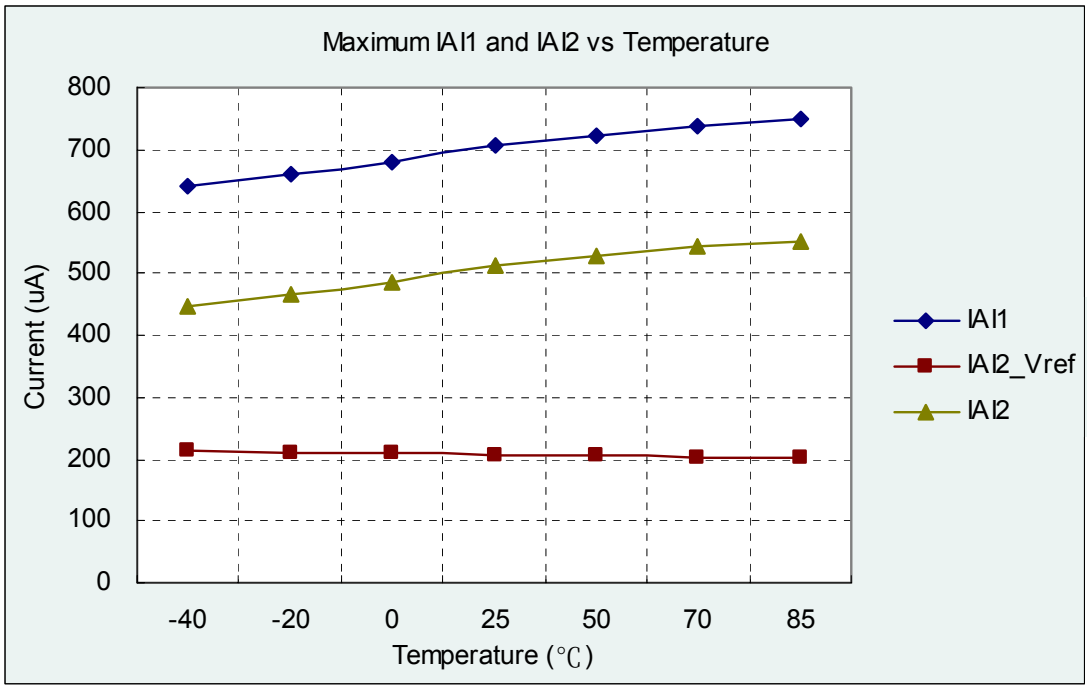


Figure 8-29 IAI1 and IAI2 vs. Temperature (Maximum)

9 AC Electrical Characteristics

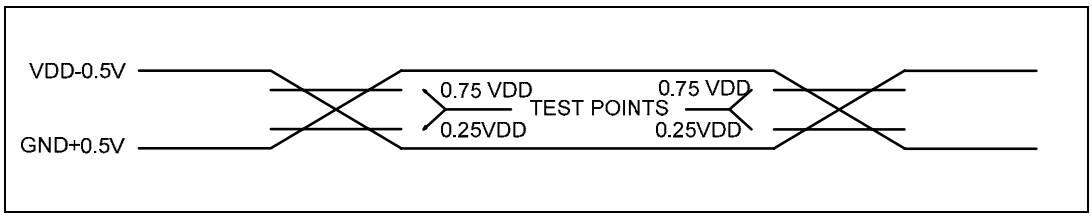
Ta=-40 to 85°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25°C	1	3	5	ns

Note: * N = selected prescaler ratio

10 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for Logic "**1**", and GND+0.5V for Logic "**0**"*
*Timing measurements are made at 0.75V for Logic "**1**", and 0.25VDD for Logic "**0**"*

Figure 10-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

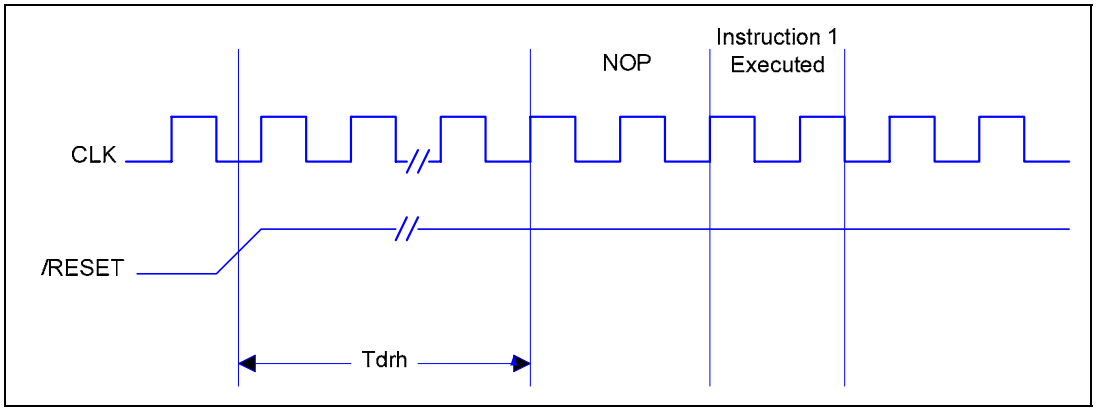


Figure 10-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

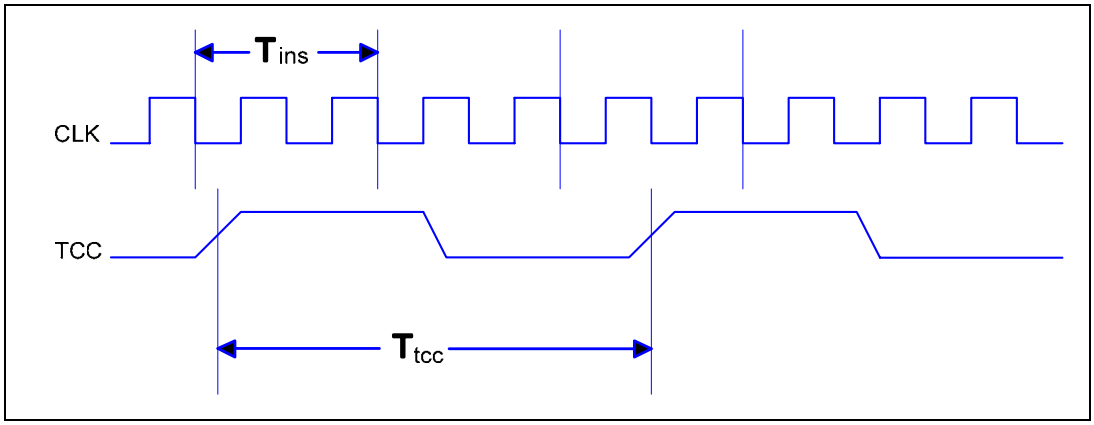


Figure 10-1c TCC Input Timing Diagram

APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P346ND18J/S	DIP	18 pins	300 mil
EM78P346NSO18J/S	SOP	18 pins	300 mil
EM78P346ND20J/S	DIP	20 pins	300 mil
EM78P346NSO20J/S	SOP	20 pins	300 mil
EM78P346NASO20J/S	SOP	20 pins	300 mil
EM78P346NSS20J/S	SSOP	20 pins	209 mil
EM78P346NK24J/S	Skinny DIP	24 pins	300 mil
EM78P346NSO24J/S	SOP	24 pins	300 mil
EM78P346NSS24J/S	SSOP	24 pins	150 mil

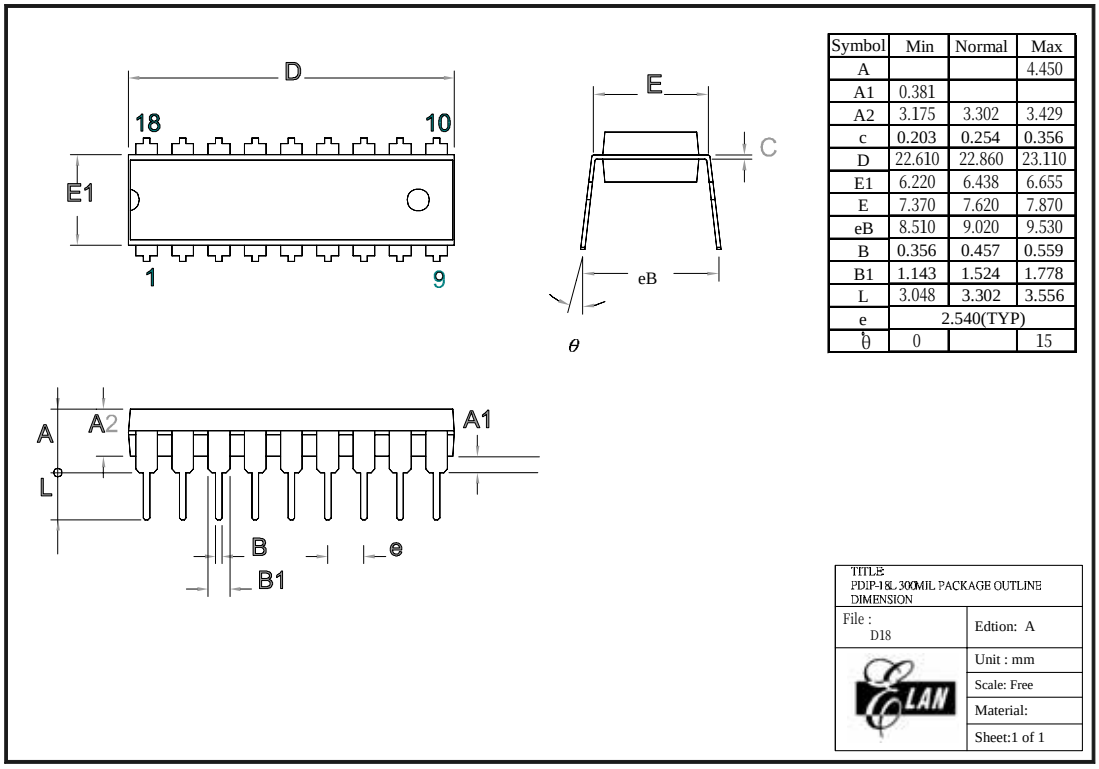
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P346NS/J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point(°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 EM78P346ND18

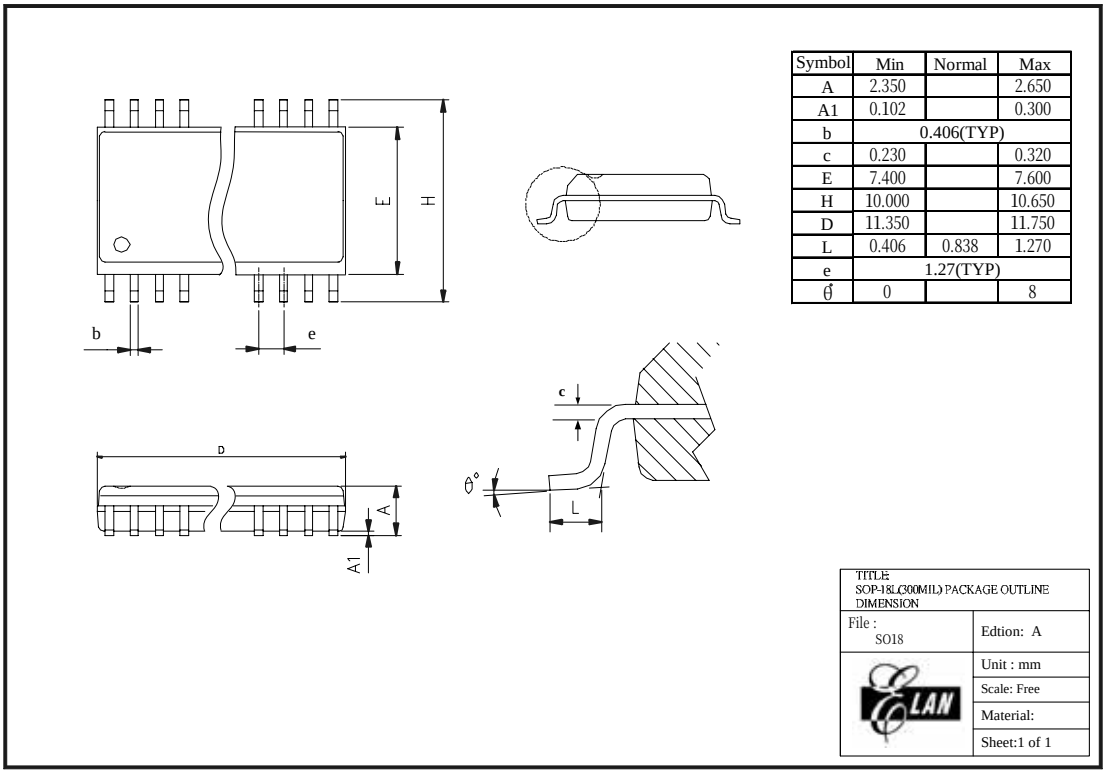


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
File : D18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78P346N 18-pin DIP Package Type

B.2 EM78P346NSO18

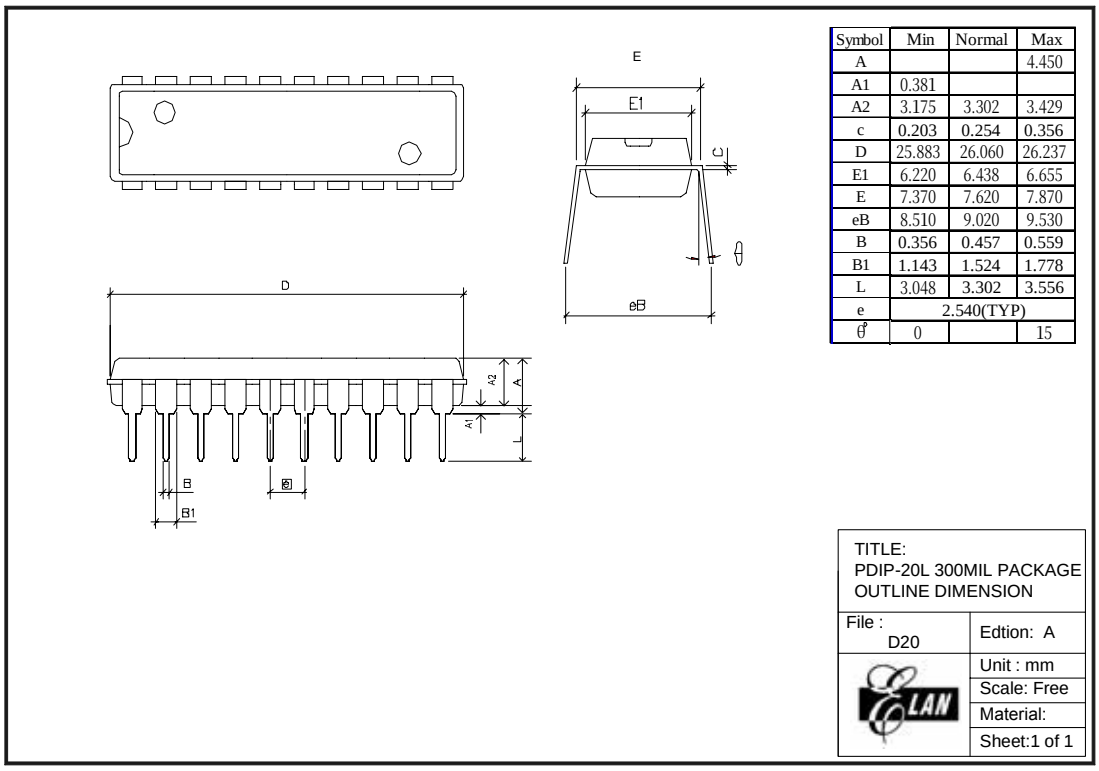


Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-2 EM78P346N 18-pin SOP Package Type

B.3 EM78P346ND20



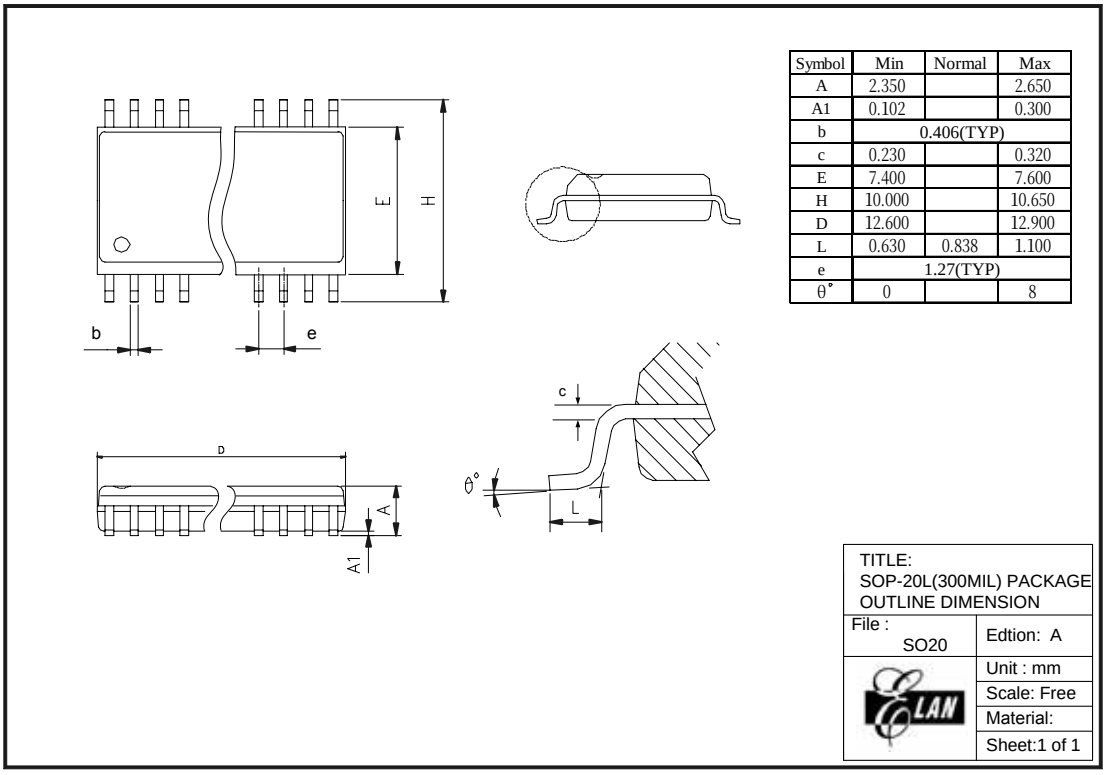
Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE:
PDIP-20L 300MIL PACKAGE
OUTLINE DIMENSION

File : D20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-3 EM78P346N 20-pin DIP Package Type

B.4 EM78P346NSO20

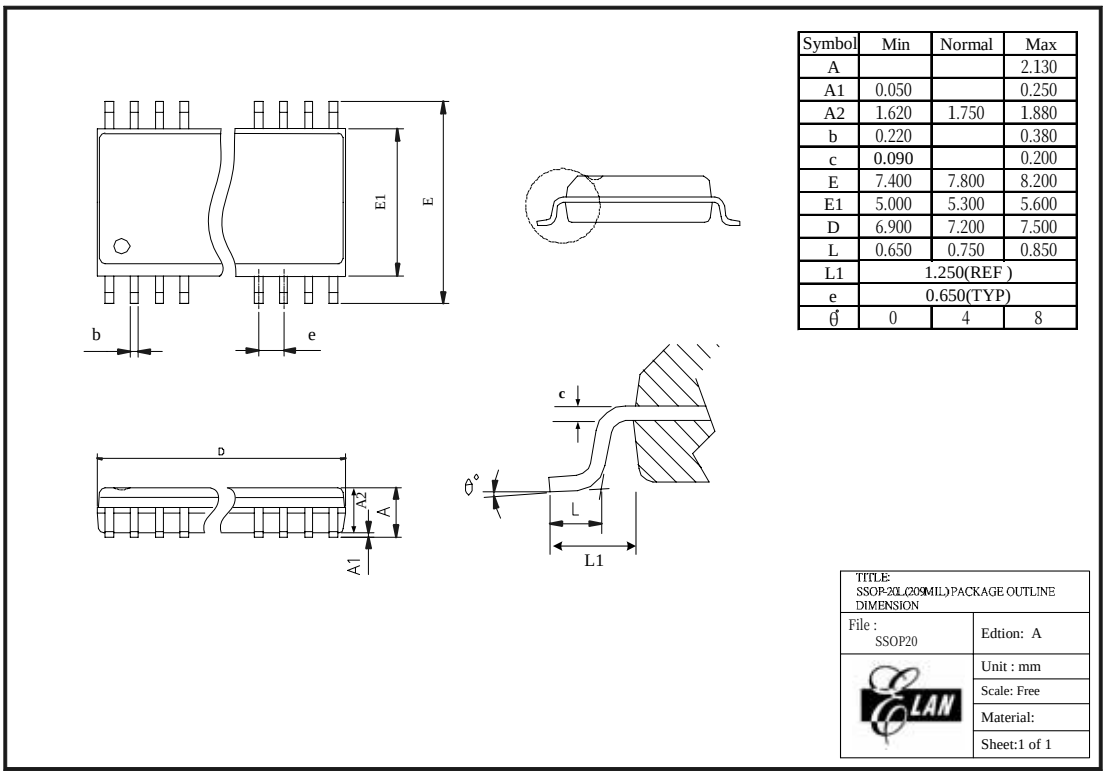


Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 EM78P346N 20-pin SOP Package Type

B.5 EM78P346NSS20



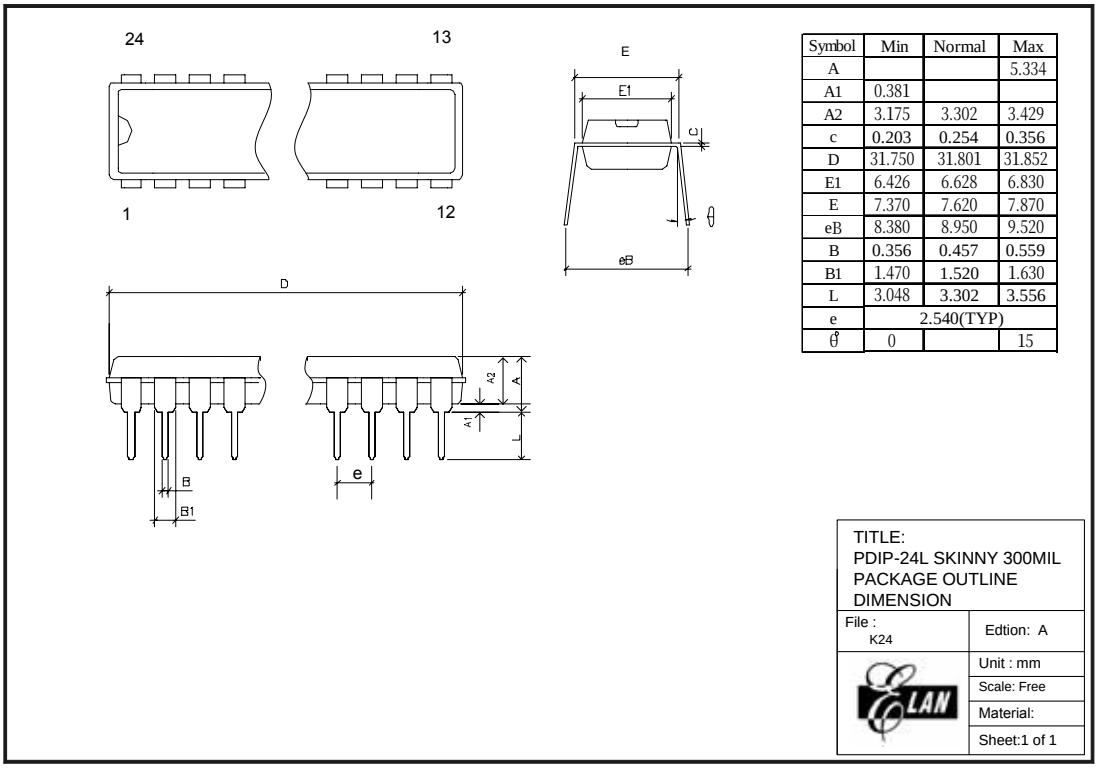
Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ	0	4	8

TITLE:
SSOP-20L(209MIL) PACKAGE OUTLINE DIMENSION

File : SSOP20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-5 EM78P346N 20-pin SSOP Package Type

B.6 EM78P346NK24



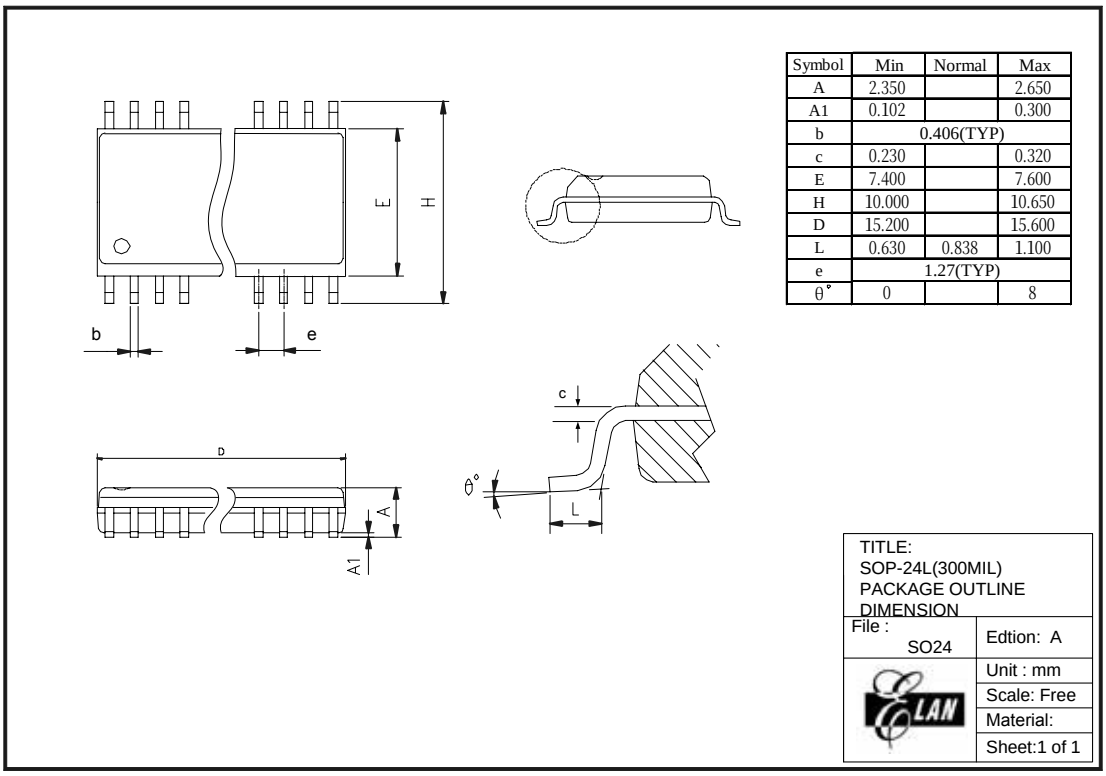
Symbol	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE:
PDIP-24L SKINNY 300MIL
PACKAGE OUTLINE
DIMENSION

File : K24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-6 EM78P346N 24-pin Skinny DIP Package Type

B.7 EM78P346NSO24



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE:
SOP-24L(300MIL)
PACKAGE OUTLINE
DIMENSION

File : SO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-7 EM78P346N 24-pin SOP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15min)~150°C (15min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%, TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%, TD (endurance) = 168, 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ ｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

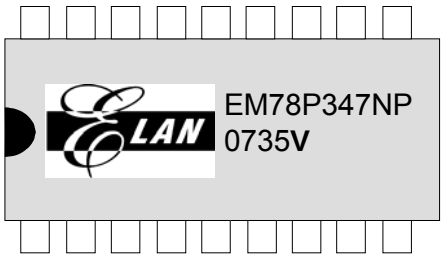
C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

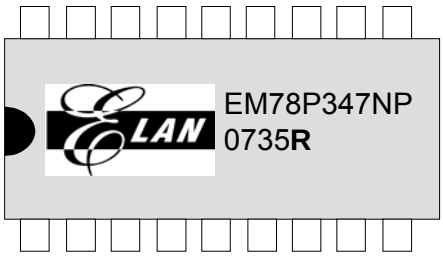
D Comparison between V-Package and R-Package

This series of microcontrollers comprise of the V-package version and the R-package version. In the R-package version, a Code Option NRM is added along with various features such as Crystal mode Operating frequency range and IRC mode wake-up time from sleep mode to normal mode, have been modified to favorably meet users' requirements. The following table is provided for quick comparison between the two package version and for user convenience in the choice of the most suitable product for their application.

Item	EM78P345/6/7N-V	EM78P345/6/7N-R
Level Voltage Reset	**4.1V, 3.7V, 2.8V**	**4.1V, 3.7V, 2.4V**
Crystal mode Operating frequency range	**DC ~ 12 MHz, 4.5V** **DC ~ 8 MHz, 3.0V** **DC ~ 4 MHz, 2.1V**	**DC ~ 16 MHz, 4.5V** **DC ~ 8 MHz, 3.0V** **DC ~ 4 MHz, 2.1V**
IRC mode wake-up time **Sleep mode → Normal mode** **Condition: 5V, 4 MHz**	**80 µs**	**10 µs**
Code Option	×	**Added a Code Option NRM**

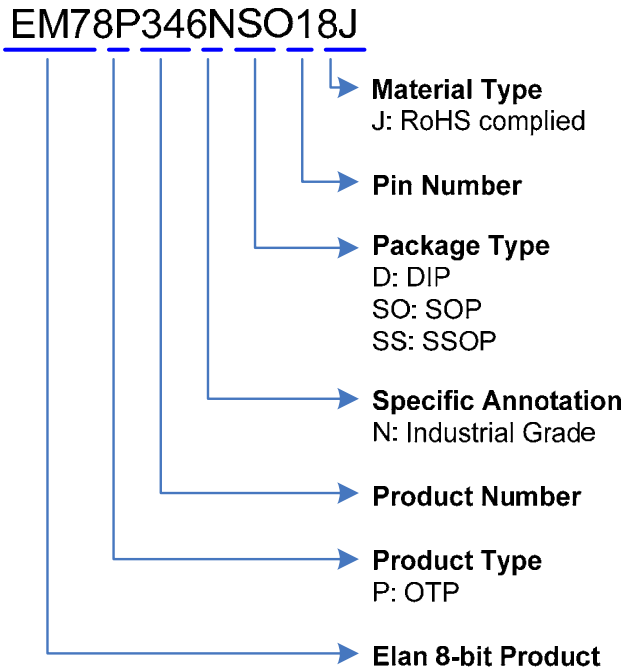


EM78P345/6/7N-V Package Version



EM78P345/6/7N-R Package Version

E Ordering and Manufacturing Information



For example:

EM78P346NSO18J

is EM78P346N with OTP program memory, industrial grade product, in 18-pin SOP package with RoHS complied