TL06xx Low-Power JFET-Input Operational Amplifiers

Check for Samples: TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B

FEATURES

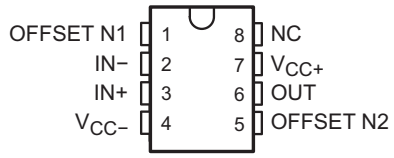
- Very Low Power Consumption
- Typical Supply Current: 200 µA (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes V_{CC+}
- Output Short-Circuit Protection
- High Input Impedance: JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 3.5 V/µs Typ
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

DESCRIPTION

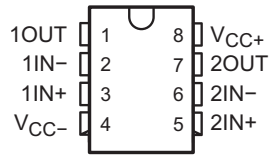
The JFET-input operational amplifiers of the TL06x series are designed as low-power versions of the TL08x series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06x series features the same terminal assignments as the TL07x and TL08x series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in an integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

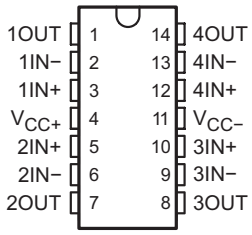
TL061, TL061A . . . D, P, OR PS PACKAGE
TL061B . . . P PACKAGE
(TOP VIEW)



TL062 . . . D, JG, P, PS, OR PW PACKAGE
TL062A . . . D, P, OR PS PACKAGE
TL062B . . . D OR P PACKAGE
(TOP VIEW)

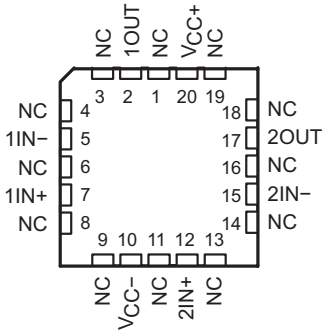


TL064 . . . D, J, N, NS, PW, OR W PACKAGE
TL064A, TL064B . . . D OR N PACKAGE
(TOP VIEW)

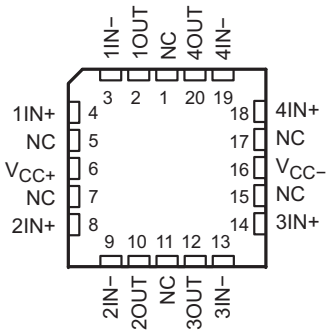


NC − No internal connection

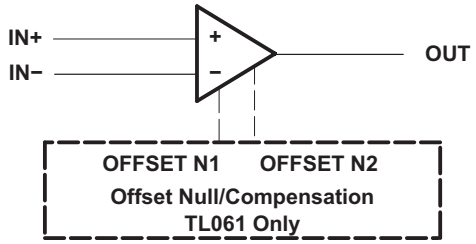
TL062 . . . FK PACKAGE
(TOP VIEW)



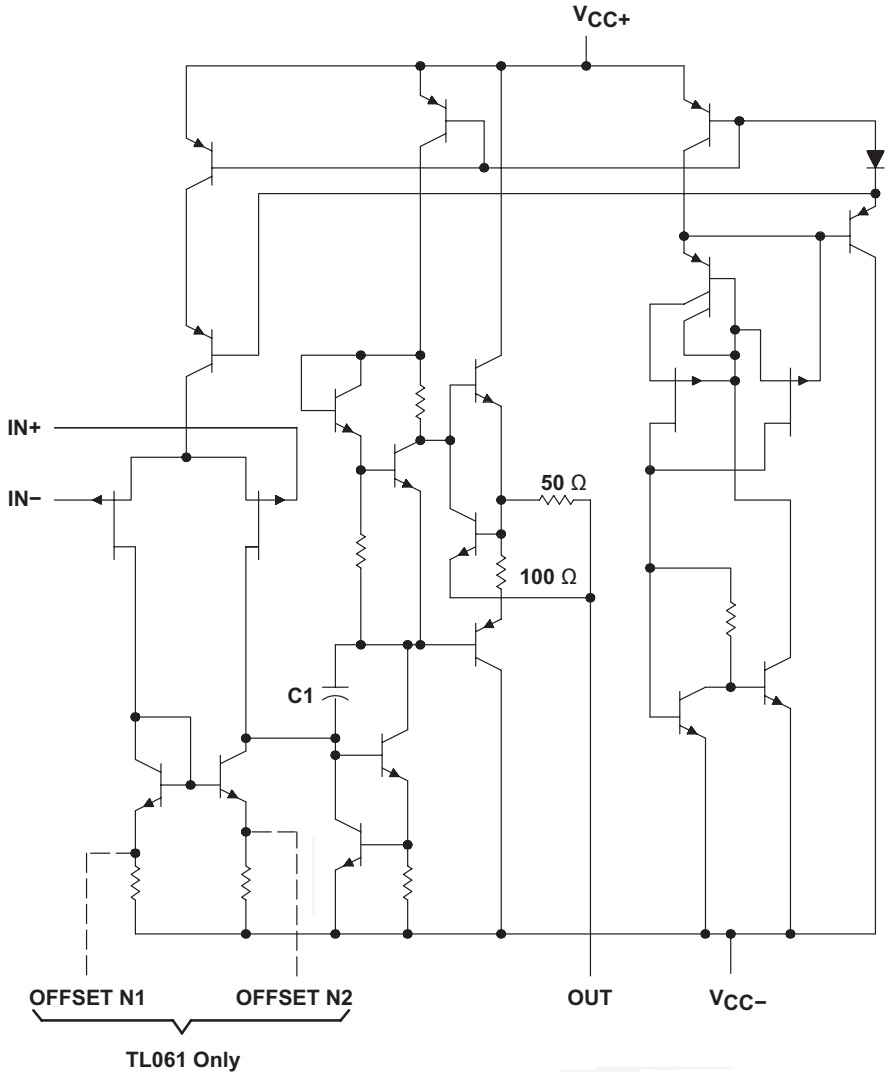
TL064 . . . FK PACKAGE
(TOP VIEW)



Symbols



Schematic (Each Amplifier)



C1 = 10 pF on TL061, TL062, and TL064
Component values shown are nominal.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
V_{CC+}	Supply voltage(2)		18	18	18	V
V_{CC-}			–18	–18	–18	
V_{ID}	Differential input voltage(3)		±30	±30	±30	V
V_I	Input voltage(2)(4)		±15	±15	±15	V
	Duration of output short circuit(5)		Unlimited	Unlimited	Unlimited	
θ_{JA}	Package thermal impedance(6)(7)	D package (8 pin)	97	97		°C/W
		D package (14 pin)	86	86		
		N package	80	80		
		NS package	76	76		
		P package	85	85		
		PS package	95	95		
		PW (8 pin) package	149	149		
		PW (14 pin) package	113	113		
θ_{JC}	Package thermal impedance(8)(9)	FK package			5.61	°C/W
		J package			15.05	
		JG package			14.5	
		W package			14.65	
T_J	Operating virtual junction temperature		150	150	150	°C
	Case temperature for 60 seconds	FK package			260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	260		°C
T_{stg}	Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.
(8) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(9) The package thermal impedance is calculated in accordance with MIL-STD-883.

Electrical Characteristics

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		TL061C, TL062C, TL064C			TL061AC, TL062AC, TL064AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	15		3	6	mV
			T_A = Full range			20			7.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		µV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	200		5	100	pA
			T_A = Full range			5			3	nA
I_{IB}	Input bias current[2]	V_O = 0	T_A = 25°C		30	400		30	200	pA
			T_A = Full range			10			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	3	6		4	6		V/mV
			T_A = Full range	3			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and −40°C to 85°C for TL06xI.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

Electrical Characteristics

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		TL061BC TL062BC TL064BC			TL061I TL062I TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		2	3		3	6	mV
			T_A = Full range			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10		µV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = Full range			3			10	nA
I_{IB}	Input bias current[2]	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = Full range			7			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = Full range		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = Full range	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and −40°C to 85°C for TL06xI.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

Electrical Characteristics

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		TL061M TL062MM			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = –55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = –55°C to 125°C			10			10		µV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = –55°C			20[2]			20[2]	nA
			T_A = 125°C			20			20	
I_{IB}	Input bias current[3]	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = –55°C			50[2]			50[2]	nA
			T_A = 125°C			50			50	
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = –55°C to 125°C		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = –55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C								MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, No load, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, No load, T_A = 25°C			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
(2) This parameter is not production tested.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A= 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain[1]	V_I = 10 V, R_L = 10 kΩ,	C_L = 100 pF, See Figure 1	1.5	3.5		V/µs
t_r	Rise-time	V_I = 20 V, R_L = 10 kΩ,	C_L = 100 pF, See Figure 1		0.2		µs
	Overshoot factor				10		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		42		nV/√Hz

(1) Slew rate at −55°C to 125°C is 0.7 V/µs min.

Parameter Measurement Information

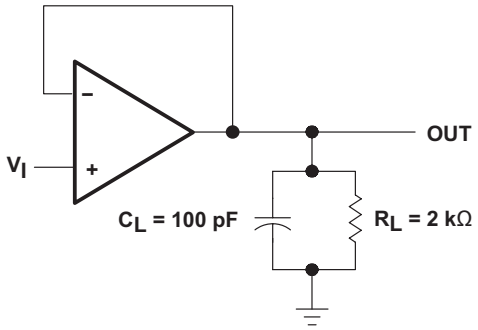


Figure 1. Unity-Gain Amplifier

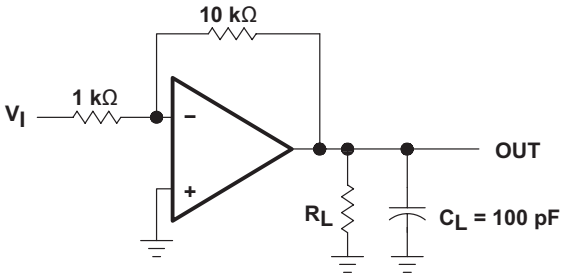


Figure 2. Gain-of-10 Inverting Amplifier

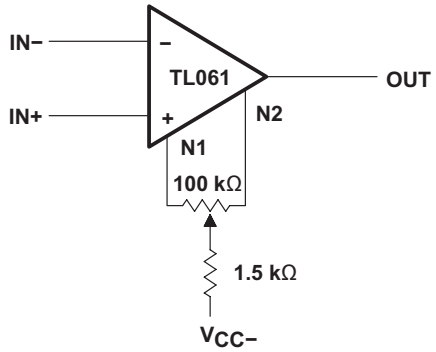


Figure 3. Input Offset-Voltage Null Circuit

Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

Table of Graphs

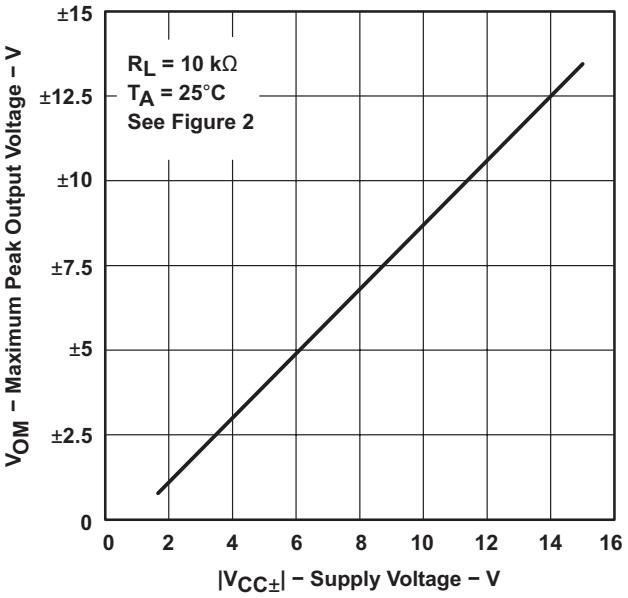


Figure 4. Maximum Peak Output Voltage vs Supply Voltage

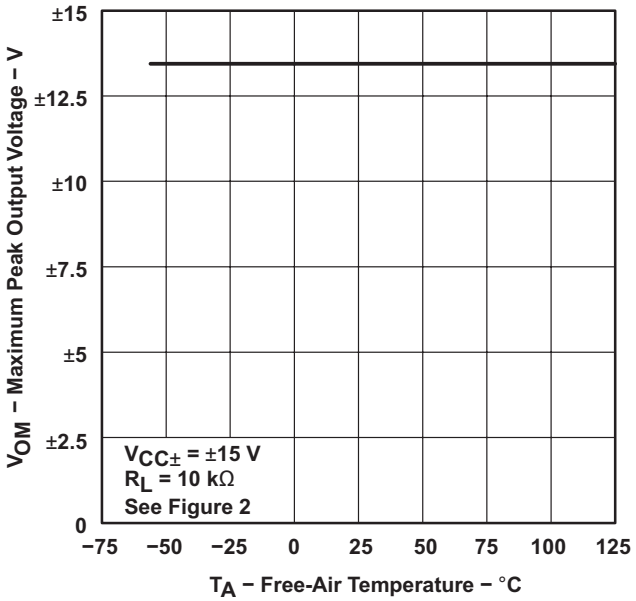


Figure 5. Maximum Peak Output Voltage vs Free-Air Temperature

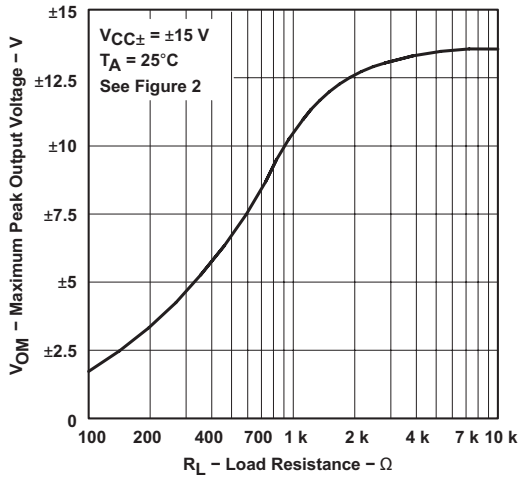


Figure 6. Maximum Peak Output Voltage vs Load Resistance

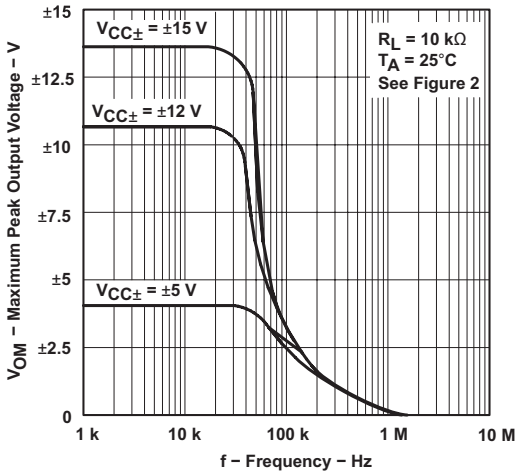


Figure 7. Maximum Peak Output Voltage vs Frequency

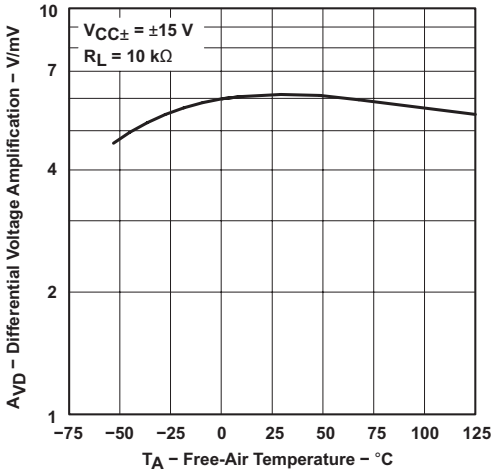


Figure 8. Differential Voltage Amplification vs Free-Air Temperature

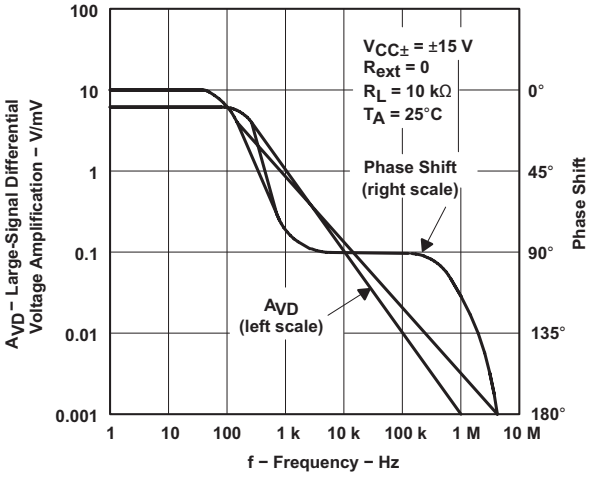


Figure 9. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

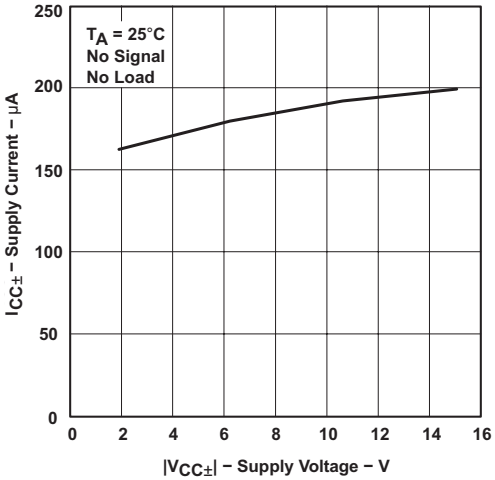


Figure 10. Supply Current vs Supply Voltage

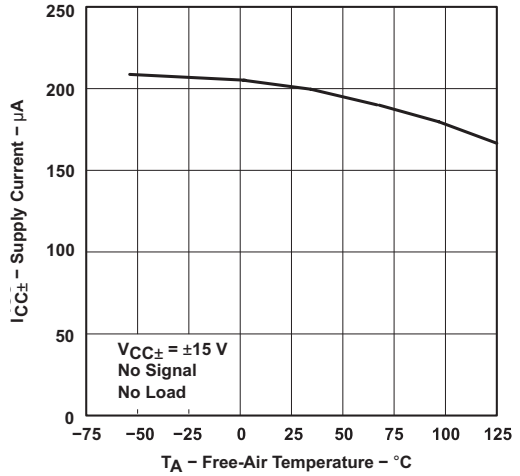


Figure 11. Supply Current vs Free-Air Temperature

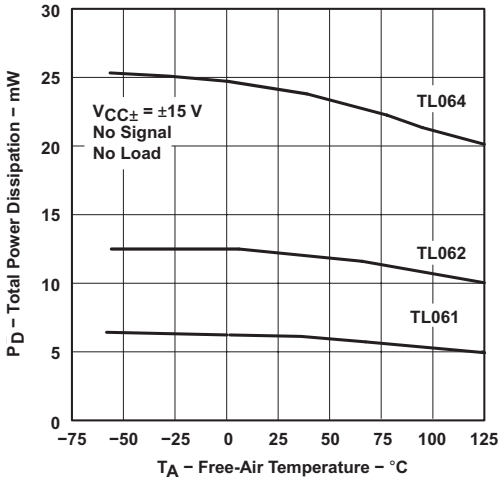


Figure 12. Total Power Dissipation vs Free-Air Temperature

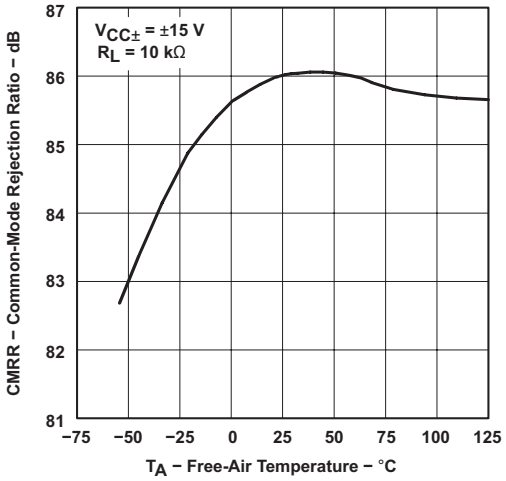


Figure 13. All Except TL06_C Common-Mode Rejection Ratio vs Free-Air Temperature

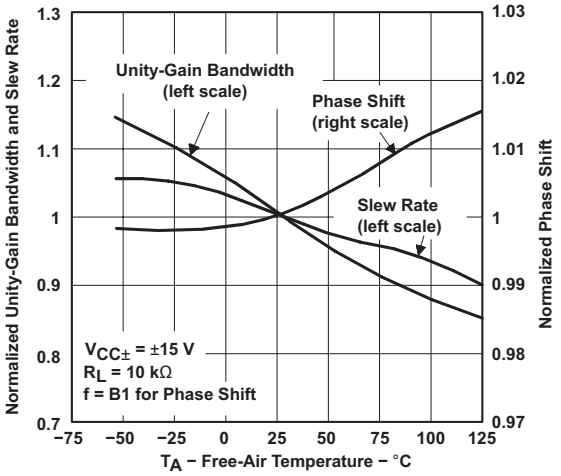


Figure 14. Normalized Unity-Gain Bandwidth, Slew Rate, and Phase Shift vs Free-Air Temperature

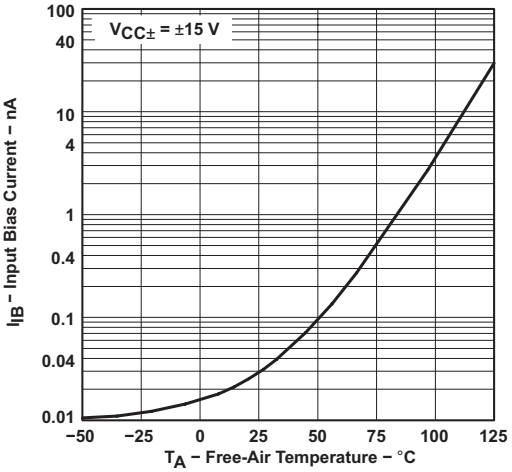


Figure 15. Input Bias Current vs Free-Air Temperature

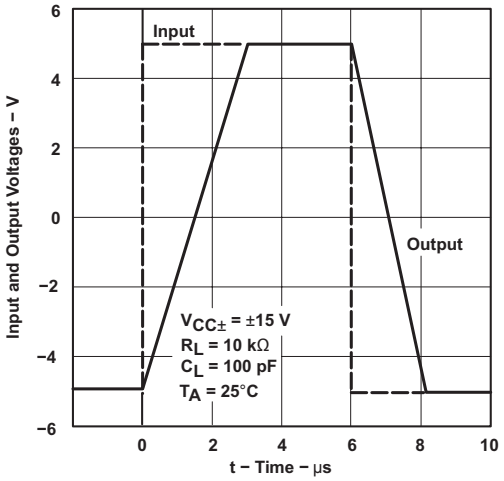


Figure 16. Voltage-Follower Large-Signal Pulse Response vs Time

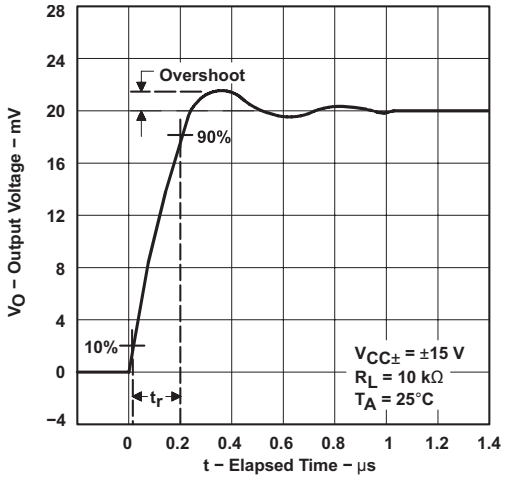


Figure 17. Output Voltage vs Elapsed Time

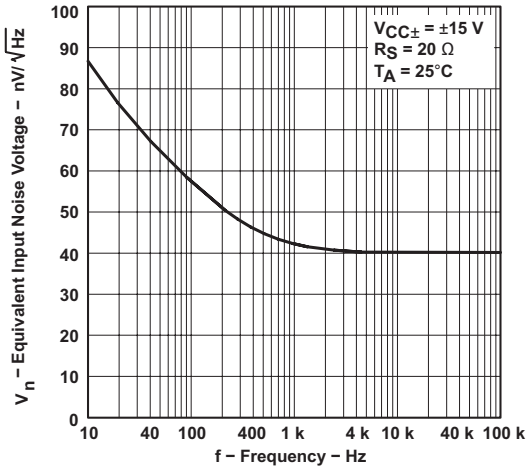


Figure 18. Equivalent Input Noise Voltage vs Frequency

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
Instrumentation amplifier	TL064	Figure 19
0.5-Hz square-wave oscillator	TL061	Figure 20
High-Q notch filter	TL061	Figure 21
Audio-distribution amplifier	TL064	Figure 22
Low-level light detector preamplifier	TL061	Figure 23
AC amplifier	TL061	Figure 24
Microphone preamplifier with tone control	TL061	Figure 25
Instrumentation amplifier	TL062	Figure 26
IC preamplifier	TL062	Figure 27

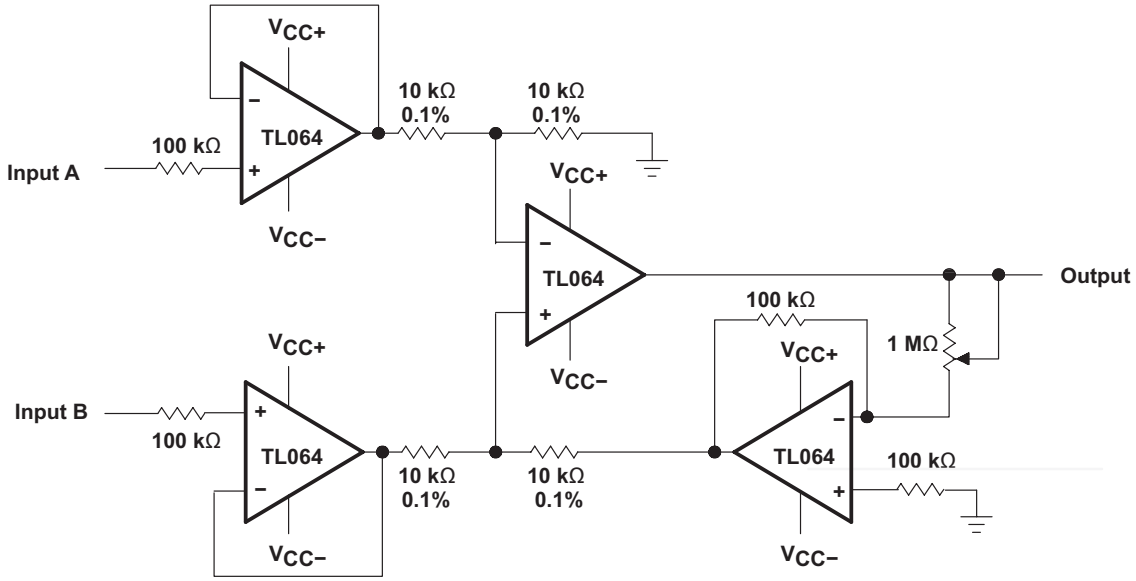


Figure 19. Instrumentation Amplifier

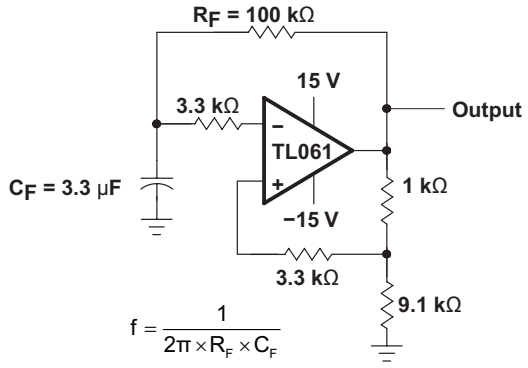


Figure 20. 0.5-Hz Square-Wave Oscillator

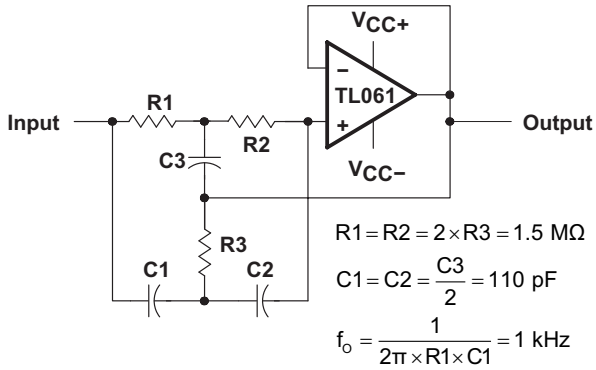


Figure 21. High-Q Notch Filter

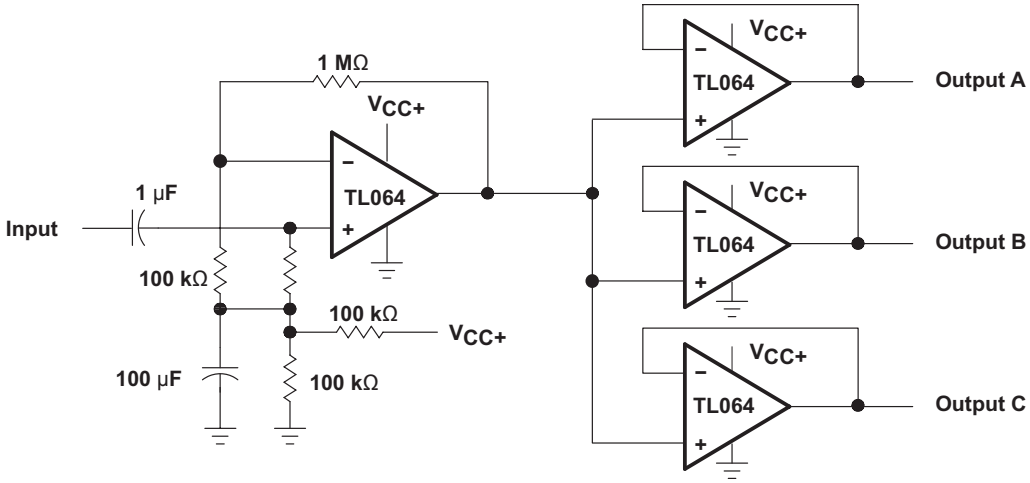


Figure 22. Audio-Distribution Amplifier

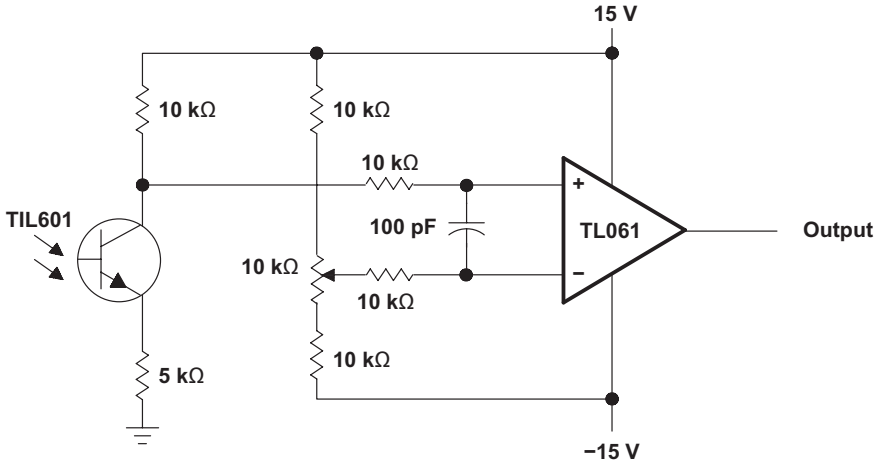


Figure 23. Low-Level Light Detector Preamplifier

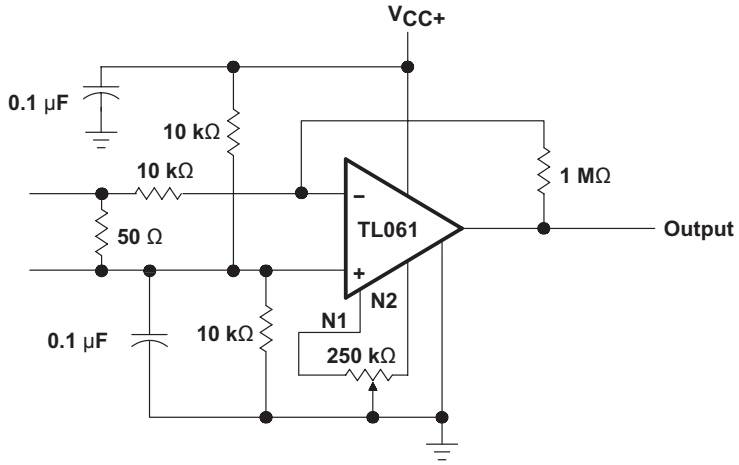


Figure 24. AC Amplifier

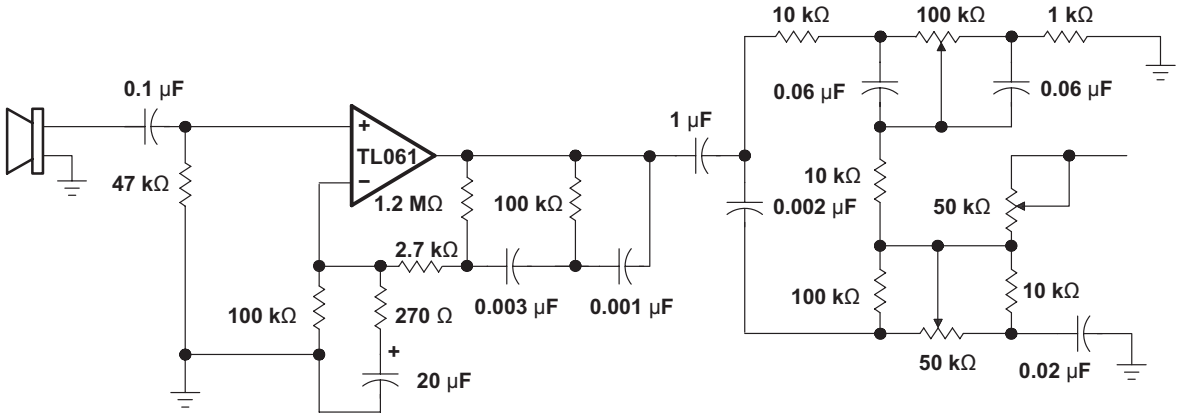


Figure 25. Microphone Preamplifier With Tone Control

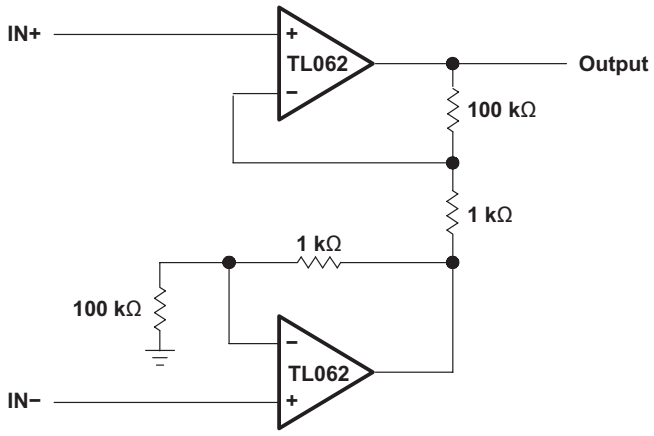


Figure 26. Instrumentation Amplifier

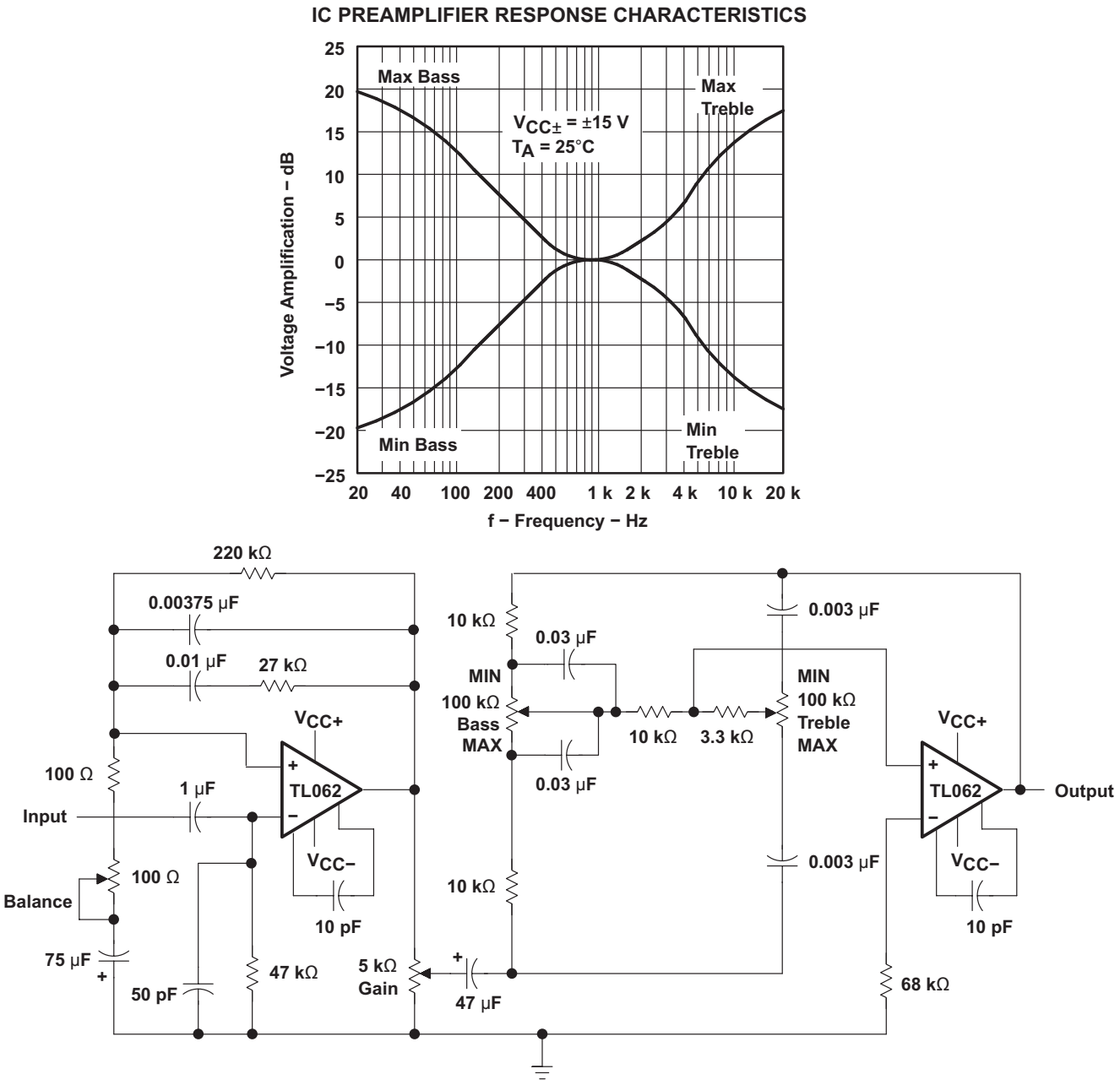


Figure 27. IC Preamplifier

REVISION HISTORY

Changes from Revision J (September 2004) to Revision K	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Deleted Ordering Information table.	1
• Updated Features.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023012A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
81023022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	Samples
8102302HA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102302HA TL062M	Samples
8102302PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102302PA TL062M	Samples
81023032A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	Samples
8102303CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	Samples
8102303DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	Samples
TL061ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	Samples
TL061ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	Samples
TL061ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	061AC	Samples
TL061ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061ACP	Samples
TL061ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061ACP	Samples
TL061BCD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		
TL061BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061BCP	Samples
TL061BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061BCP	Samples
TL061CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	Samples
TL061CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL061C	Samples
TL061CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL061CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL061CP	Samples
TL061CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T061	Samples
TL061CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL061ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	Samples
TL061IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	Samples
TL061IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL061I	Samples
TL061IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL061IP	Samples
TL061IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL061IP	Samples
TL061MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL061MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL062ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062AC	Samples
TL062ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL062ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062ACP	Samples
TL062ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062ACP	Samples
TL062ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062A	Samples
TL062ACPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	Samples
TL062BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	Samples
TL062BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	062BC	Samples
TL062BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062BCP	Samples
TL062BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062BCP	Samples
TL062CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL062C	Samples
TL062CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL062CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062CP	Samples
TL062CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL062CP	Samples
TL062CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL062CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL062CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL062CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T062	Samples
TL062ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	Samples
TL062IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	Samples
TL062IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	Samples
TL062IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL062I	Samples
TL062IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
TL062IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL062IP	Samples
TL062IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL062IP	Samples
TL062IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z062	Samples
TL062IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z062	Samples
TL062MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023022A TL062MFKB	Samples
TL062MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL062MJG	Samples
TL062MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102302PA TL062M	Samples
TL064ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	Samples
TL064ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	Samples
TL064ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	Samples
TL064ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL064ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064ACN	Samples
TL064ACP	NRND	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LF444ACN	
TL064BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	Samples
TL064BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	Samples
TL064BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064BC	Samples
TL064BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064BCN	Samples
TL064BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064BCN	Samples
TL064BCP	NRND	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LF444ACN	
TL064CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064C	Samples
TL064CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064CN	Samples
TL064CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL064CN	Samples
TL064CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064	Samples
TL064CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL064	Samples
TL064CP	NRND	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LF444CN	
TL064CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL064CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples
TL064CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples
TL064CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70		
TL064CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples
TL064CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T064	Samples
TL064ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL064IN	Samples
TL064INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL064IN	Samples
TL064INS	ACTIVE	SO	NS	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064INSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL064I	Samples
TL064IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z064	Samples
TL064MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL064MFK	Samples
TL064MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023032A TL064MFKB	Samples
TL064MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL064MJ	Samples
TL064MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303CA TL064MJB	Samples
TL064MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102303DA TL064MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL062, TL062M, TL064, TL064M :

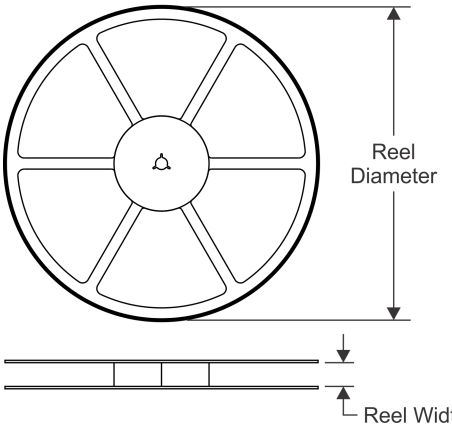
- Catalog: TL062, TL064
- Military: TL062M, TL064M

NOTE: Qualified Version Definitions:

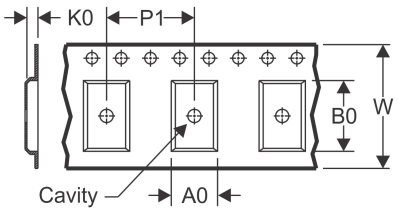
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

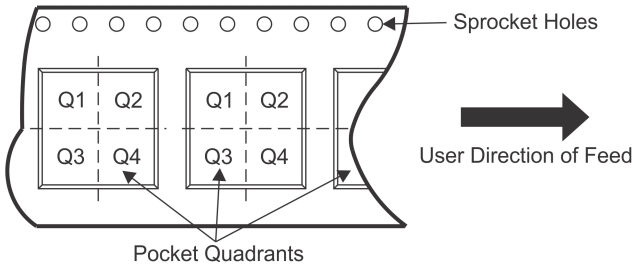


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

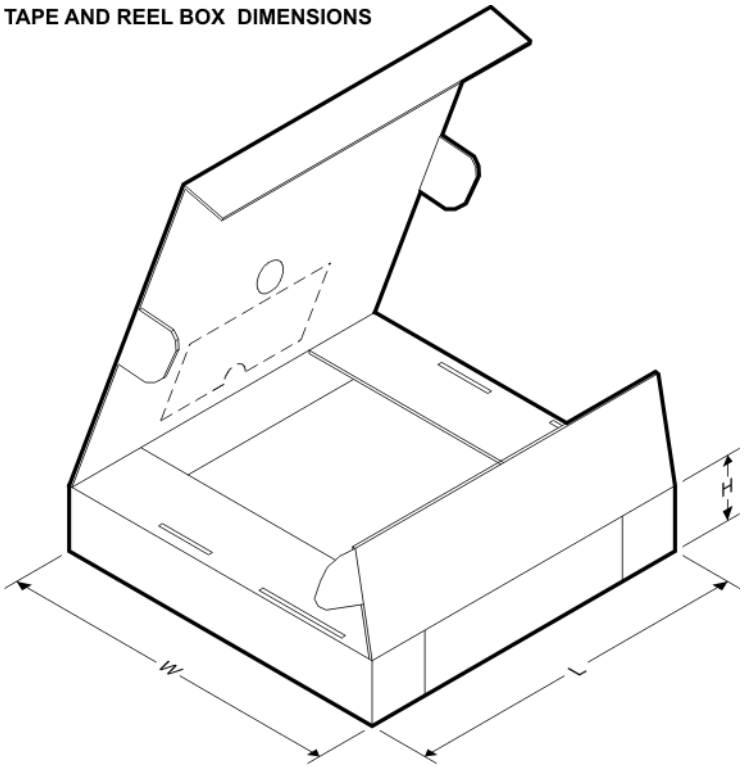


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL061ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL062BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064INSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



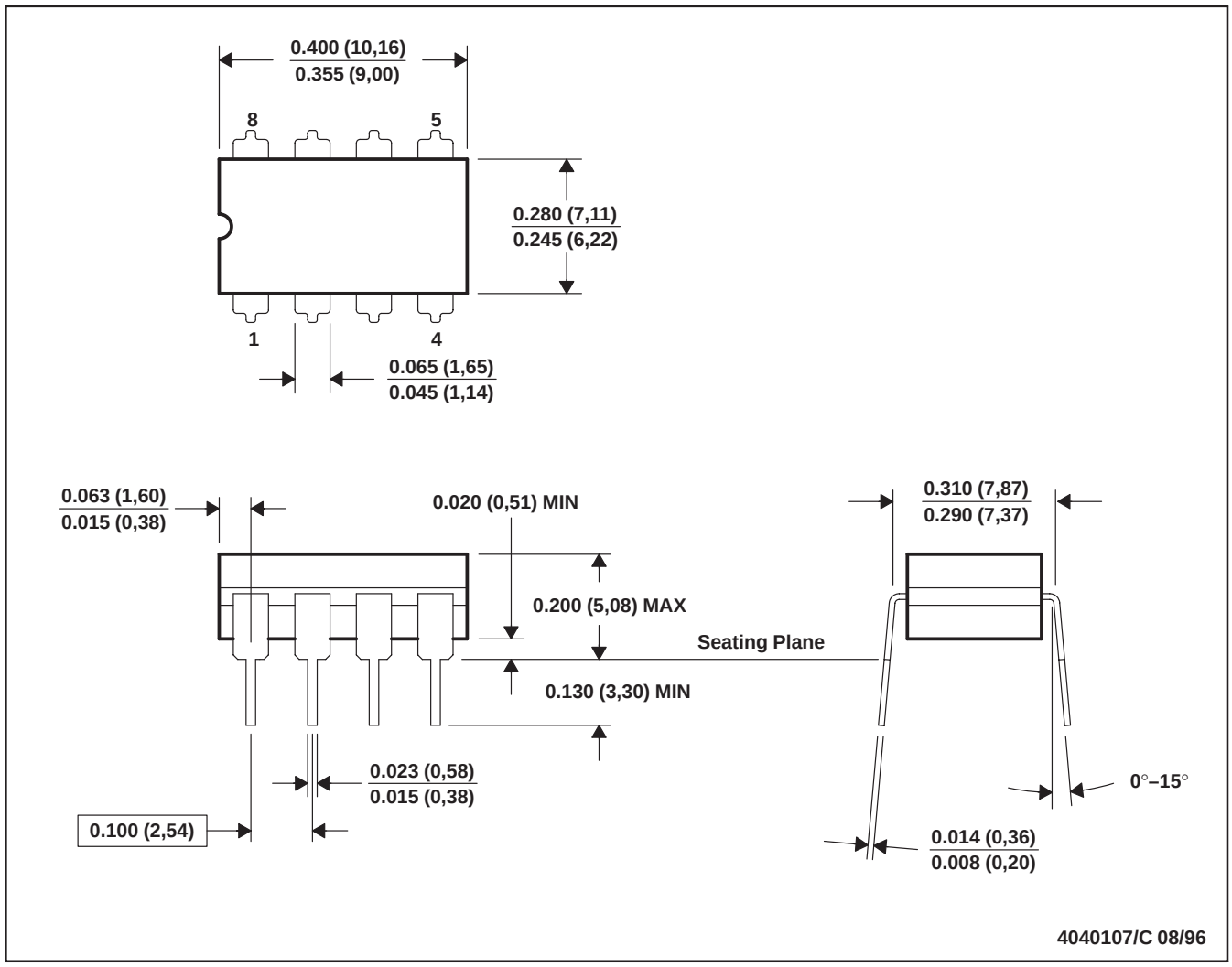
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL061ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL061IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL062BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL062IDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL062IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL064ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064BCDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL064IDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064IDRG4	SOIC	D	14	2500	367.0	367.0	38.0
TL064INSR	SO	NS	14	2000	367.0	367.0	38.0
TL064IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

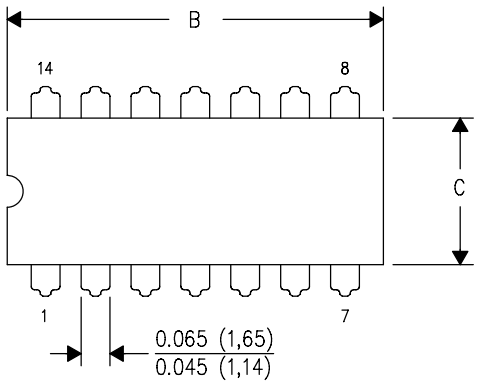


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

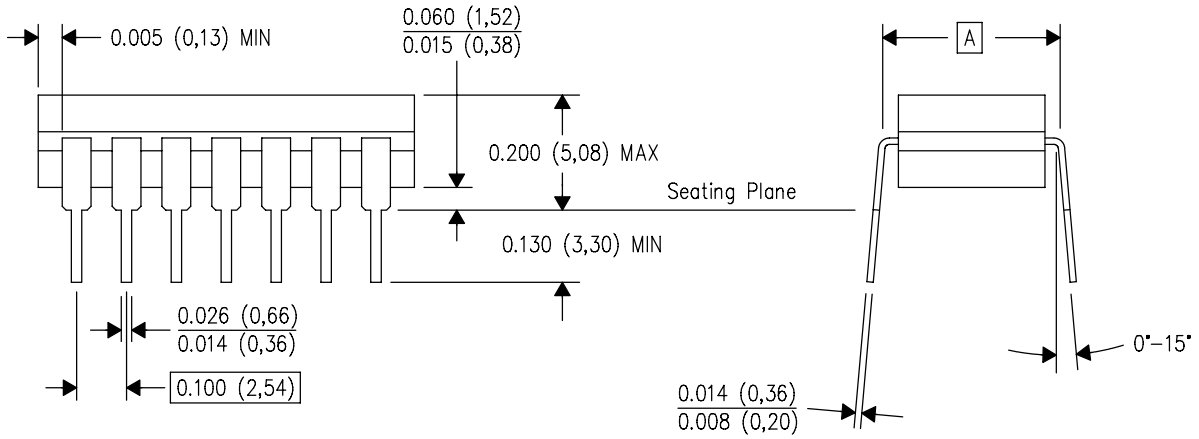
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



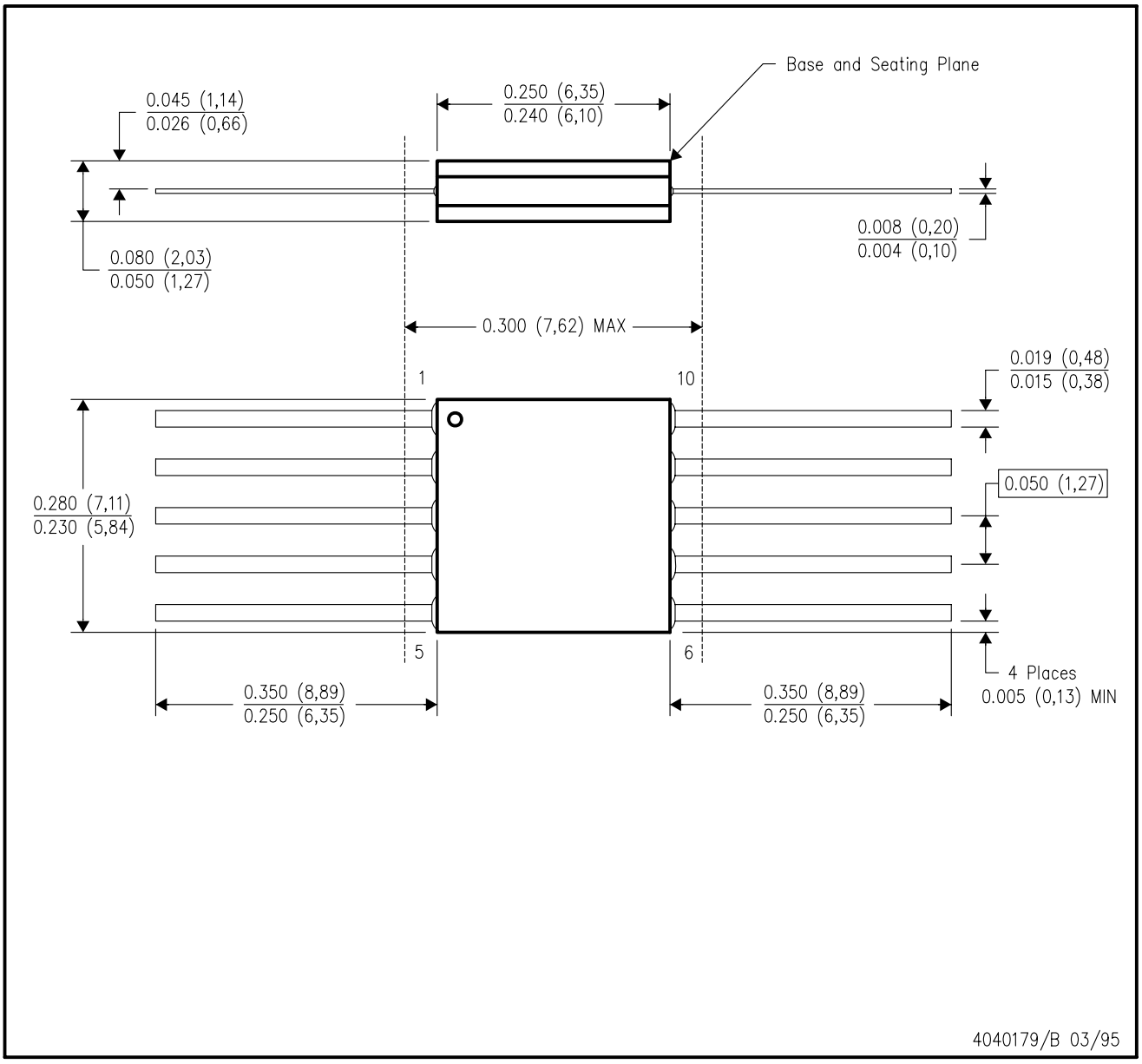
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

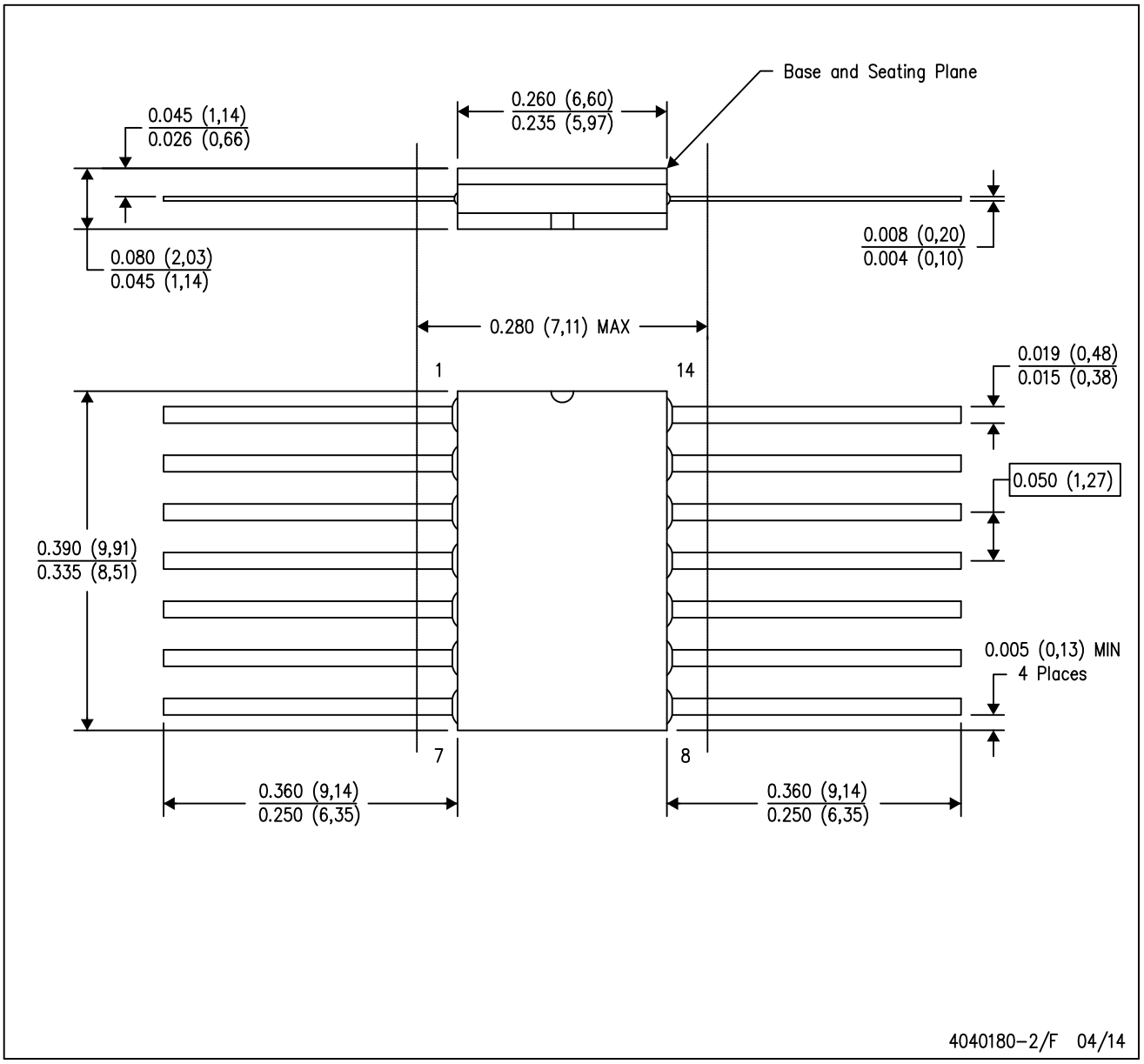
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

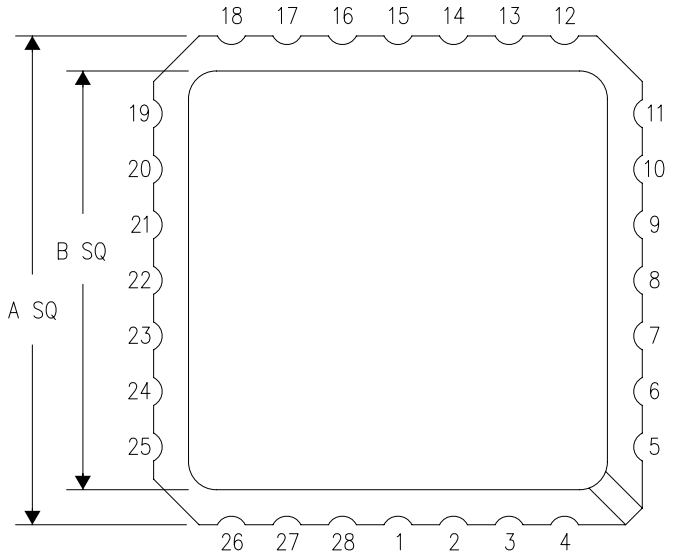
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



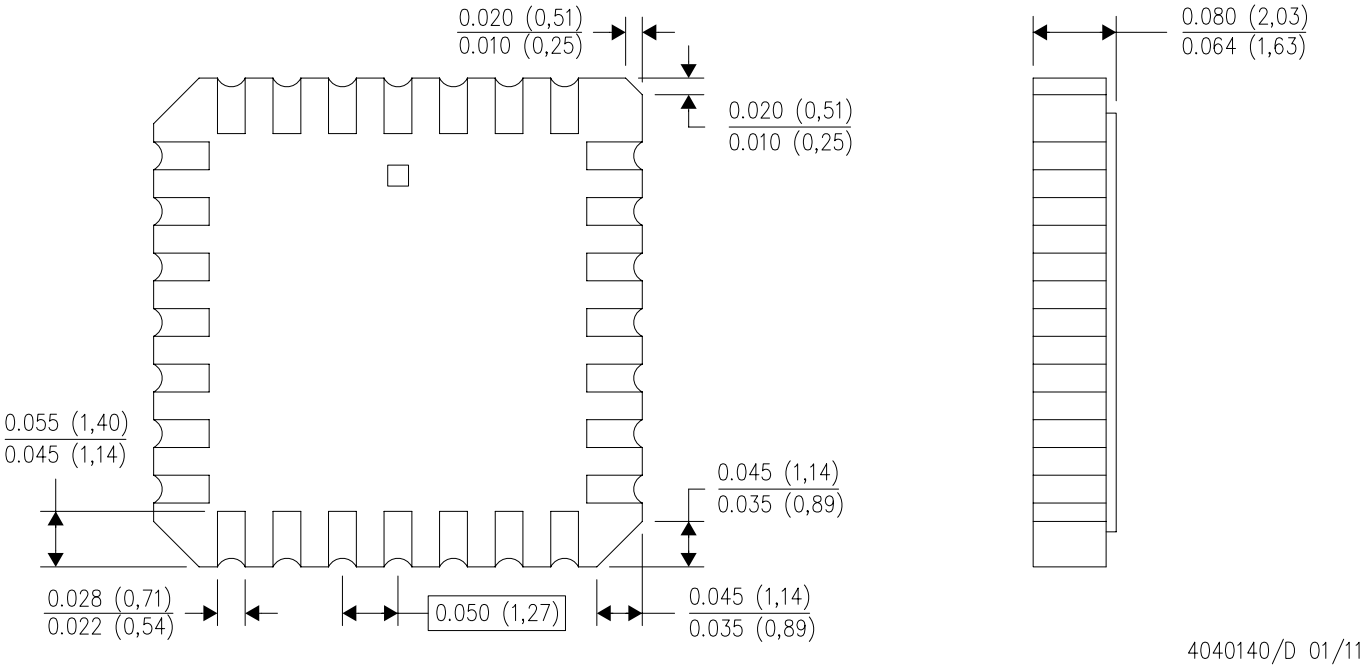
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



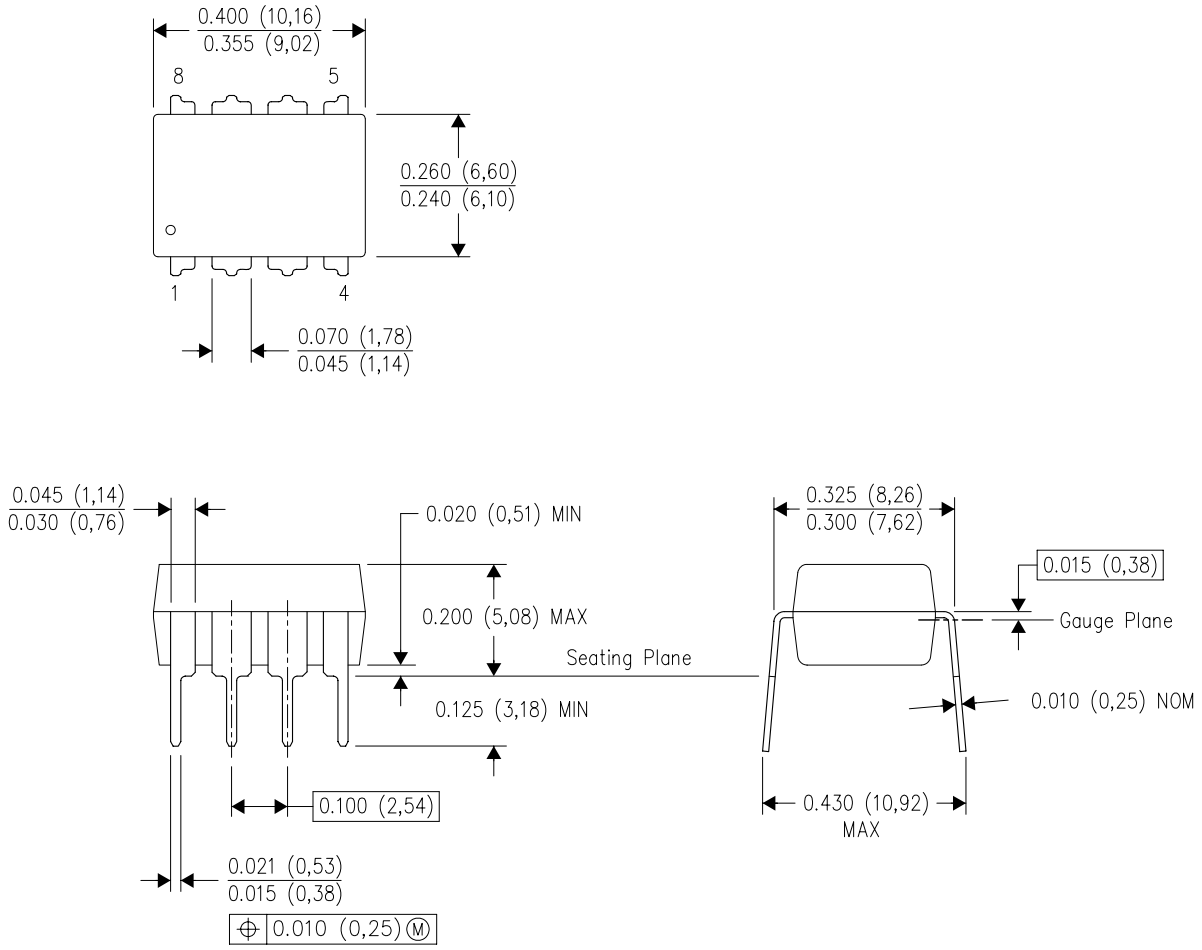
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

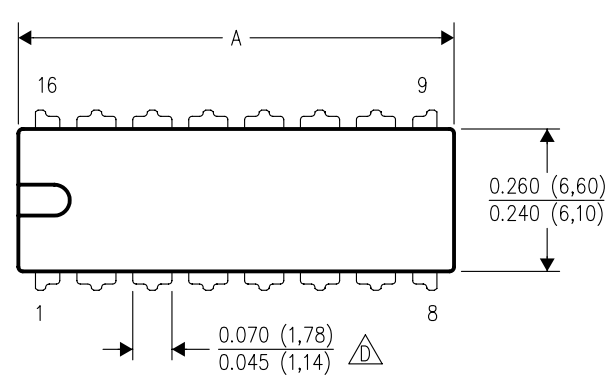


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

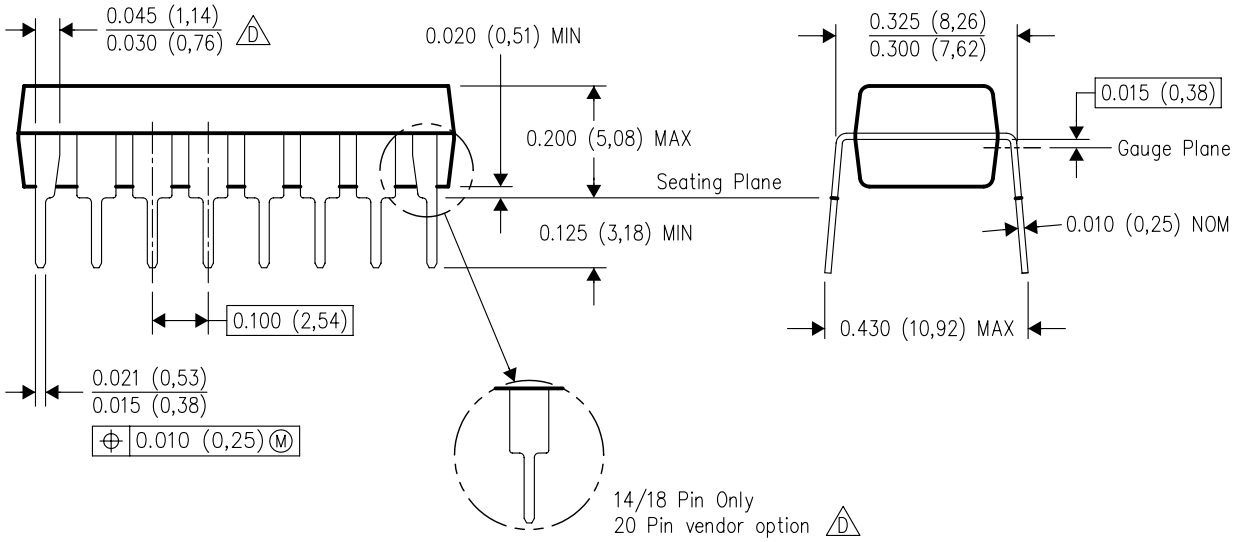
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



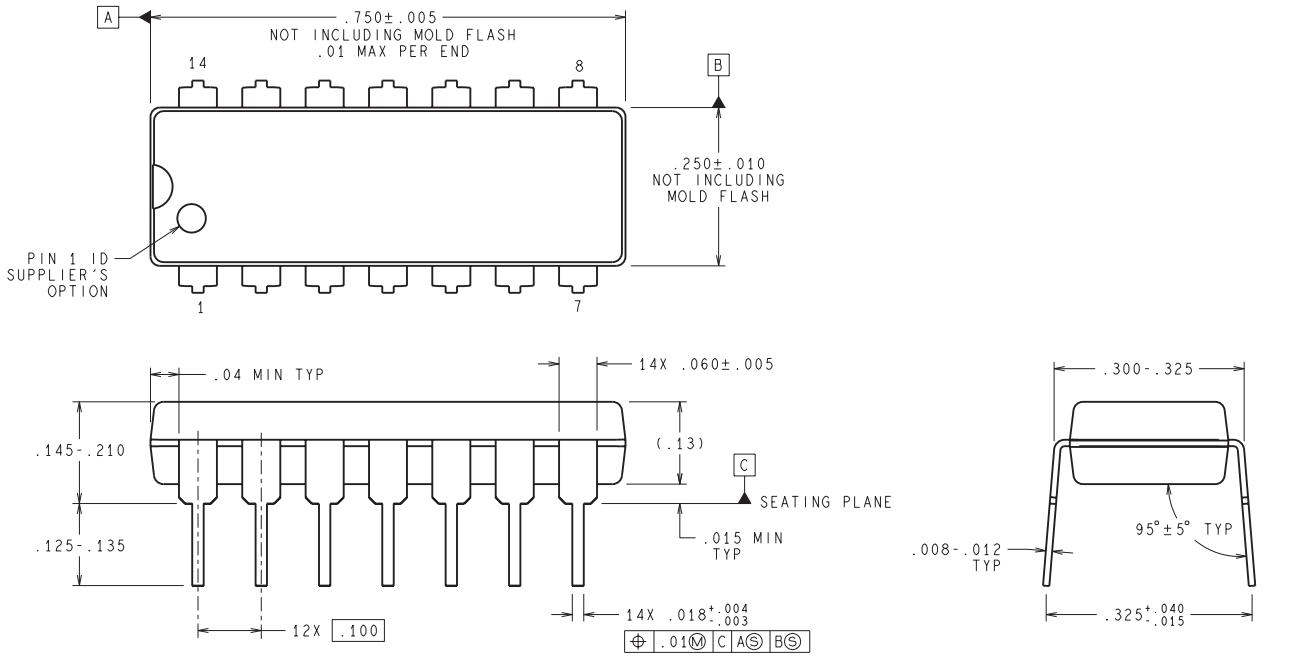
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

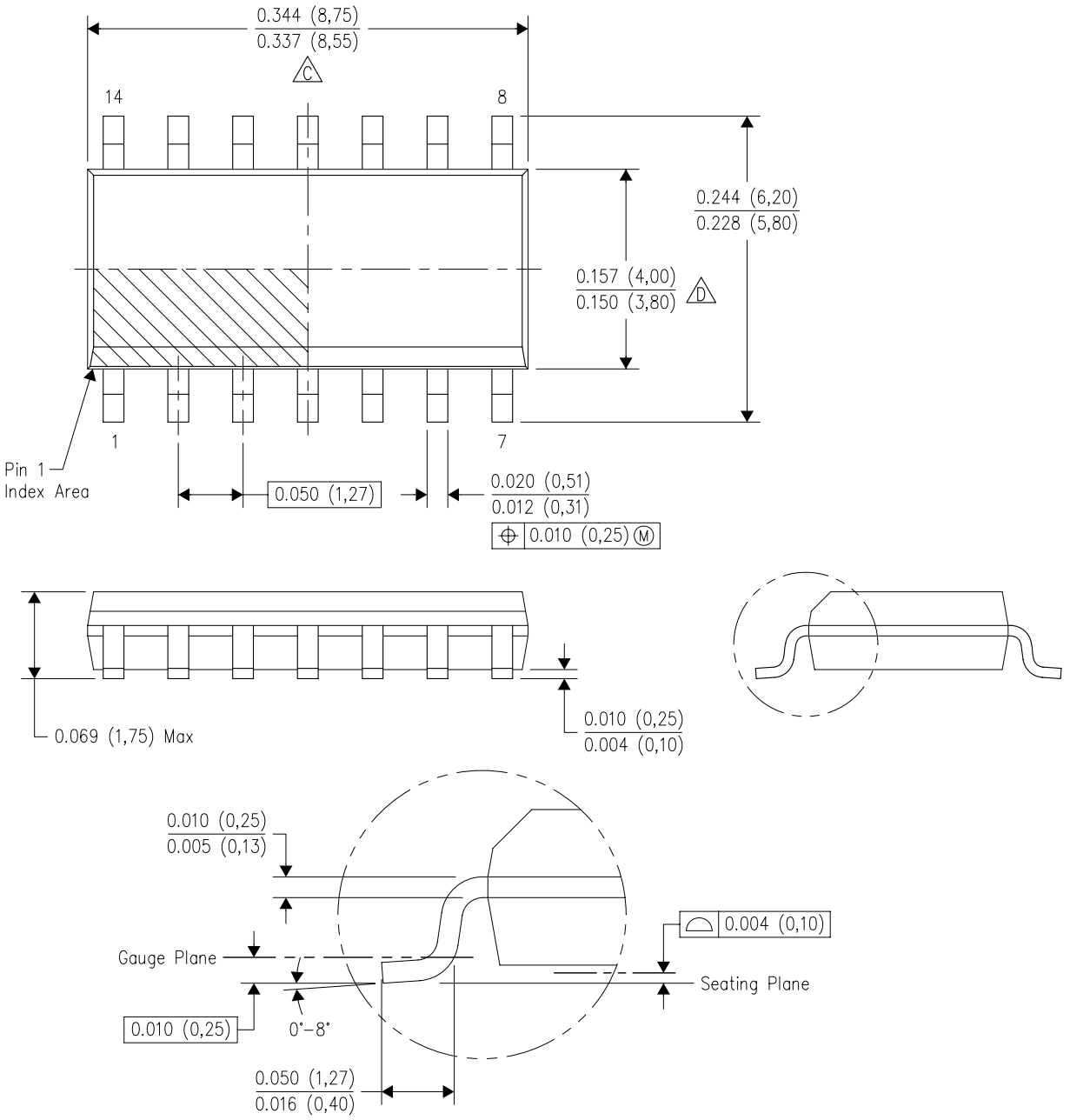
NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

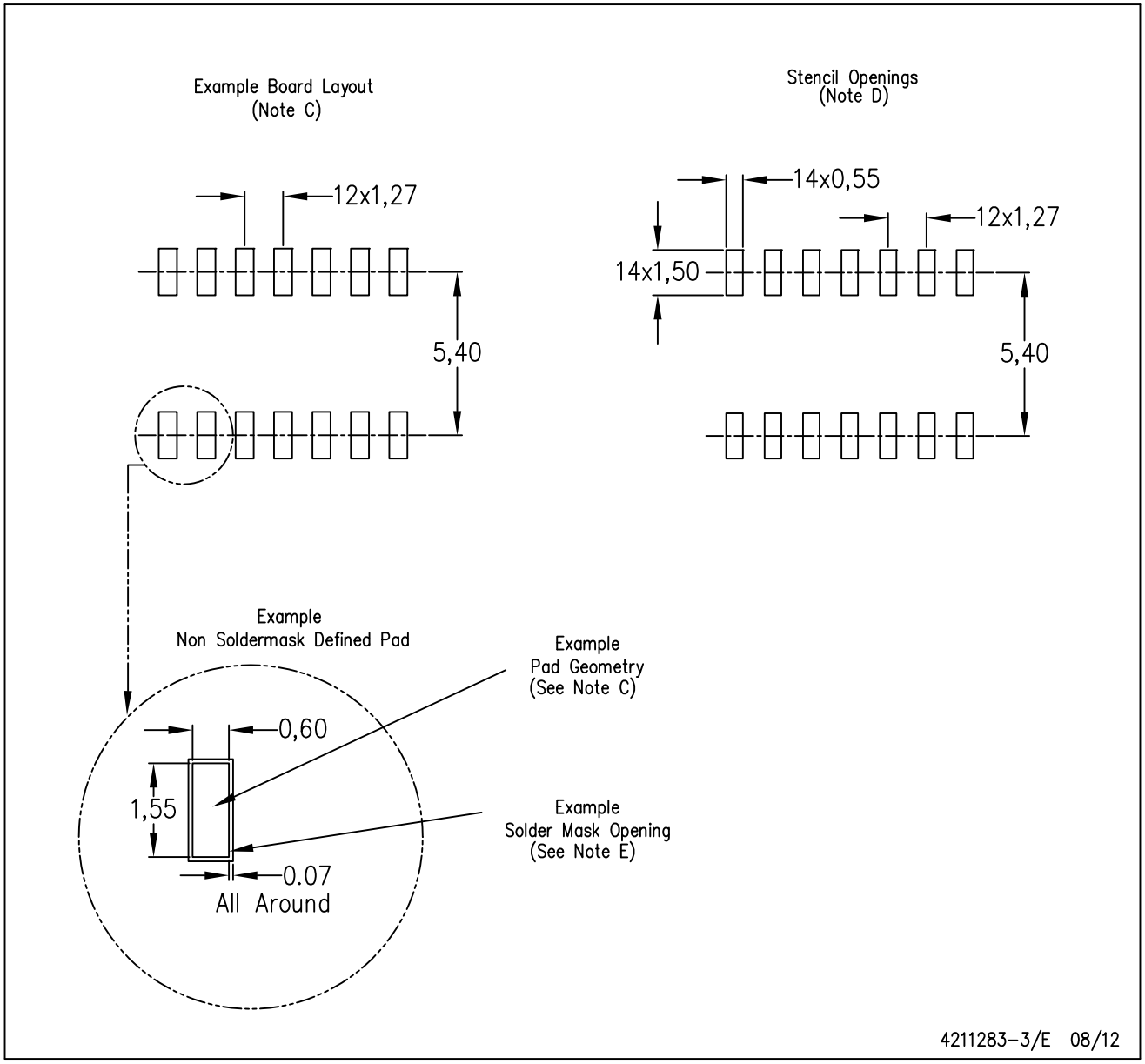
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

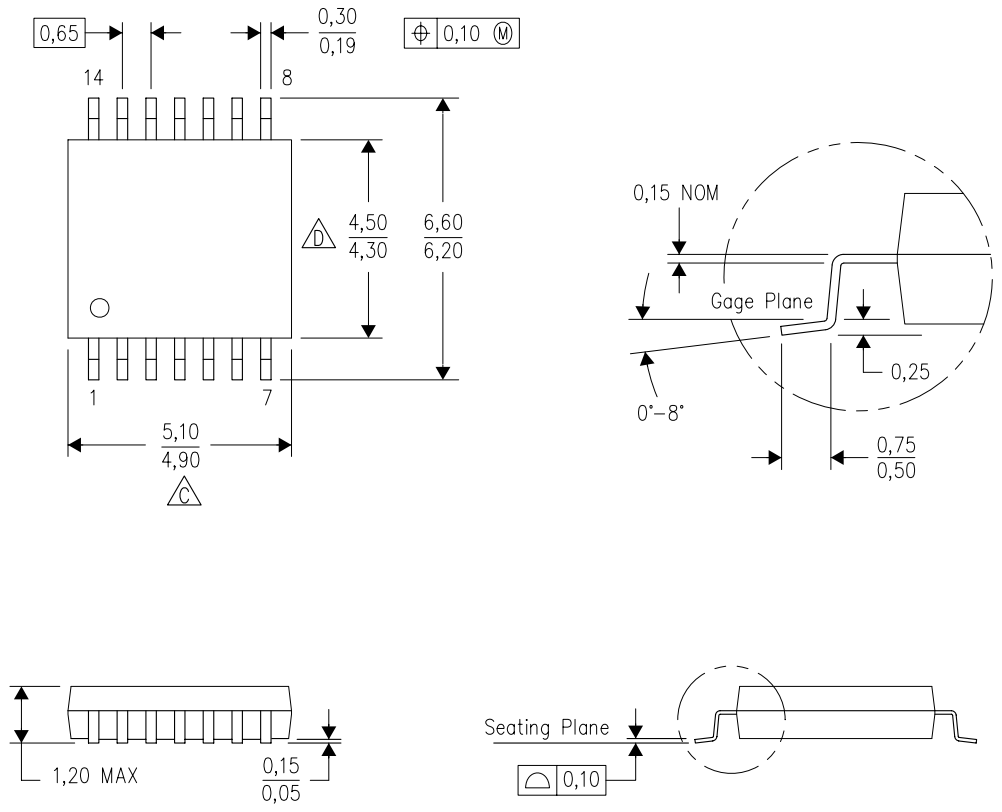
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

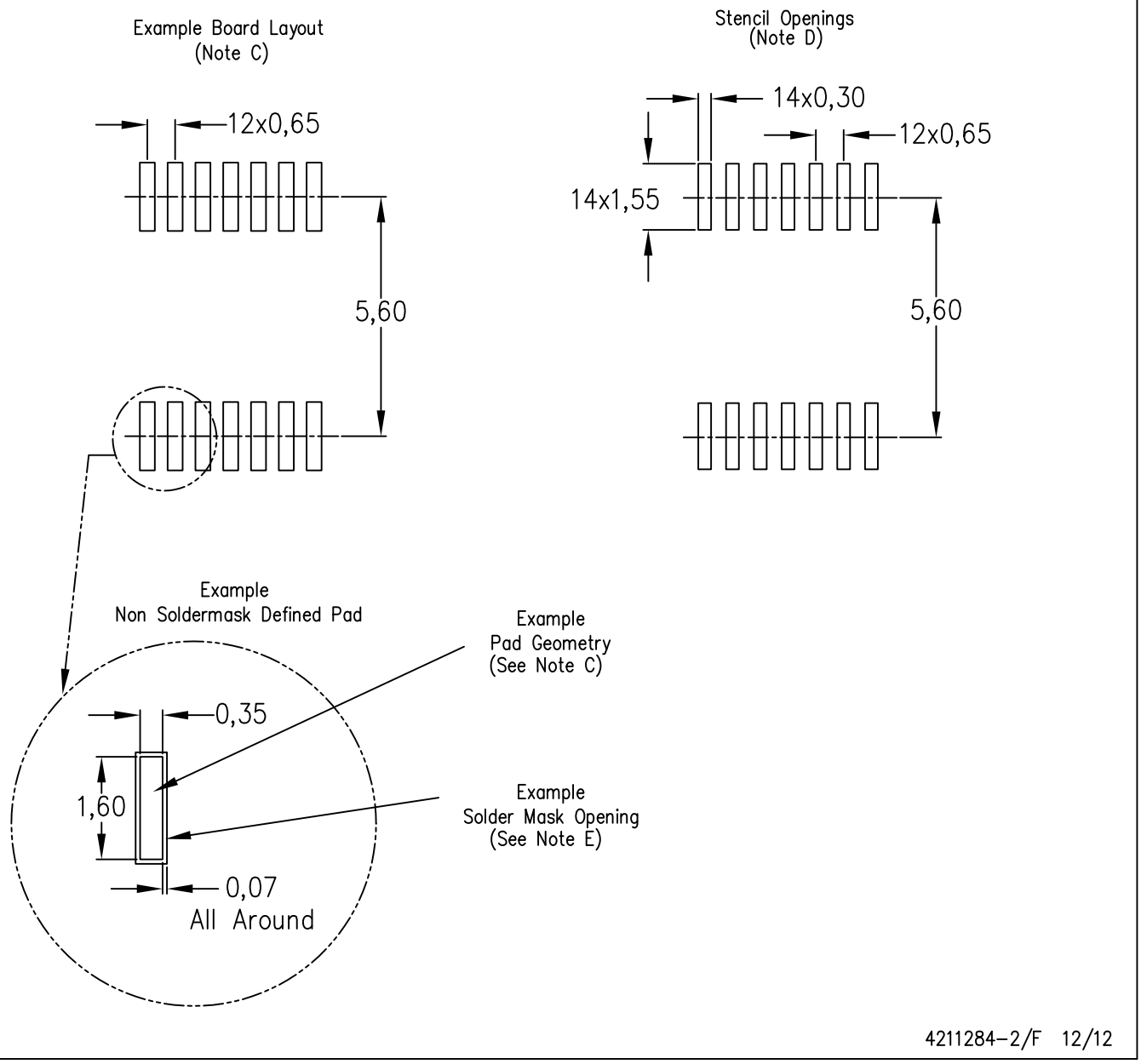
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

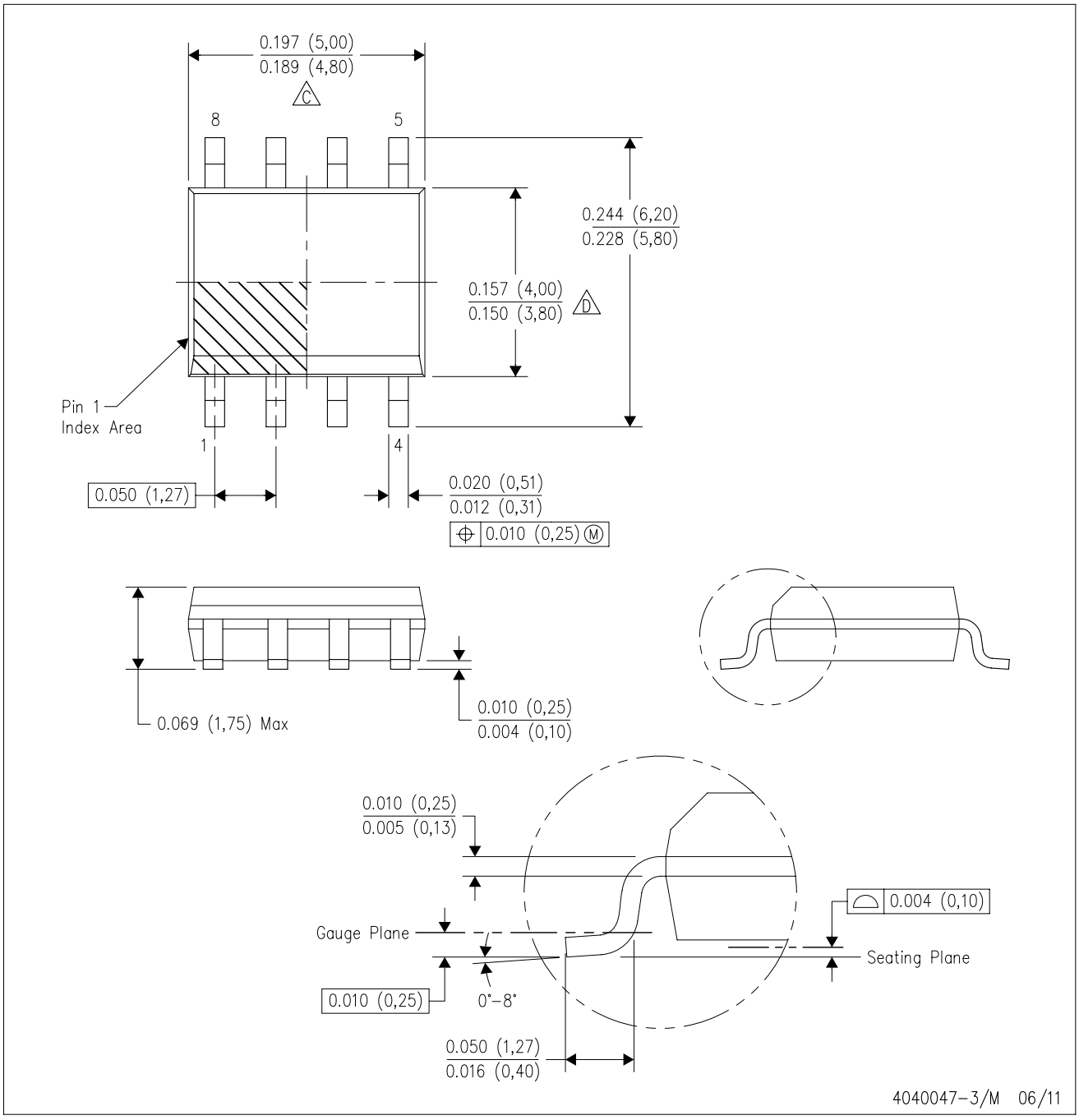
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



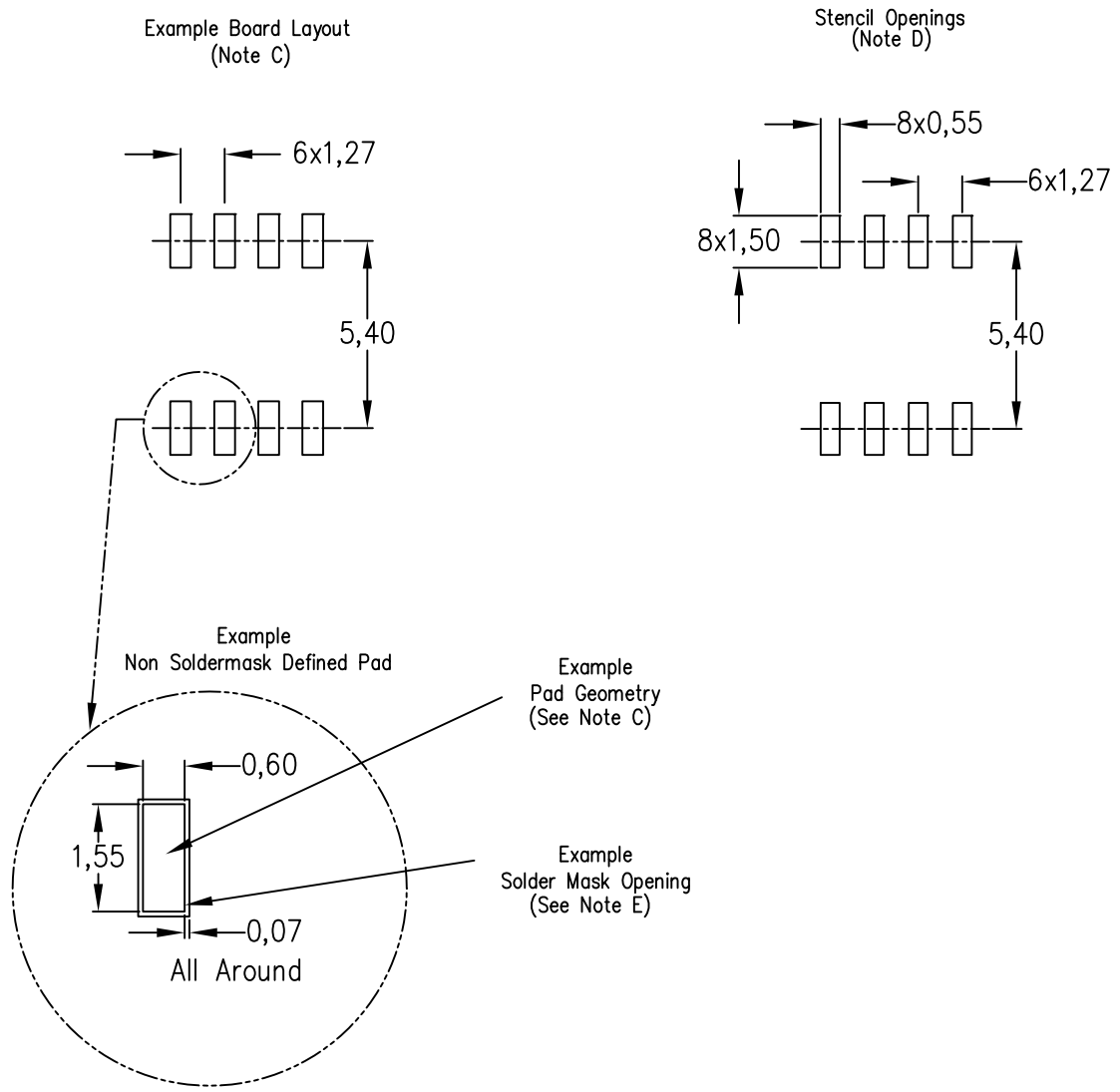
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

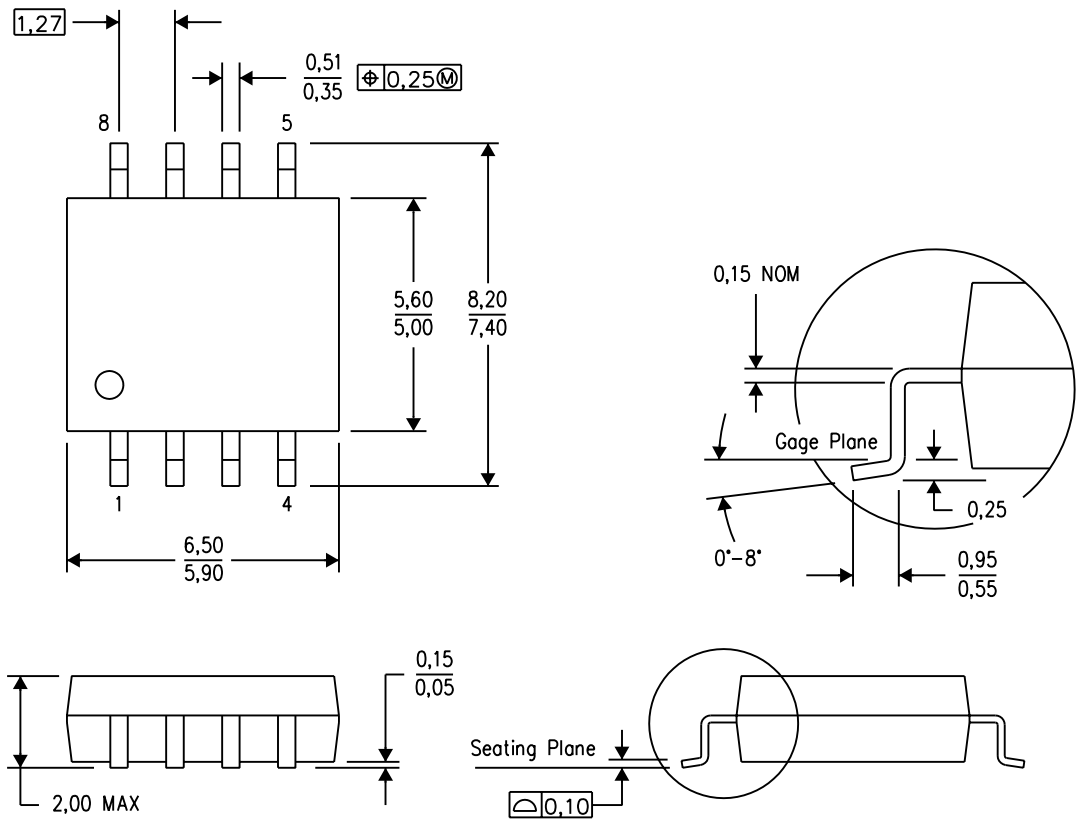
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

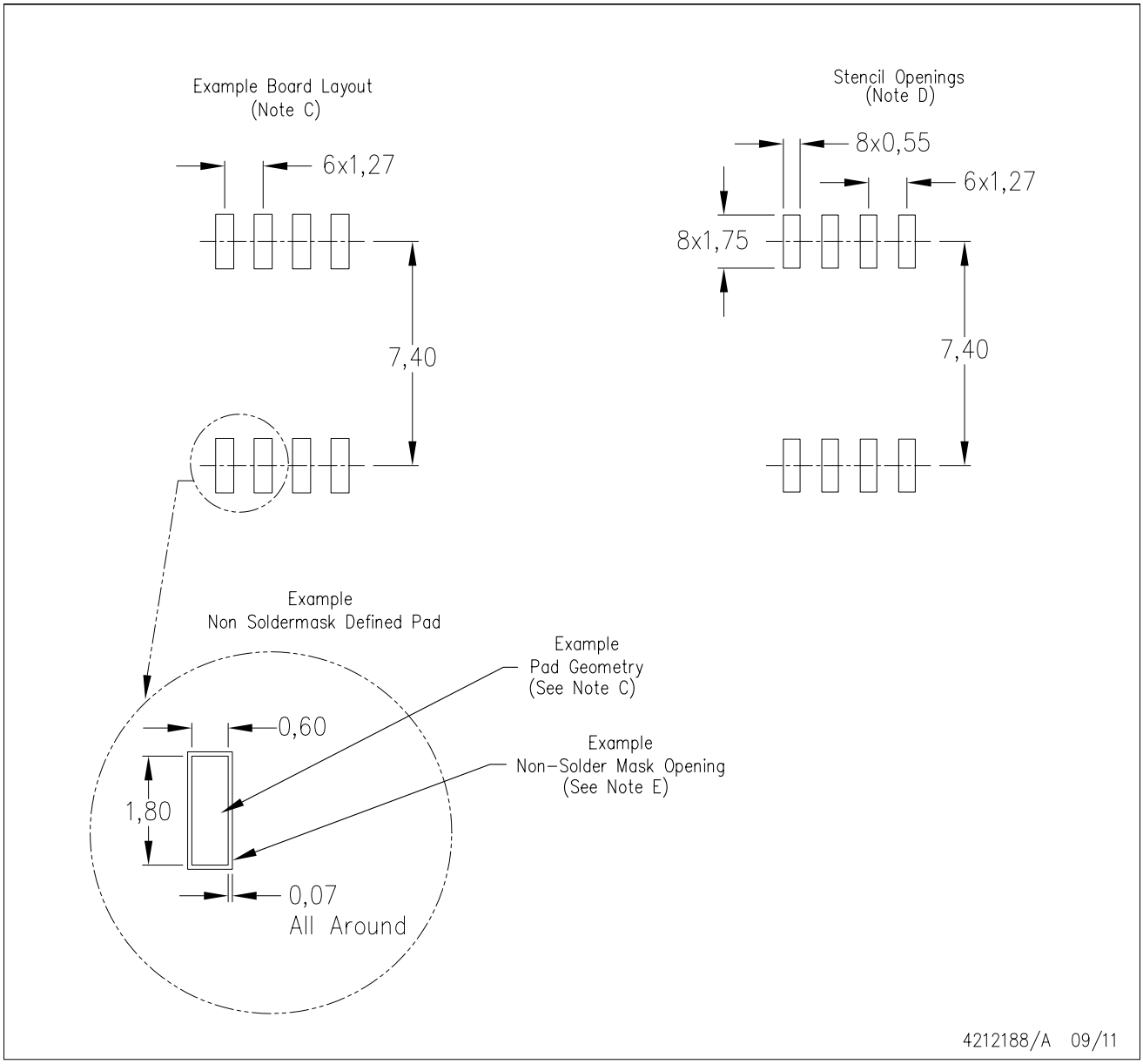
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE

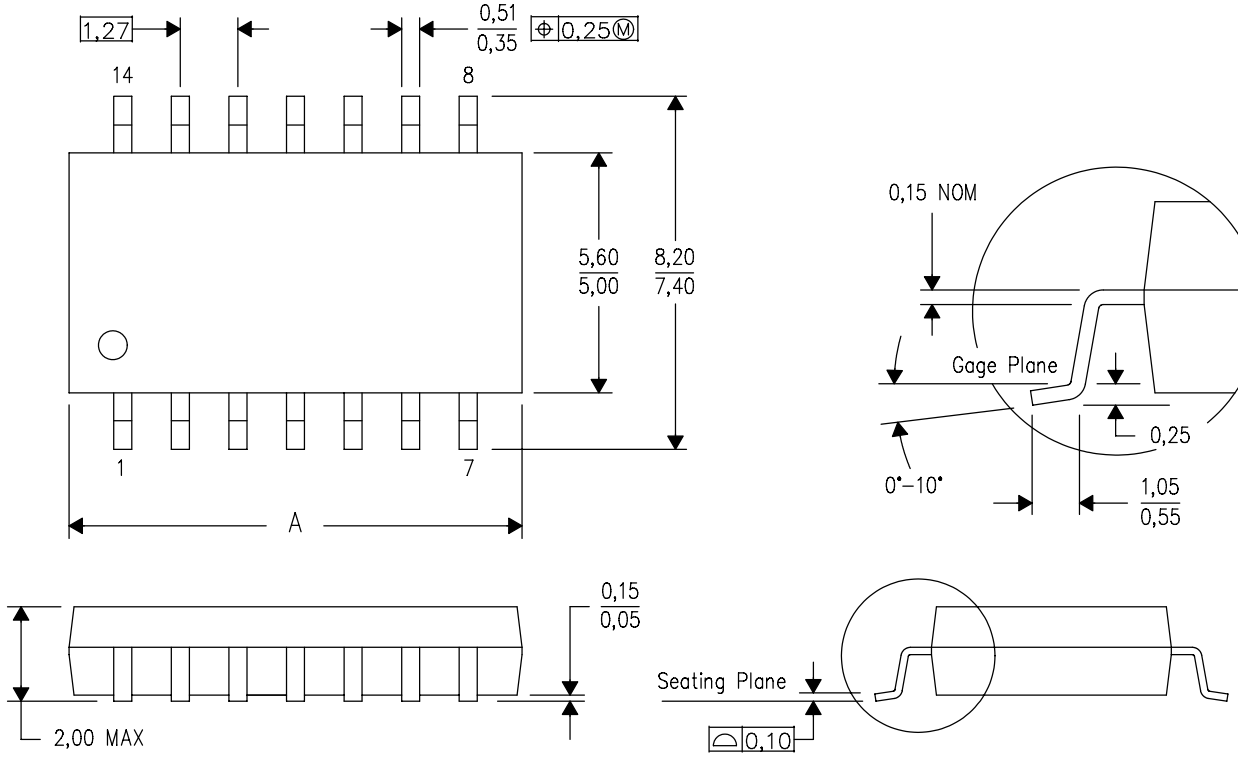


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

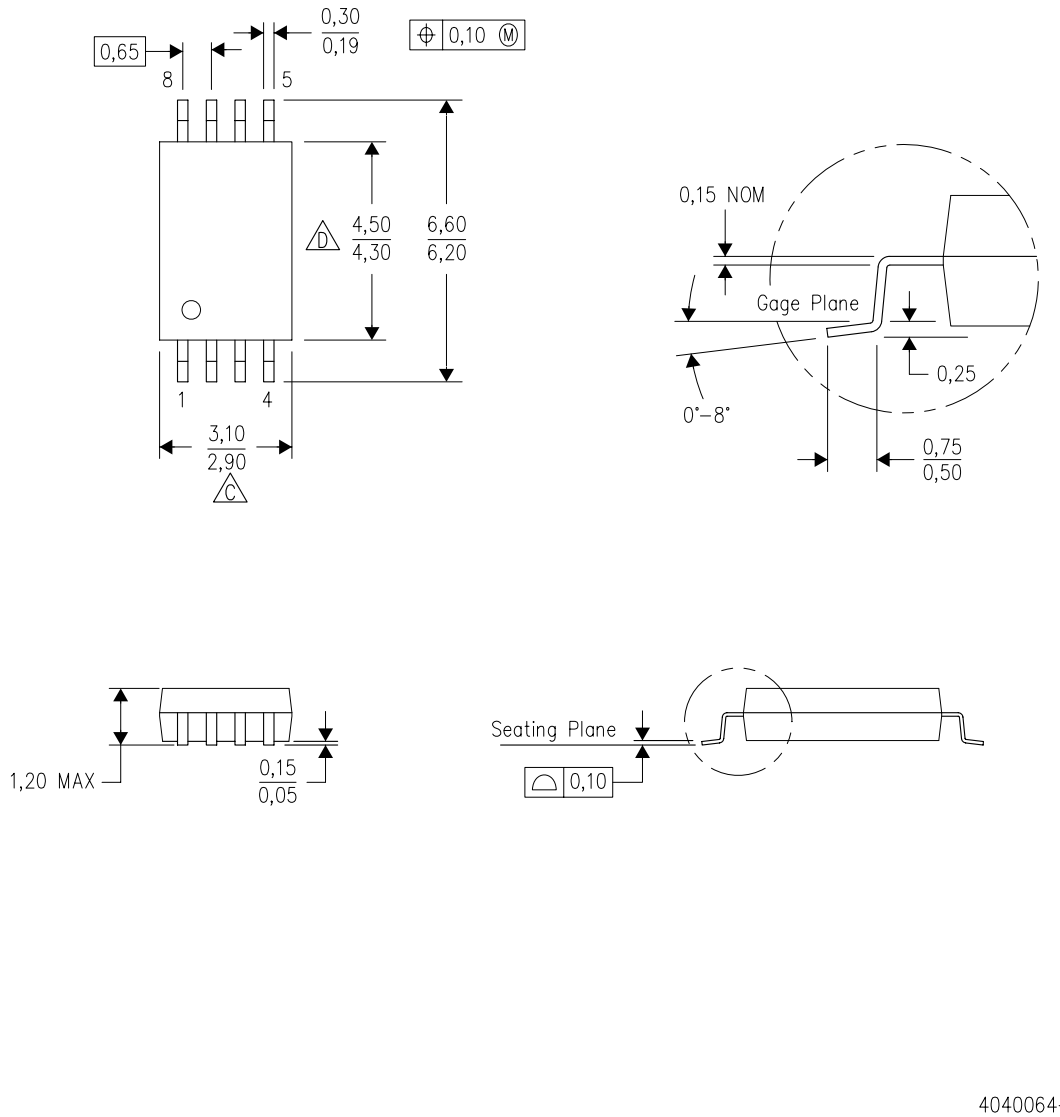


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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