

## TL08xx JFET-Input Operational Amplifiers

 Check for Samples: [TL081](#), [TL081A](#), [TL081B](#), [TL082](#), [TL082A](#), [TL082B](#), [TL084](#), [TL084A](#), [TL084B](#)

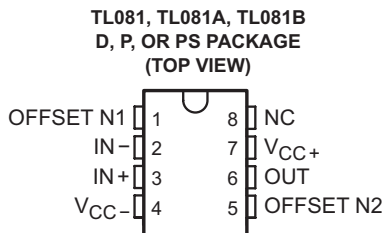
### FEATURES

- **Low Power Consumption: 1.4 mA/ch Typ**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias Current: 30 pA Typ**
- **Low Input Offset Current: 5 pA Typ**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion: 0.003% Typ**
- **High Input Impedance: JFET Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate: 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes  $V_{CC+}$**

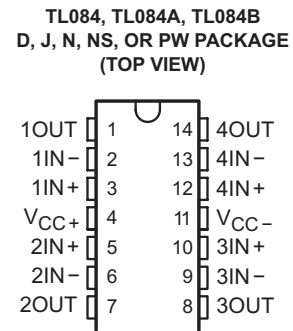
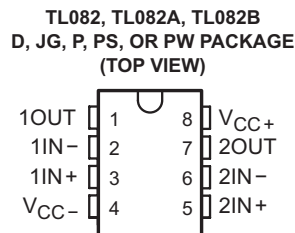
### DESCRIPTION

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

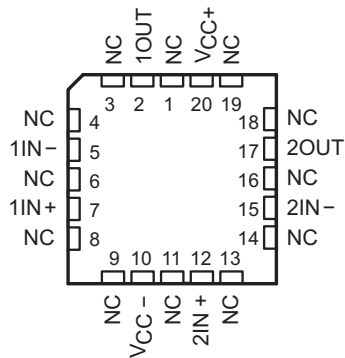
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The Q-suffix devices are characterized for operation from -40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.



NC – No internal connection

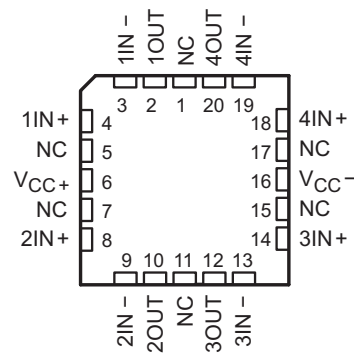


**TL082M . . . FK PACKAGE**  
(TOP VIEW)



NC – No internal connection

**TL084M . . . FK PACKAGE**  
(TOP VIEW)



NC – No internal connection



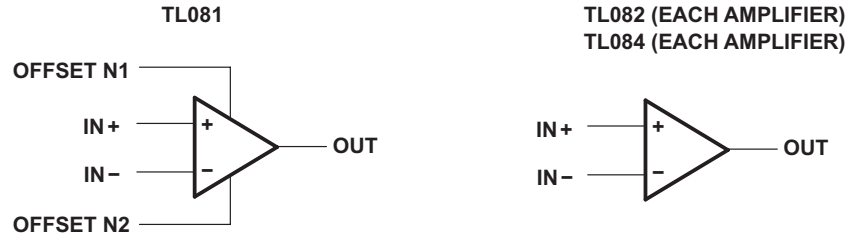
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



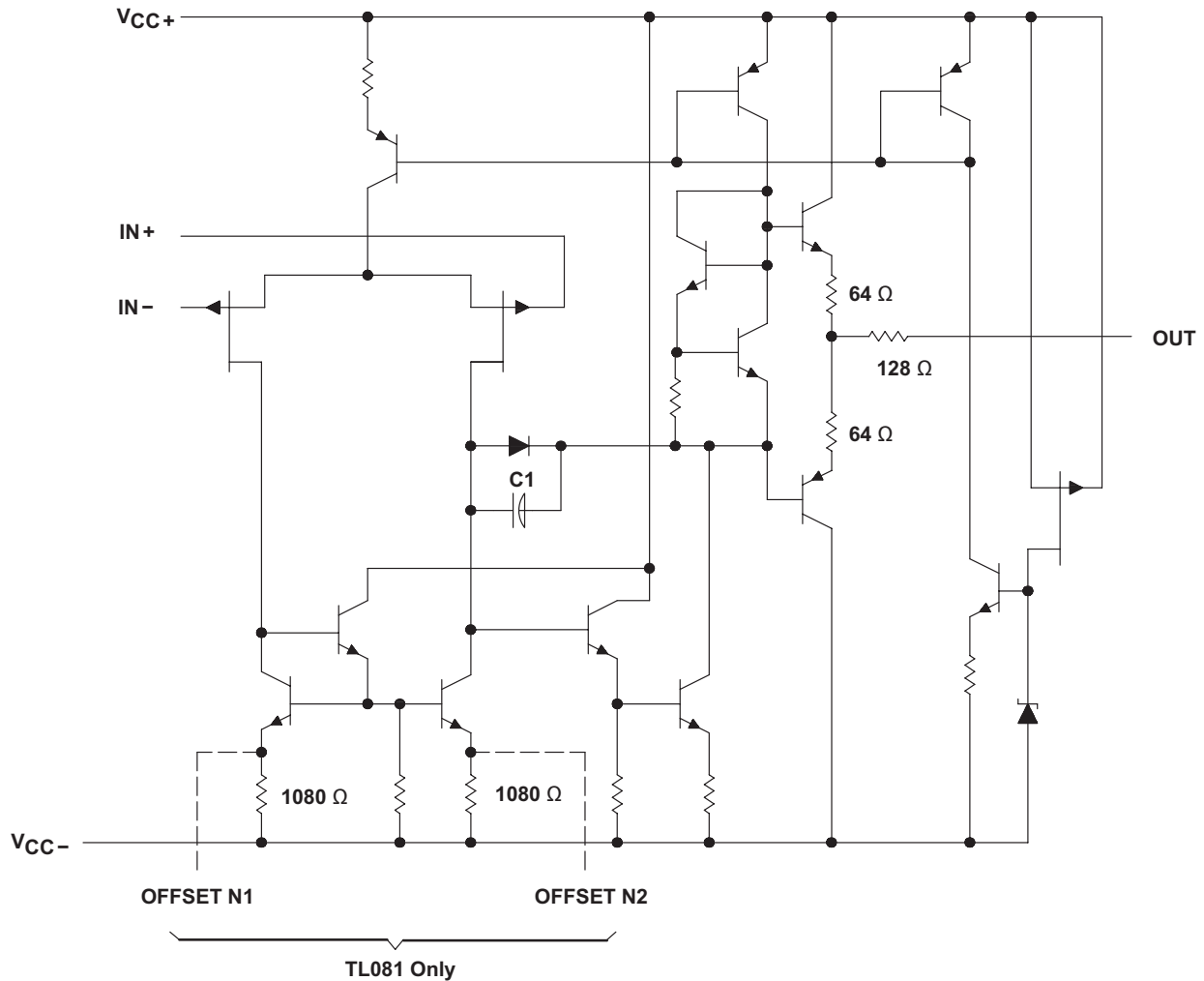
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Symbols



## Schematic (Each Amplifier)



Component values shown are nominal.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT	
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>	18	18	18	18	V	
V <sub>CC-</sub>		-18	-18	-18	-18		
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>	±30	±30	±30	±30	V	
V <sub>I</sub>	Input voltage <sup>(2)(4)</sup>	±15	±15	±15	±15	V	
Duration of output short circuit <sup>(5)</sup>		Unlimited	Unlimited	Unlimited	Unlimited		
Continuous total power dissipation		See Dissipation Rating Table					
T <sub>A</sub>	Operating free-air temperature range	0 to 70	-40 to 85	-40 to 125	-55 to 125	°C	
θ <sub>JA</sub>	Package thermal impedance <sup>(6)(7)</sup>	D package (8-pin)	97	97		97	°C/W
		D package (14-pin)	86	86		86	
		N package (14-pin)	76	76		80	
		NS package (14-pin)	80			76	
		P package	85	85		85	
		PS package	95	95		95	
		PW package (8 pin)	149			149	
		PW package (14 pin)	113	113		113	
Operating virtual junction temperature		150	150	150	150	°C	
T <sub>C</sub>	Case temperature for 60 seconds	FK package			260	°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package			300	°C	
T <sub>stg</sub>	Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C	

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- Differential voltages are at IN+, with respect to IN-.
- The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

### Dissipation Rating Table

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T <sub>A</sub>	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW

## Electrical Characteristics

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$ <sup>(1)</sup>	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_O = 0$ , $R_S = 50\ \Omega$	25°C		3	15	3	6	2	3	3	6	mV		
			Full range		20			7.5			5				
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_O = 0$ , $R_S = 50\ \Omega$	Full range		18			18			18			$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current <sup>(2)</sup>	$V_O = 0$	25°C		5	200	5	100	5	100	5	100	pA		
			Full range		2			2			10				
$I_{IB}$	Input bias current <sup>(2)</sup>	$V_O = 0$	25°C		30	400	30	200	30	200	30	200	pA		
			Full range		10			7			20				
$V_{ICR}$	Common-mode input voltage range		25°C		$\pm 11$	-12 to 15	$\pm 11$	-12 to 15	$\pm 11$	-12 to 15	$\pm 11$	-12 to 15	V		
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C		$\pm 12$	$\pm 13.5$	$\pm 12$	$\pm 13.5$	$\pm 12$	$\pm 13.5$	$\pm 12$	$\pm 13.5$	V		
		$R_L \geq 10\ \text{k}\Omega$	Full range		$\pm 12$			$\pm 12$			$\pm 12$				
		$R_L \geq 2\ \text{k}\Omega$	Full range		$\pm 10$			$\pm 12$			$\pm 10$				
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ , $R_L \geq 2\ \text{k}\Omega$	25°C		25	200	50	200	50	200	50	200	V/mV		
			Full range		15			15			25				
$B_1$	Unity-gain bandwidth		25°C		3			3			3			MHz	
$r_i$	Input resistance		25°C		$10^{12}$			$10^{12}$			$10^{12}$			$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\min}$ , $V_O = 0$ , $R_S = 50\ \Omega$	25°C		70	86	75	86	75	86	75	86	dB		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 15\ \text{V}$ to $\pm 9\ \text{V}$ , $V_O = 0$ , $R_S = 50\ \Omega$	25°C		70	86	80	86	80	86	80	86	dB		
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ , No load	25°C		1.4	2.8	1.4	2.8	1.4	2.8	1.4	2.8	mA		
$V_{O1}/V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120			120			dB	

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for  $T_A$  is 0°C to 70°C for TL08\_C, TL08\_AC, TL08\_BC and -40°C to 85°C for TL08\_I.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

## Electrical Characteristics

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	$T_A$	TL081M, TL082M			TL084Q, TL084M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C		3	6		3	9	mV
		Full range			9			15	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range		18			18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$ Input offset current <sup>(2)</sup>	$V_O = 0$	25°C		5	100		5	100	pA
		125°C			20			20	nA
$I_{IB}$ Input bias current <sup>(2)</sup>	$V_O = 0$	25°C		30	200		30	200	pA
		125°C			50			50	nA
$V_{ICR}$ Common-mode input voltage range		25°C	$\pm 11$	–12 to 15		$\pm 11$	–12 to 15		V
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		V
	$R_L \geq 10\ \text{k}\Omega$	Full range	$\pm 12$			$\pm 12$			
	$R_L \geq 2\ \text{k}\Omega$		$\pm 10$	$\pm 12$		$\pm 10$	$\pm 12$		
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	25	200		25	200		V/mV
		Full range	15			15			
$B_1$ Unity-gain bandwidth		25°C		3			3		MHz
$r_i$ Input resistance		25°C		$10^{12}$			$10^{12}$		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 15\ \text{V}$ to $\pm 9\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$I_{CC}$ Supply current (each amplifier)	$V_O = 0, \text{No load}$	25°C		1.4	2.8		1.4	2.8	mA
$V_{O1}/V_{O2}$ Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.  
 (2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

## Operating Characteristics

 $V_{CC\pm} = \pm 15\ \text{V}, T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}$ , See <a href="#">Figure 1</a>	8 <sup>(1)</sup>	13		V/ $\mu\text{s}$
	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , See <a href="#">Figure 1</a>	5 <sup>(1)</sup>			
$t_r$ Rise-time	$V_I = 20\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}$ , See <a href="#">Figure 1</a>		0.05		$\mu\text{s}$
overshoot factor			20		%
$V_n$ Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\ \text{kHz}$		18	$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\ \text{Hz}$ to $10\ \text{kHz}$		4	$\mu\text{V}$
$I_n$ Equivalent input noise current	$R_S = 20\ \Omega, f = 1\ \text{kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{I\text{rms}} = 6\ \text{V}, A_{VD} = 1, R_S \leq 1\ \text{k}\Omega, R_L \geq 2\ \text{k}\Omega, f = 1\ \text{kHz}$		0.003		%

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Parameter Measurement Information

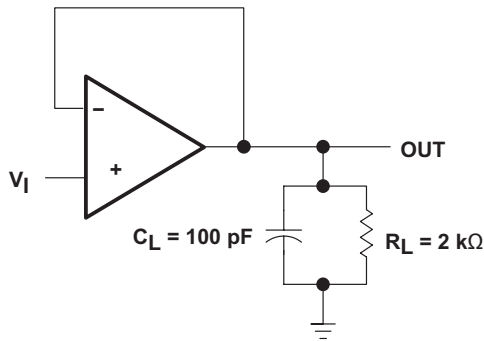


Figure 1.

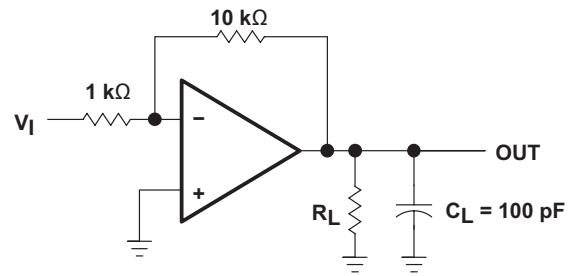


Figure 2.

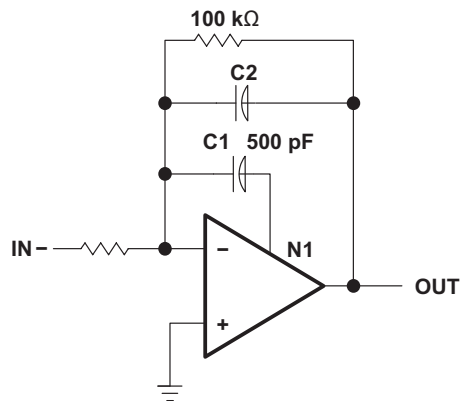


Figure 3.

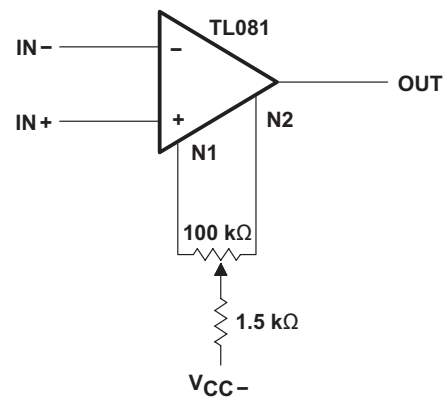


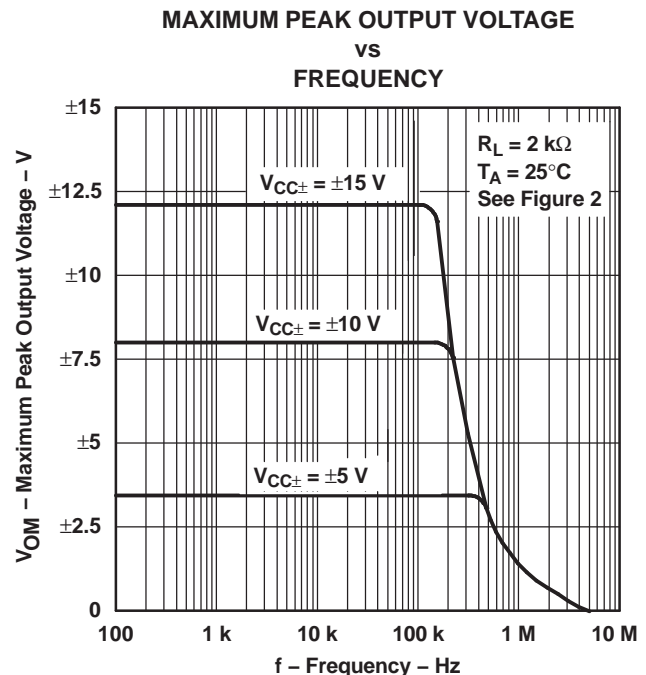
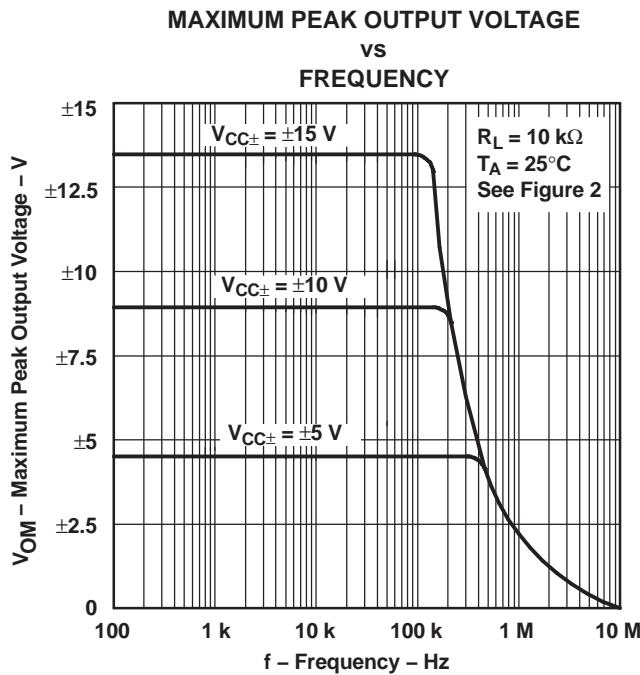
Figure 4.

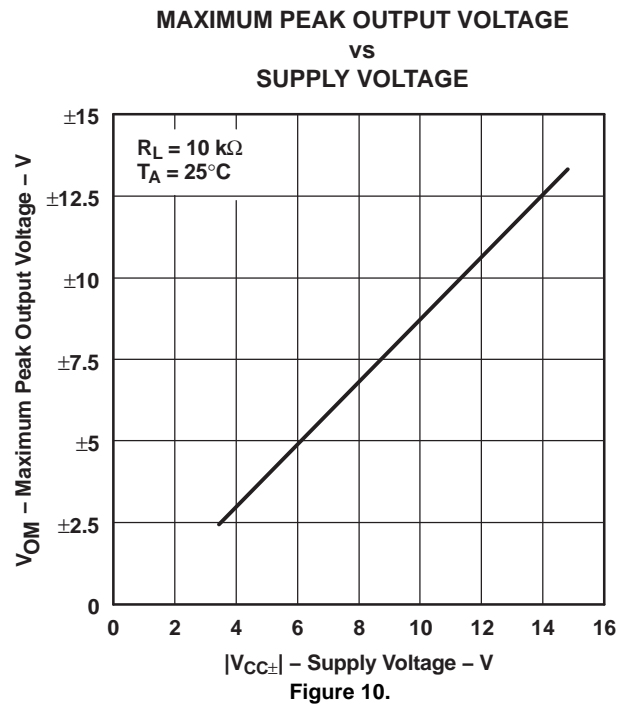
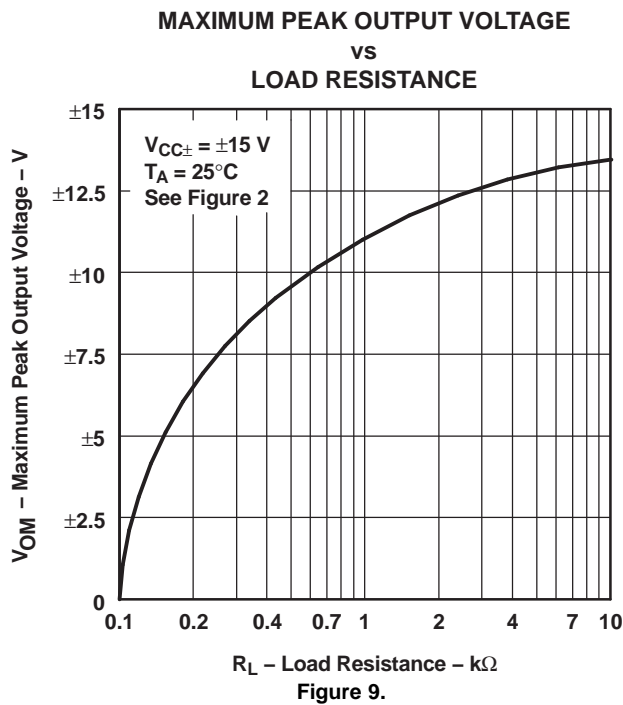
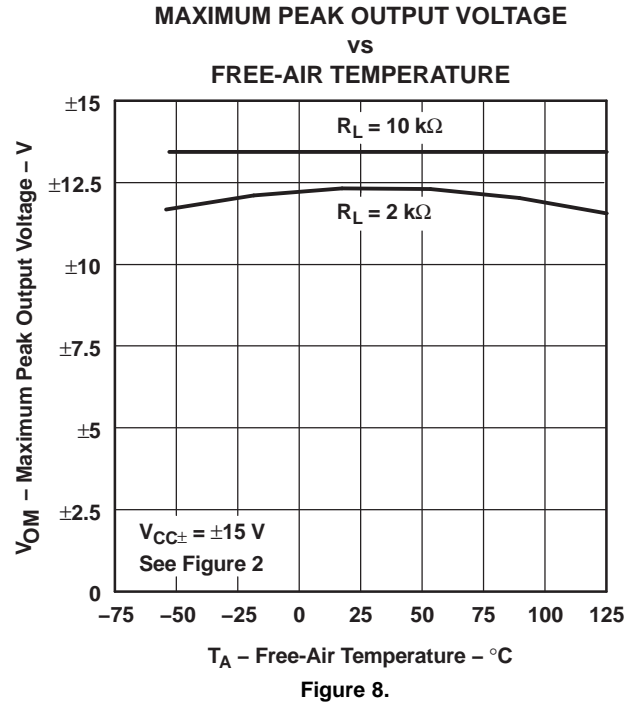
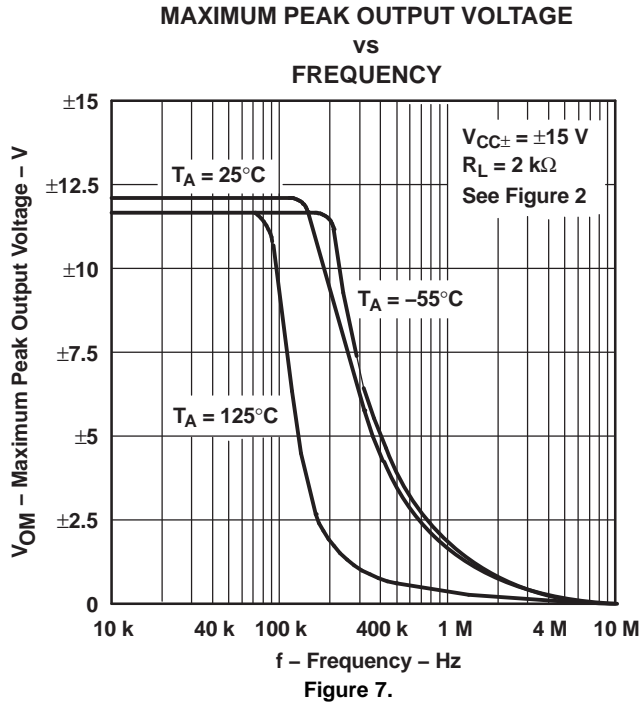
### Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

#### Table of Graphs

			Figure
$V_{OM}$	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	Figure 5, Figure 6, Figure 7 Figure 8 Figure 9 Figure 10
$A_{VD}$	Large-signal differential voltage amplification	vs Free-air temperature vs Load resistance	Figure 11 Figure 12
	Differential voltage amplification	vs Frequency with feed-forward compensation	Figure 13
$P_D$	Total power dissipation	vs Free-air temperature	Figure 14
$I_{CC}$	Supply current	vs Free-air temperature	Figure 15
		vs Supply voltage	Figure 16
$I_{IB}$	Input bias current	vs Free-air temperature	Figure 17
		Large-signal pulse response	vs Time
$V_O$	Output voltage	vs Elapsed time	Figure 19
CMRR	Common-mode rejection ratio	vs Free-air temperature	Figure 20
$V_n$	Equivalent input noise voltage	vs Frequency	Figure 21
THD	Total harmonic distortion	vs Frequency	Figure 22







LARGE-SIGNAL  
DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
FREE-AIR TEMPERATURE

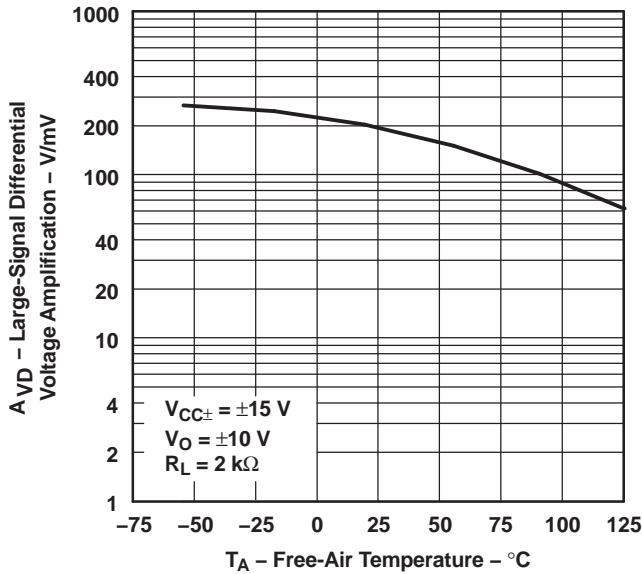


Figure 11.

LARGE-SIGNAL  
DIFFERENTIAL VOLTAGE AMPLIFICATION  
AND PHASE SHIFT  
vs  
FREQUENCY

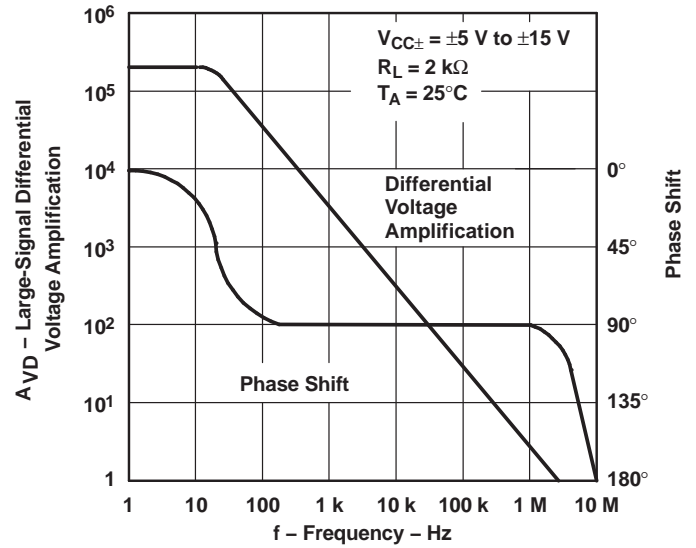


Figure 12.

DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
FREQUENCY WITH FEED-FORWARD COMPENSATION

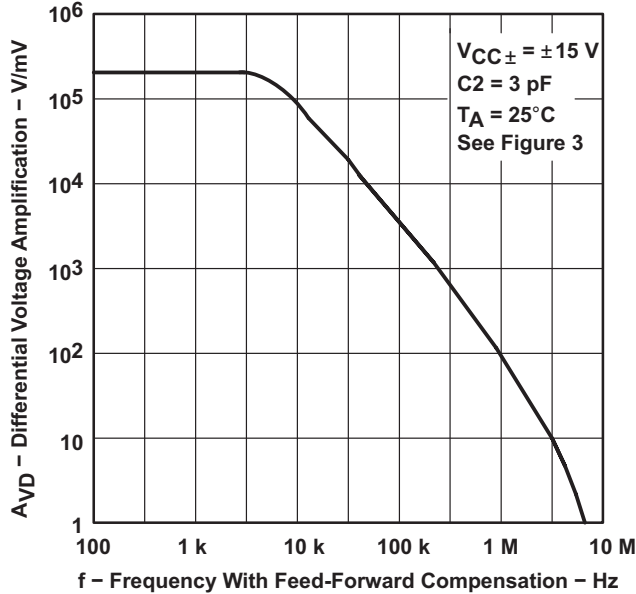


Figure 13.

TOTAL POWER DISSIPATION  
vs  
FREE-AIR TEMPERATURE

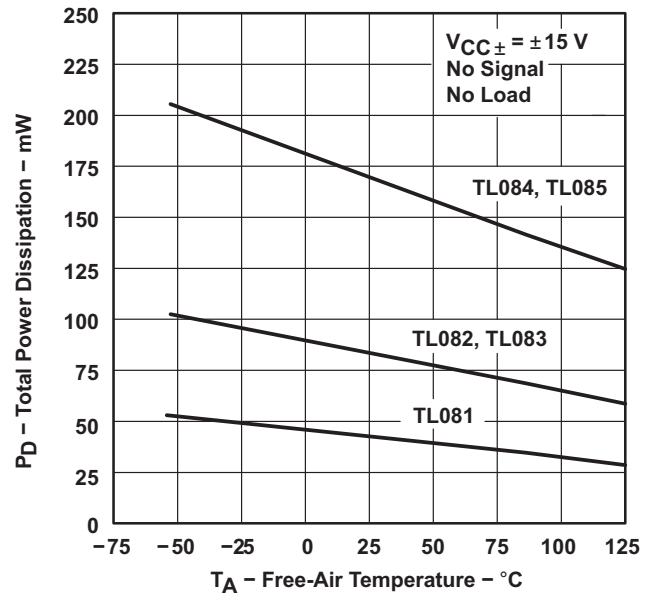


Figure 14.

SUPPLY CURRENT PER AMPLIFIER  
 vs  
 FREE-AIR TEMPERATURE

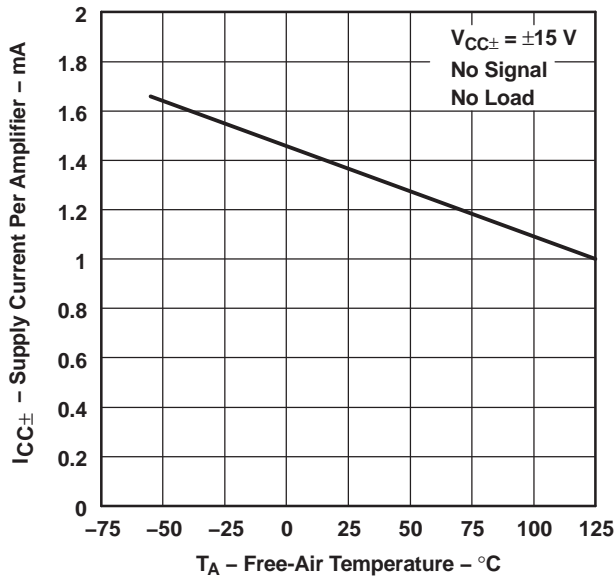


Figure 15.

SUPPLY CURRENT PER AMPLIFIER  
 vs  
 SUPPLY VOLTAGE

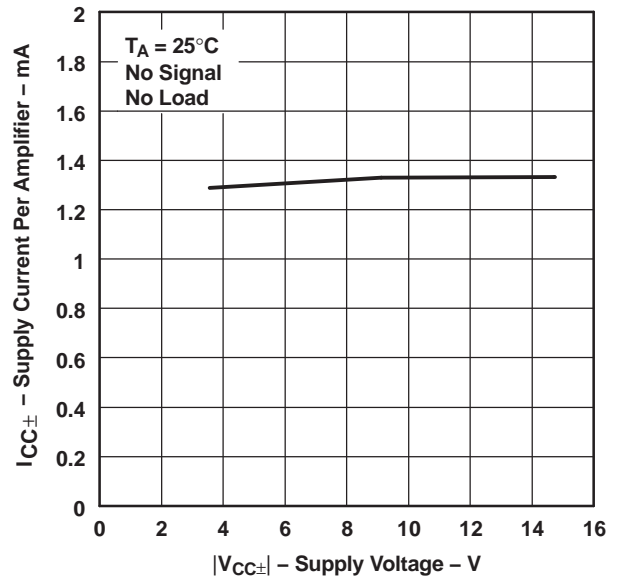


Figure 16.

INPUT BIAS CURRENT  
 vs  
 FREE-AIR TEMPERATURE

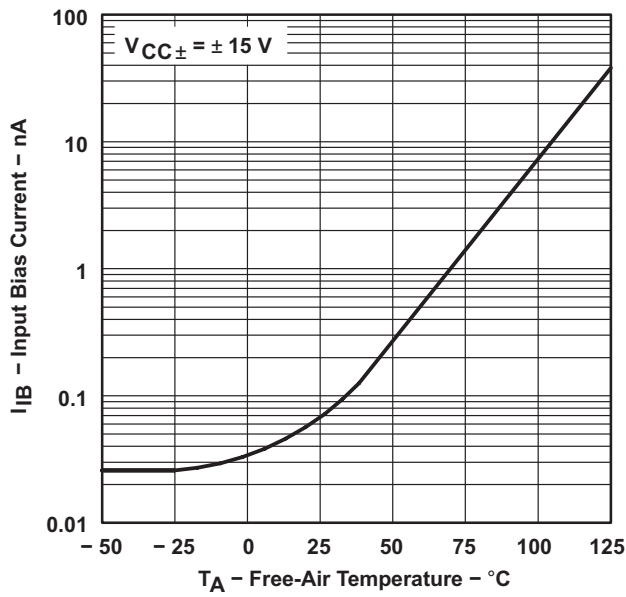


Figure 17.

VOLTAGE-FOLLOWER  
 LARGE-SIGNAL PULSE RESPONSE

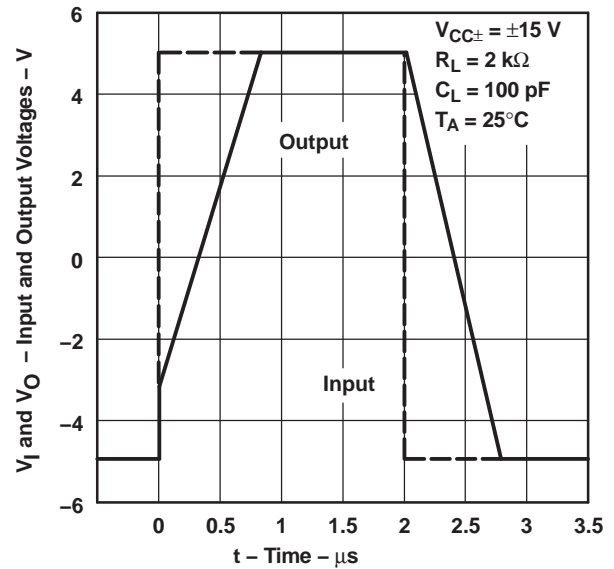
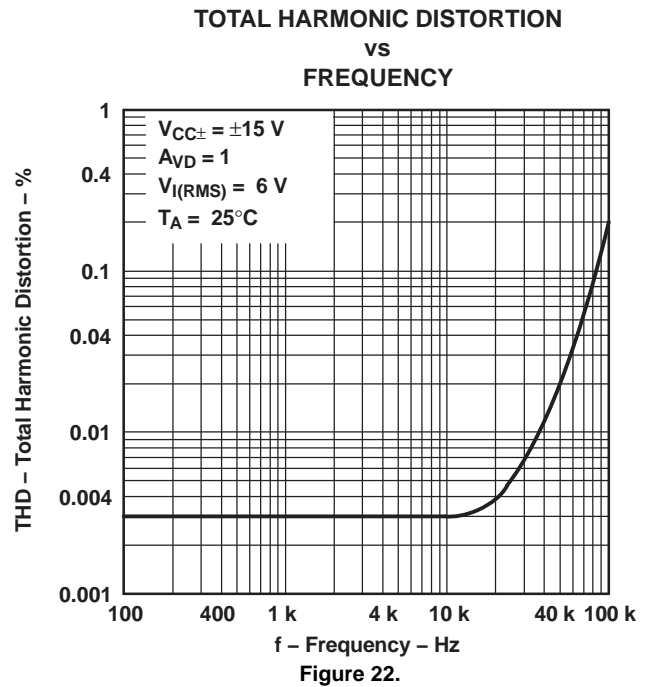
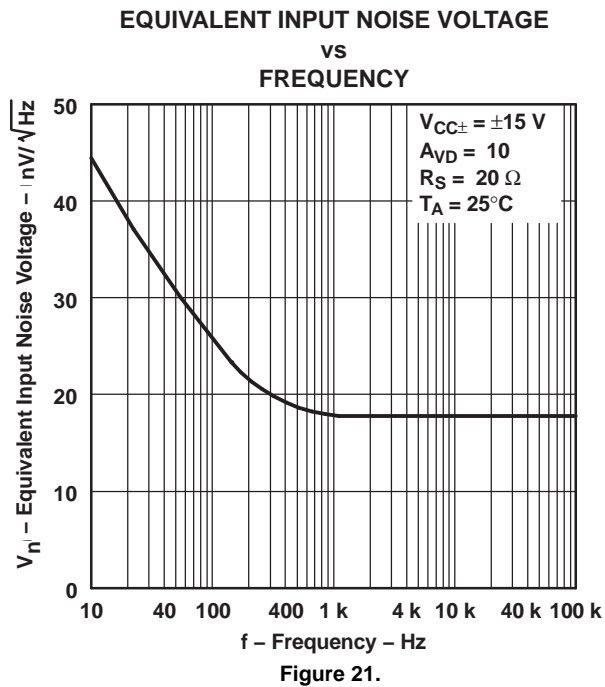
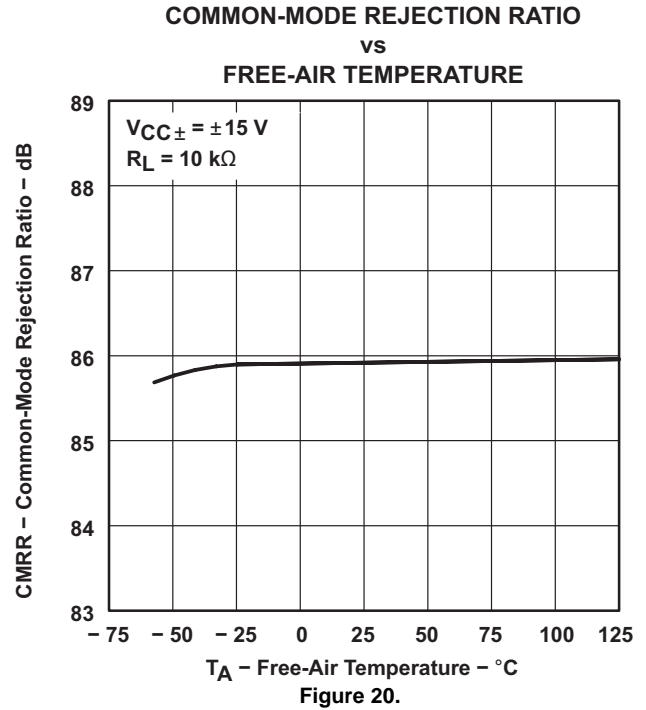
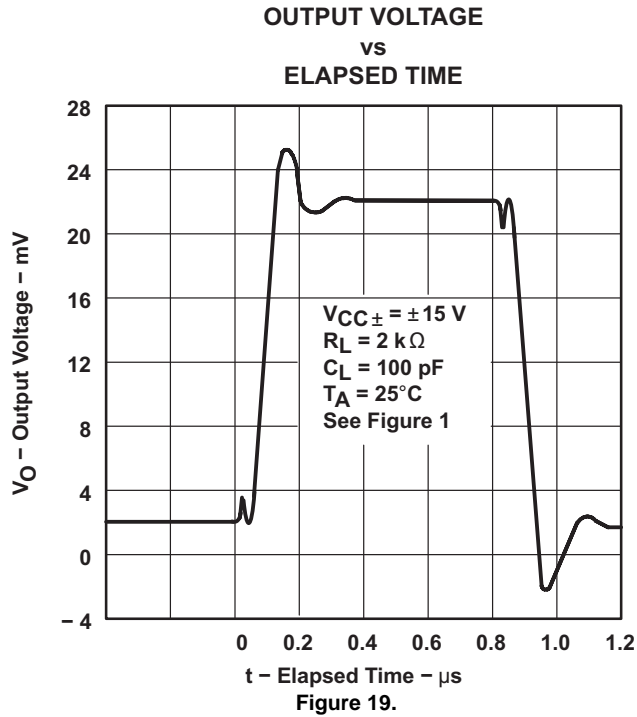


Figure 18.



APPLICATION INFORMATION

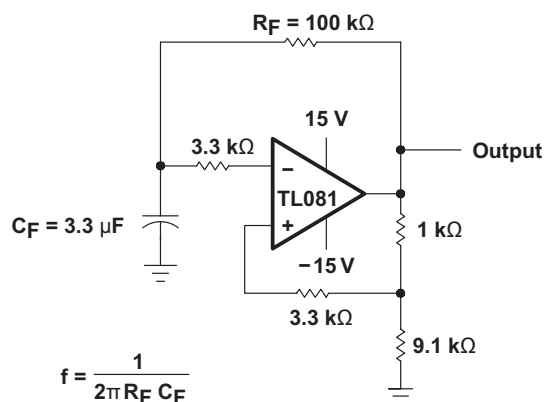


Figure 23.

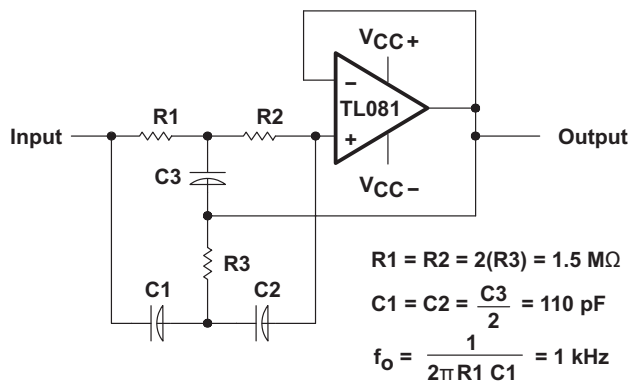


Figure 24.

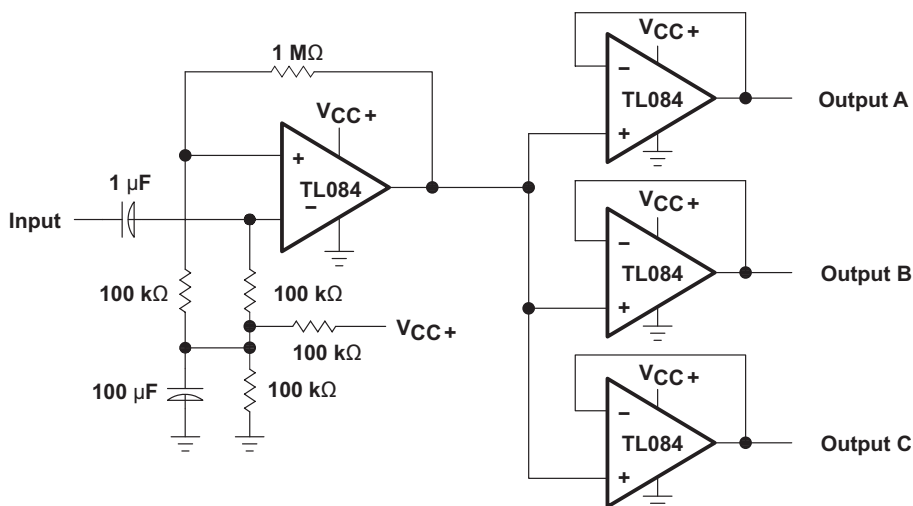
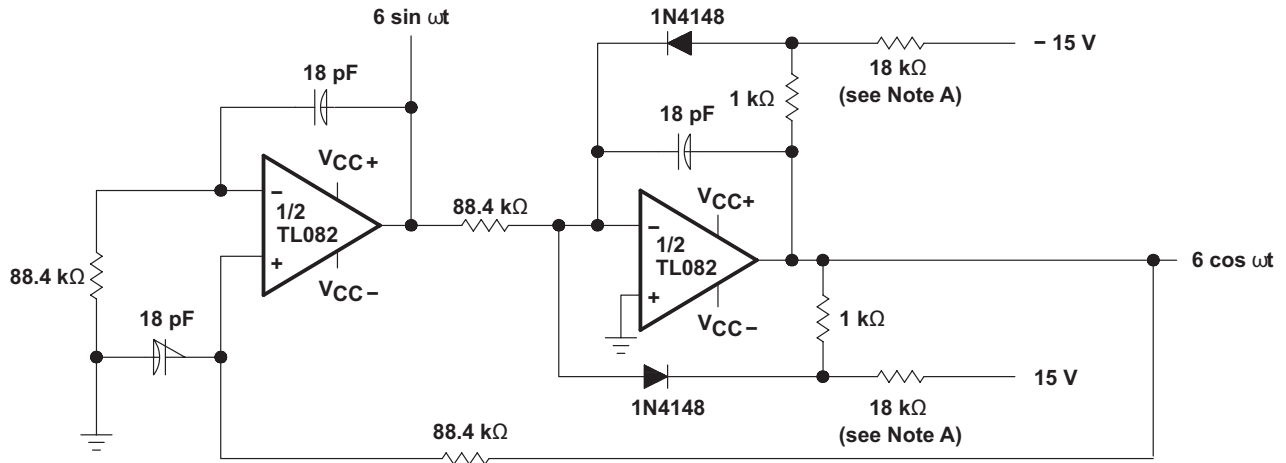


Figure 25. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

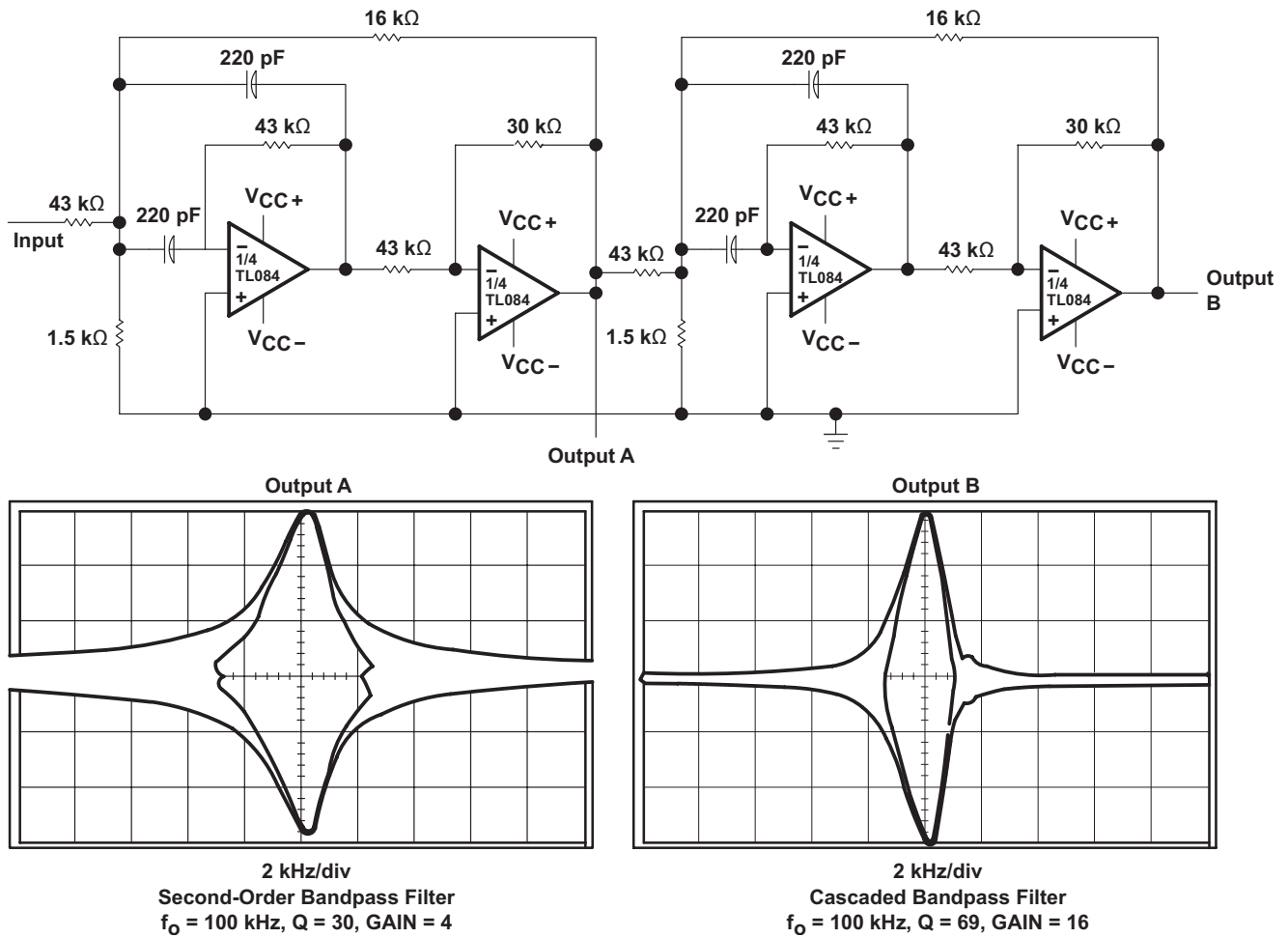


Figure 27. Positive-Feedback Bandpass Filter

## REVISION HISTORY

Changes from Revision G (September 2004) to Revision H	Page
• Updated document to new TI datasheet format - no specification changes. ....	1
• Added ESD warning. ....	2

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	<a href="#">Samples</a>
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	<a href="#">Samples</a>
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	<a href="#">Samples</a>
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	<a href="#">Samples</a>
TL081ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	<a href="#">Samples</a>
TL081ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	<a href="#">Samples</a>
TL081ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL081ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	<a href="#">Samples</a>
TL081ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	<a href="#">Samples</a>
TL081BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	<a href="#">Samples</a>
TL081BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	<a href="#">Samples</a>
TL081BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	<a href="#">Samples</a>
TL081BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	<a href="#">Samples</a>
TL081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	<a href="#">Samples</a>
TL081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	<a href="#">Samples</a>
TL081CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	<a href="#">Samples</a>
TL081CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	<a href="#">Samples</a>
TL081CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	<a href="#">Samples</a>
TL081IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	<a href="#">Samples</a>
TL081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	<a href="#">Samples</a>
TL081IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	<a href="#">Samples</a>
TL081IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	<a href="#">Samples</a>
TL081IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	<a href="#">Samples</a>
TL081MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL081MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL081MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL082ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	<a href="#">Samples</a>
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	<a href="#">Samples</a>
TL082ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	<a href="#">Samples</a>
TL082BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	<a href="#">Samples</a>
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	<a href="#">Samples</a>
TL082BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	<a href="#">Samples</a>
TL082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	<a href="#">Samples</a>
TL082CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL082CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	<a href="#">Samples</a>
TL082CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	<a href="#">Samples</a>
TL082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	<a href="#">Samples</a>
TL082IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	<a href="#">Samples</a>
TL082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	<a href="#">Samples</a>
TL082IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	<a href="#">Samples</a>
TL082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	<a href="#">Samples</a>
TL082IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
TL082IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	<a href="#">Samples</a>
TL082IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	<a href="#">Samples</a>
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	<a href="#">Samples</a>
TL082IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	<a href="#">Samples</a>
TL082MFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	<a href="#">Samples</a>
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL082MJG	<a href="#">Samples</a>
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	<a href="#">Samples</a>
TL084ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	<a href="#">Samples</a>
TL084ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	<a href="#">Samples</a>
TL084ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	<a href="#">Samples</a>
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	<a href="#">Samples</a>
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	<a href="#">Samples</a>
TL084ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	<a href="#">Samples</a>
TL084ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	<a href="#">Samples</a>
TL084ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	<a href="#">Samples</a>
TL084BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	<a href="#">Samples</a>
TL084BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	<a href="#">Samples</a>
TL084BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	<a href="#">Samples</a>
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	<a href="#">Samples</a>
TL084BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	<a href="#">Samples</a>
TL084BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	<a href="#">Samples</a>
TL084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>
TL084CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>
TL084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>
TL084CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>
TL084CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	<a href="#">Samples</a>
TL084CJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
TL084CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	<a href="#">Samples</a>
TL084CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	<a href="#">Samples</a>
TL084CNSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI	0 to 70		
TL084CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	<a href="#">Samples</a>
TL084CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	<a href="#">Samples</a>
TL084CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	<a href="#">Samples</a>
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	<a href="#">Samples</a>
TL084CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	<a href="#">Samples</a>
TL084CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70		
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	<a href="#">Samples</a>
TL084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>
TL084IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>
TL084IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>
TL084IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>
TL084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	<a href="#">Samples</a>
TL084IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-40 to 85		
TL084IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	<a href="#">Samples</a>
TL084INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	<a href="#">Samples</a>
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL084MFK	<a href="#">Samples</a>
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	<a href="#">Samples</a>
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL084MJ	<a href="#">Samples</a>
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	<a href="#">Samples</a>
TL084QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	<a href="#">Samples</a>
TL084QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	<a href="#">Samples</a>
TL084QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	<a href="#">Samples</a>
TL084QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :**

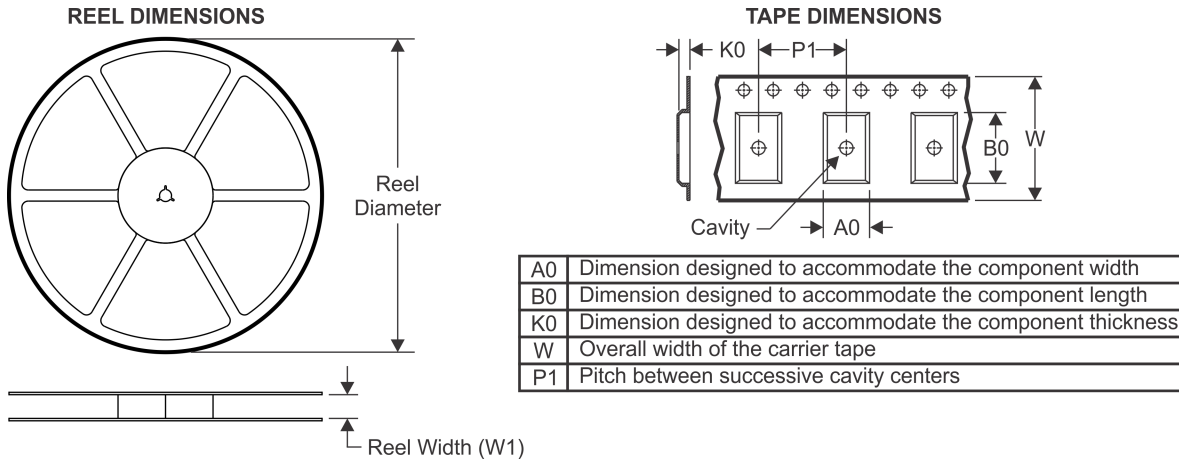
- Catalog: [TL082](#), [TL084](#)
- Automotive: [TL082-Q1](#), [TL082-Q1](#)
- Military: [TL082M](#), [TL084M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

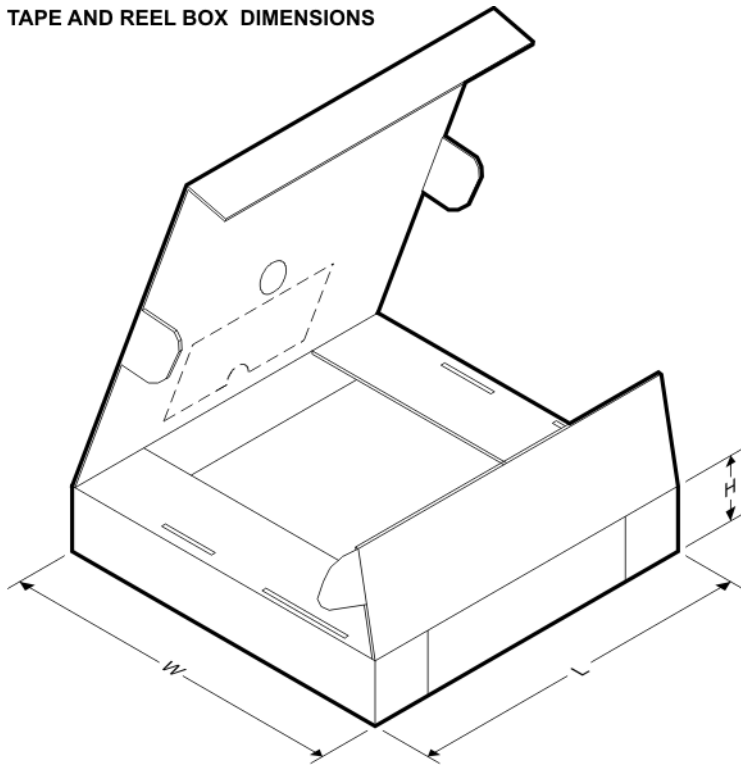


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


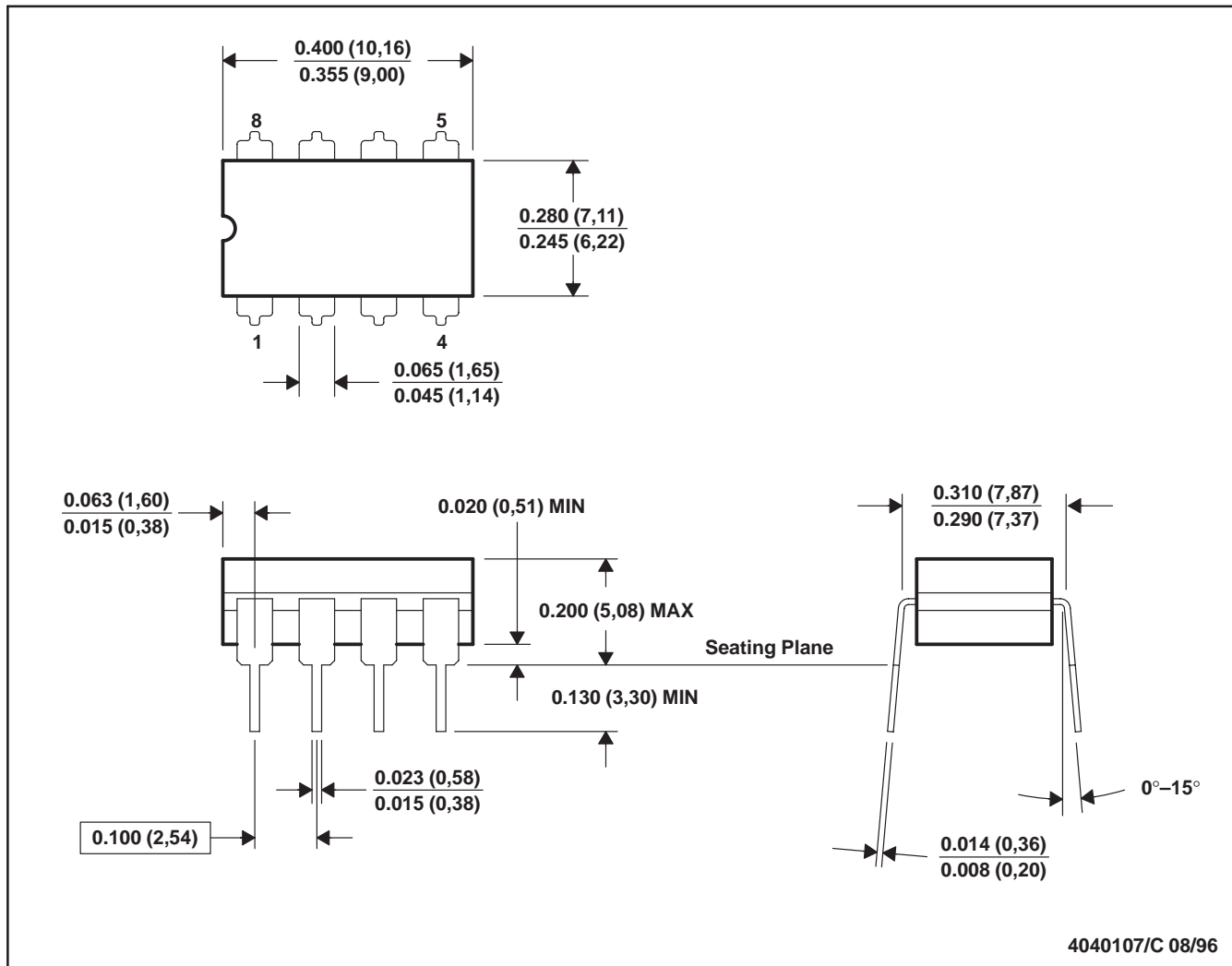
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL082IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL084CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084QDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084QDRG4	SOIC	D	14	2500	367.0	367.0	38.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

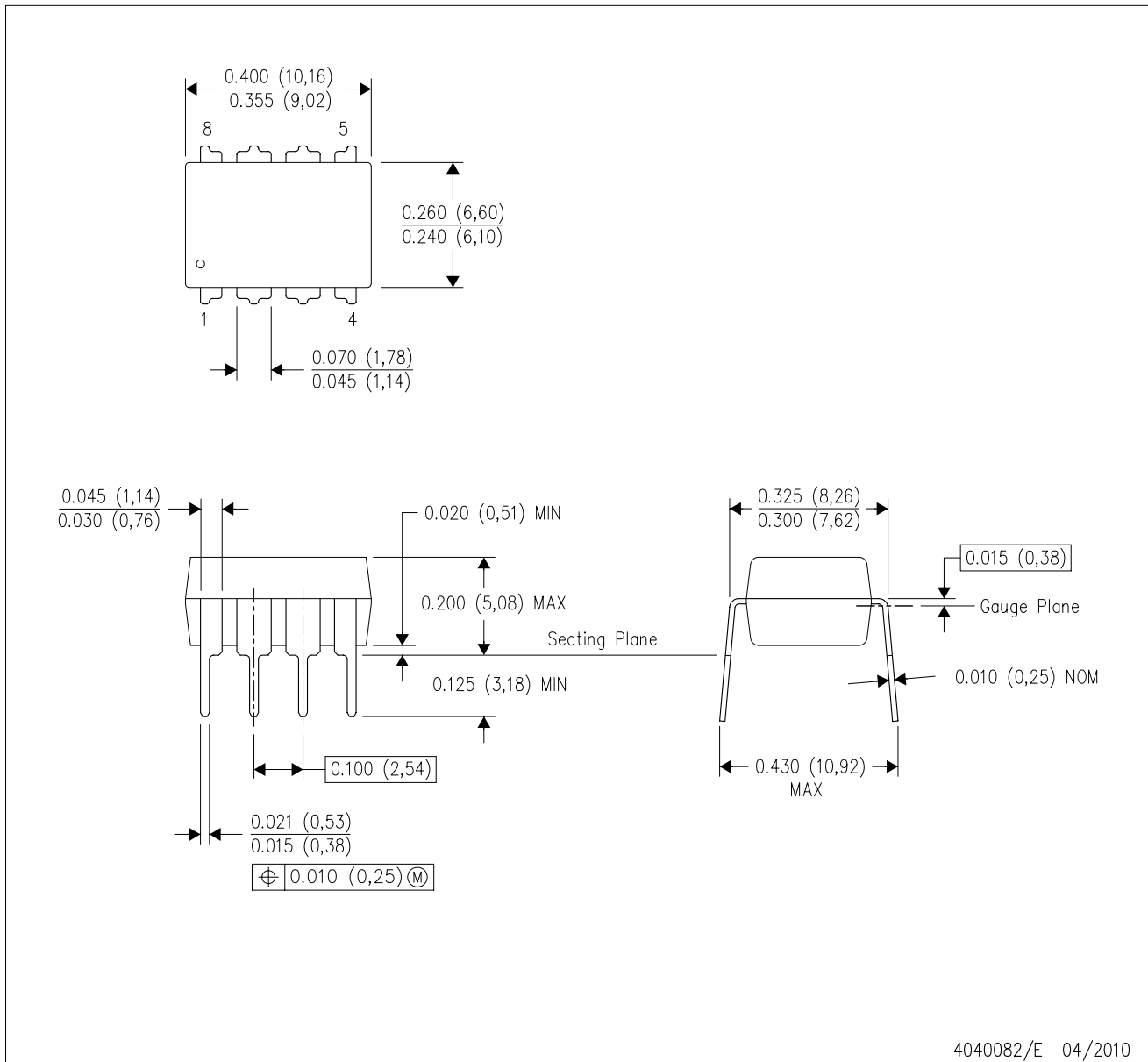


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

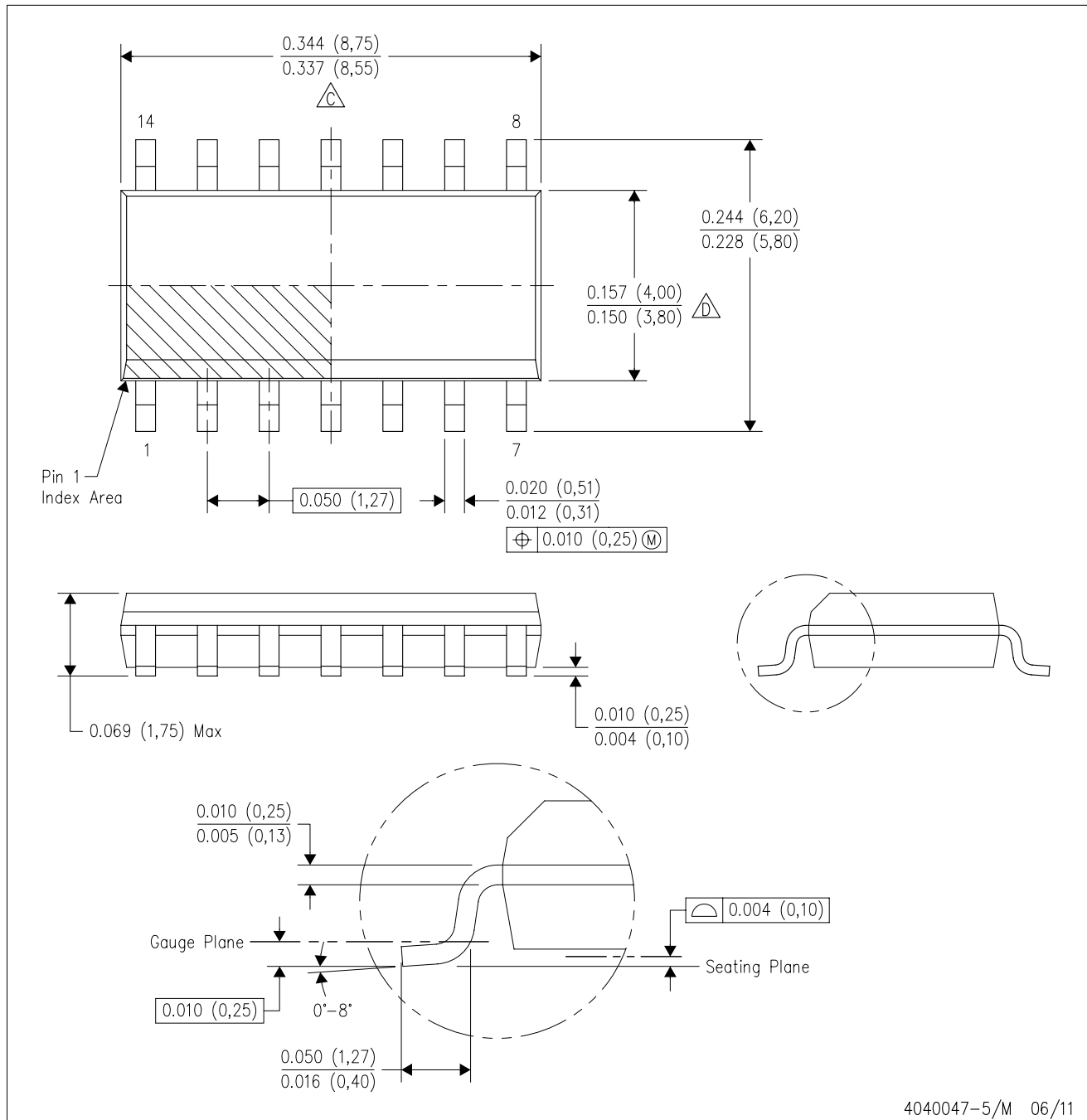


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

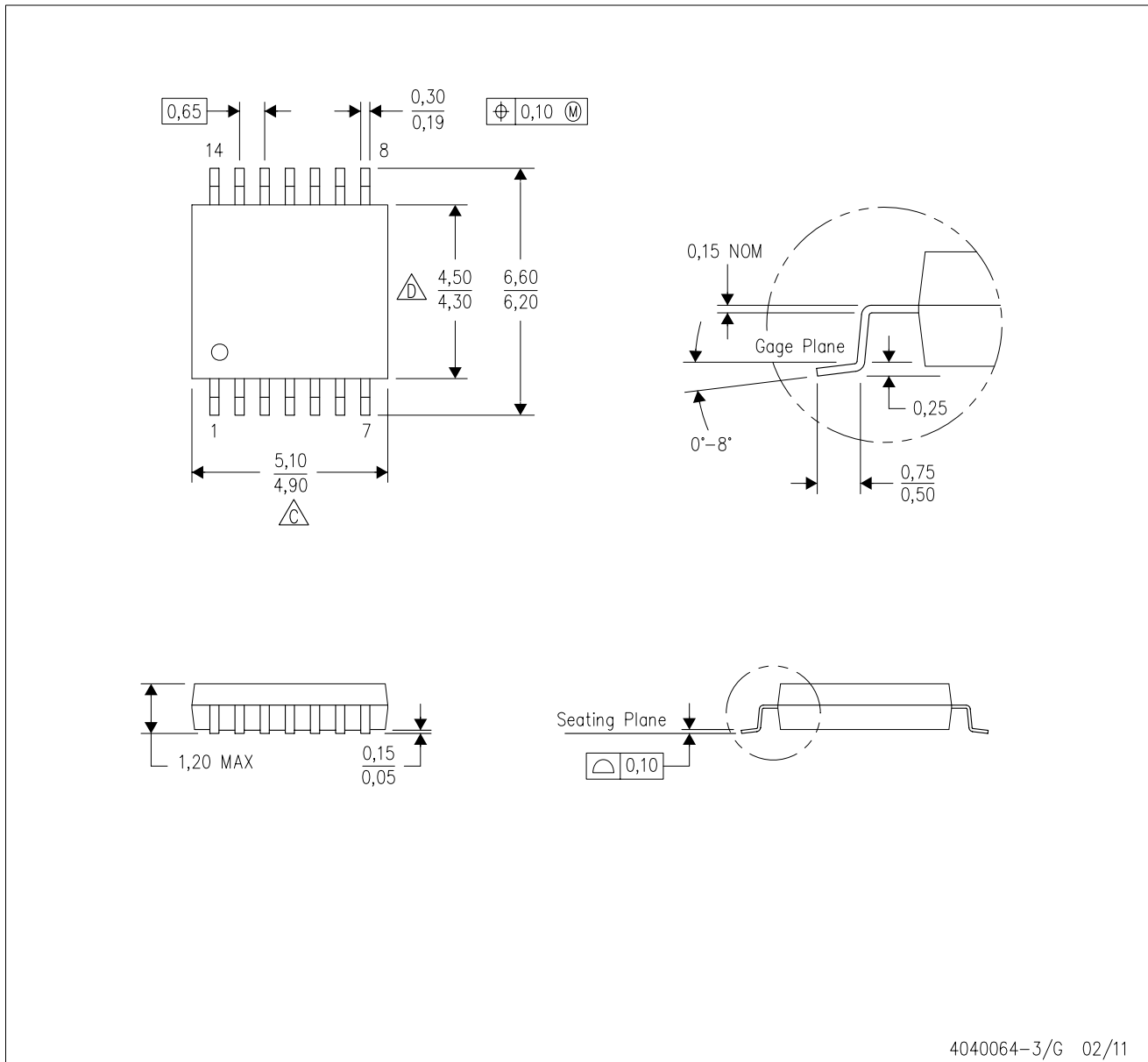
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

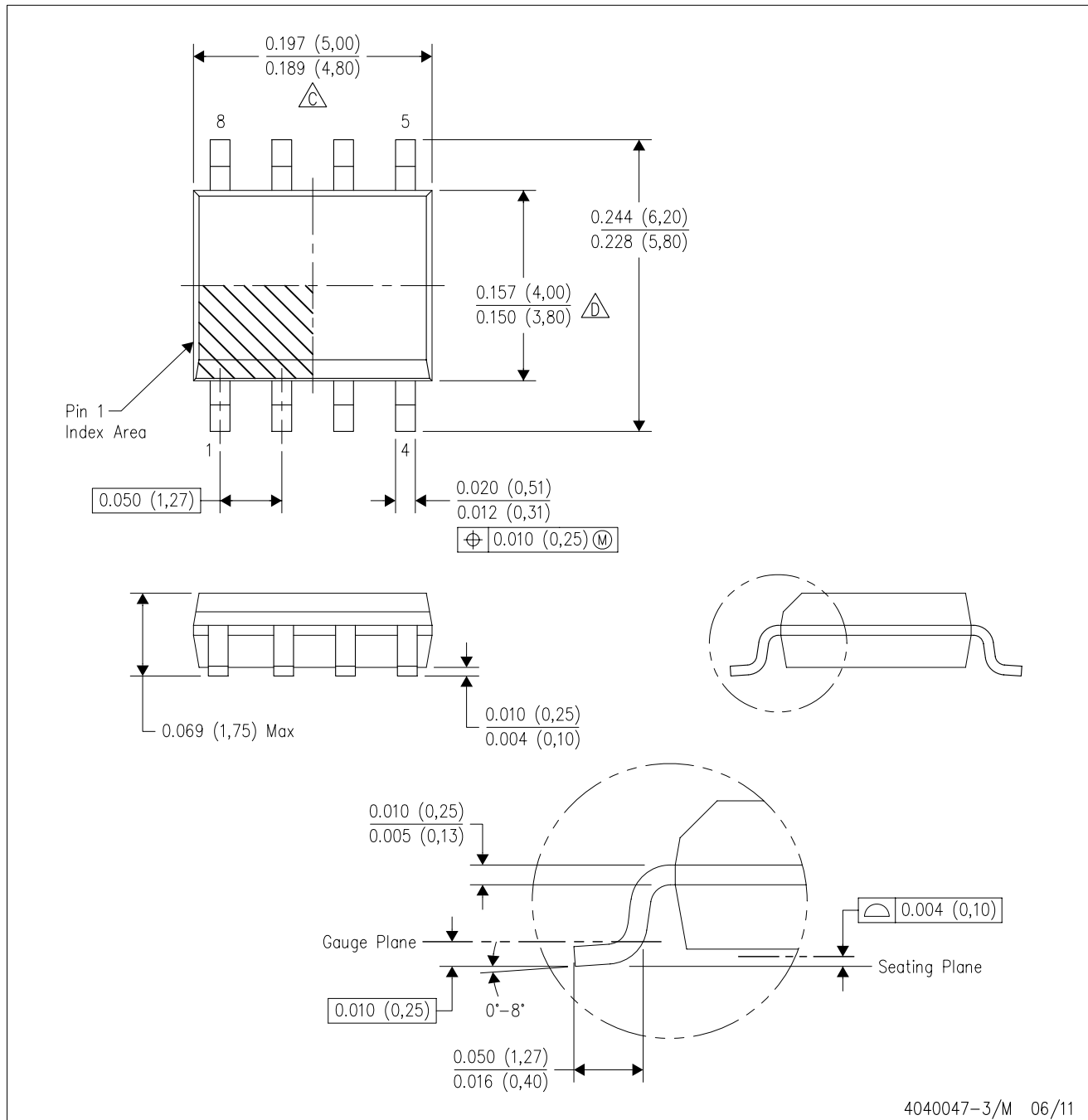
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

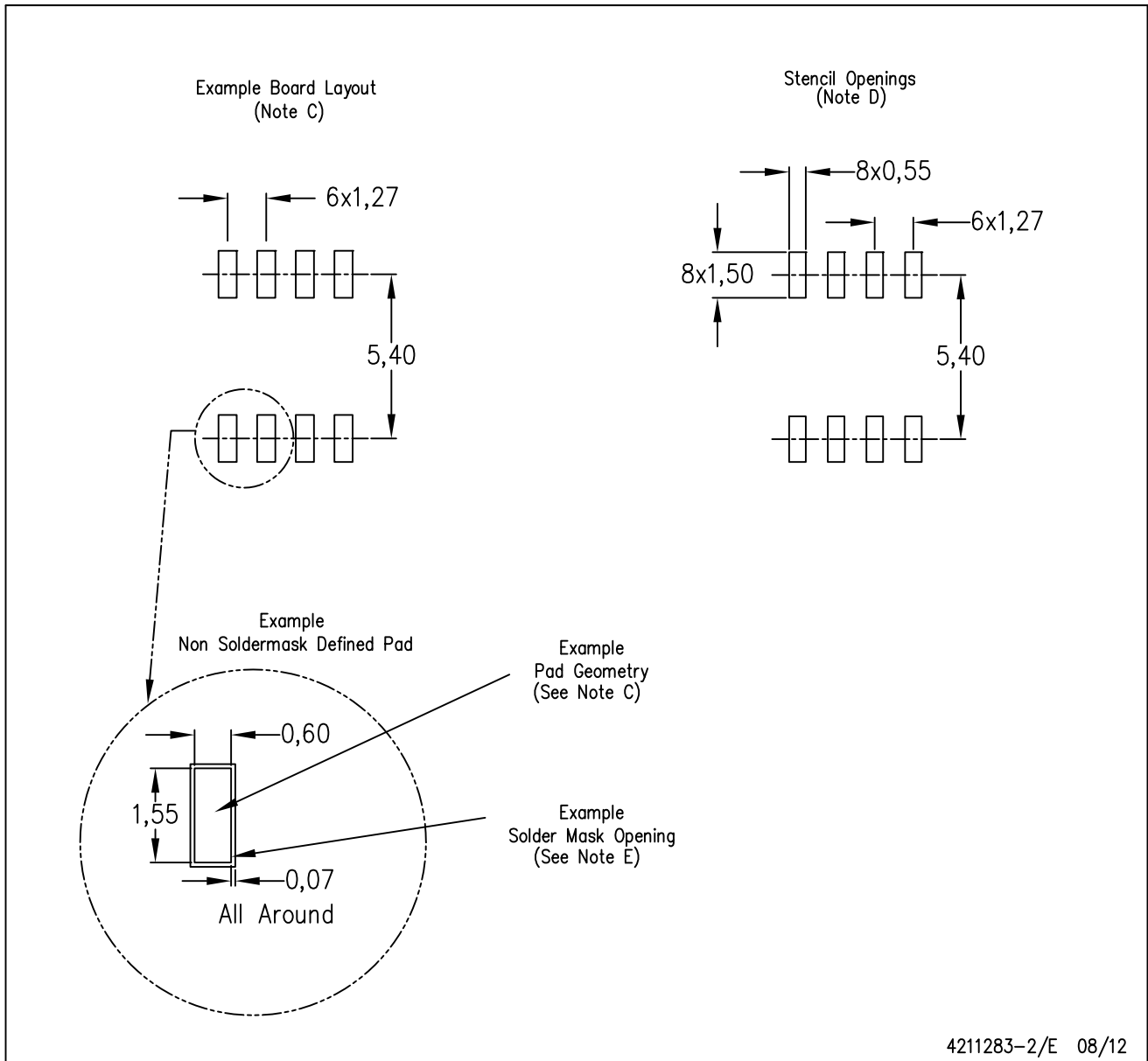
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

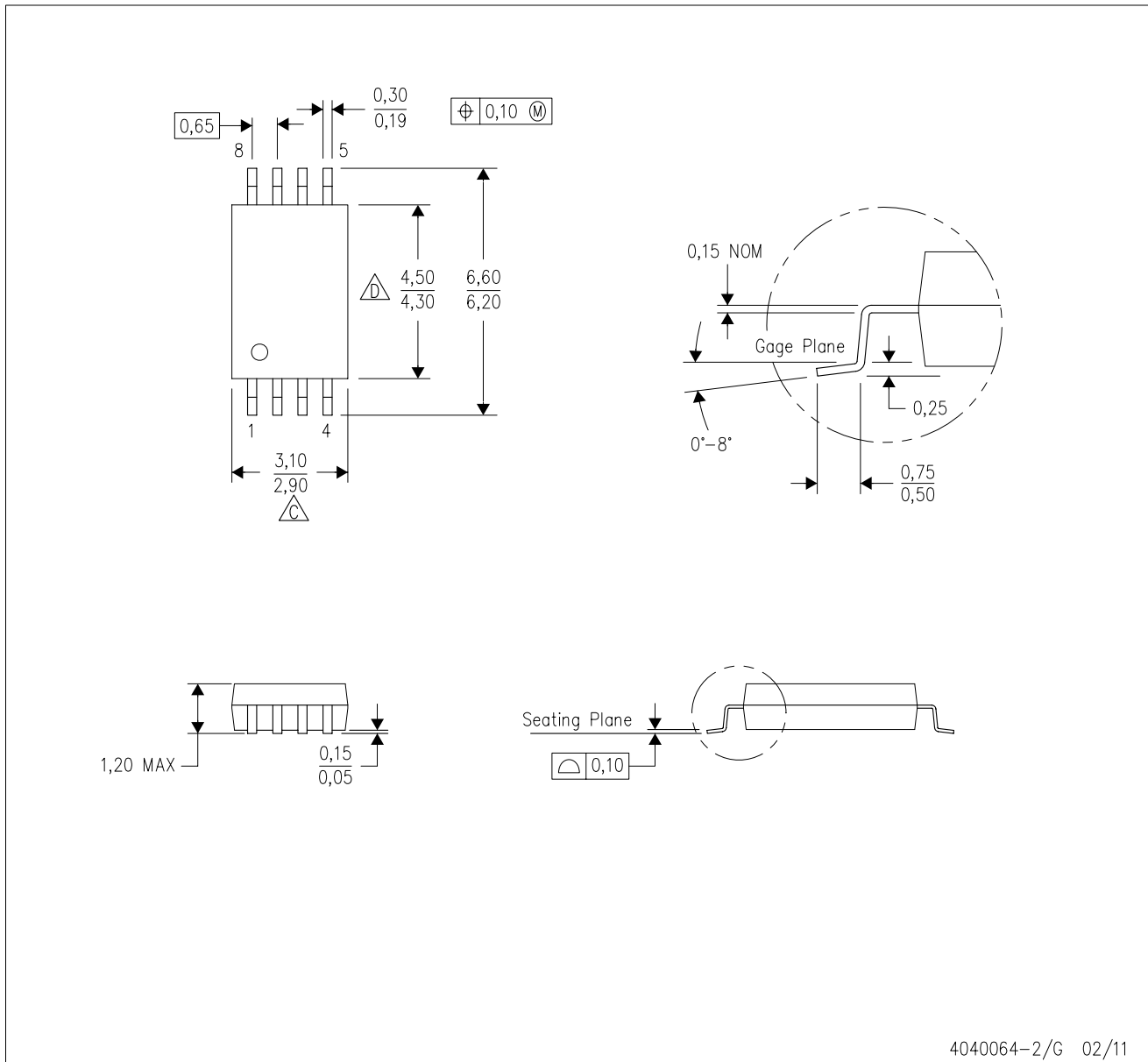


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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