

CD40102B, CD40103B Types

CMOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (20-Volt Rating)

CD40102B – 2-Decade BCD Type
CD40103B – 8-Bit Binary Type

■ CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102B is configured as two cascaded 4-bit BCD counters, and the CD40103B contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE (CI/CE) input is high. The CARRY-OUT/ZERO-DETECT (CO/ZD) output goes low when the count reaches zero if the CI/CE input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the CI/CE input. When the ASYNCHRONOUS PRESET-ENABLE (APE) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the SPE, CI/CE, or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102B and a single 8-bit binary word for the CD40103B. When the CLEAR (CLR) input is low, the counter is asynchronously cleared to its maximum count (99₁₀ for the CD40102B and 255₁₀ for the CD40103B) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except CI/CE are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

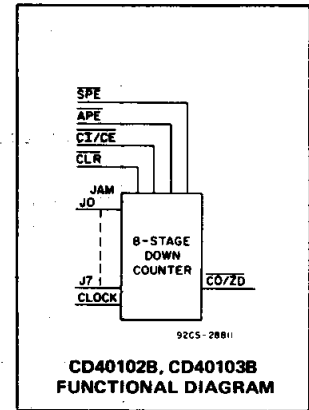
This causes the CO/ZD output to go low to enable the clock on each succeeding clock pulse.

The CD40102B and CD40103B may be cascaded using the CI/CE input and the CO/ZD output, in either a synchronous or ripple mode as shown in Figs.21 and 22.

The CD40102B and CD40103B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD40103B types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).

Features:

- Synchronous or asynchronous preset
- Medium-speed operation: $f_{CL} = 3.6 \text{ MHz (typ.) @ } V_{DD} = 10 \text{ V}$
- Cascadable
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD} = 5 \text{ V}$
2 V at $V_{DD} = 10 \text{ V}$
2.5 V at $V_{DD} = 15 \text{ V}$
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications:

- Divide-by-"N" counters
- Programmable timers
- Interrupt timers
- Cycle/program counter

RECOMMENDED OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$, Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	LIMITS		Units
		Min.	Max.	
Supply Voltage Range (At $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Clock Pulse Width, t_{w}	5	300	—	ns
	10	180	—	
	15	80	—	
Clear Pulse Width, t_{w}	5	320	—	ns
	10	160	—	
	15	100	—	
APE Pulse Width, t_{w}	5	360	—	ns
	10	160	—	
	15	120	—	
Clock Input Frequency, f_{CL}	5	—	0.7	MHz
	10	—	1.8	
	15	—	2.4	
Clock Rise and Fall Time, t_{rCL} , t_{fCL}	5	—	—	μs
	10	—	15	
	15	—	—	
SPE Setup Time, t_{SU}	5	280	—	ns
	10	140	—	
	15	100	—	
Jam Setup Time, t_{SU}	5	200	—	ns
	10	80	—	
	15	60	—	
CI/CE Setup Time, t_{SU}	5	500	—	ns
	10	250	—	
	15	150	—	

CD40102B, CD40103B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	-0.5V to +20V
Voltages referenced to V _{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1, 9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1, 9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

Note 1: These parameters and limits also apply to the Synchronous Preset Mode should a Preset condition of JAM Zero on J₀ to J₇ exist.

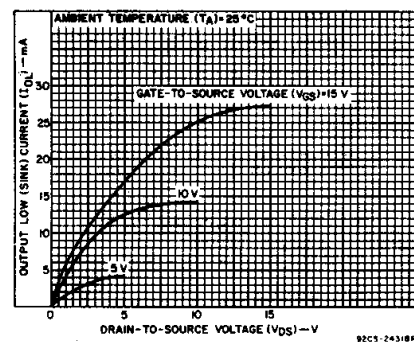


Fig. 1 — Typical output low (sink) current characteristics.

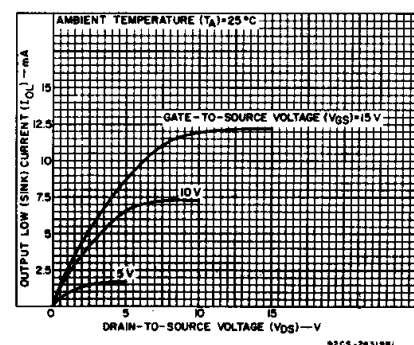


Fig. 2 — Minimum output low (sink) current characteristics.

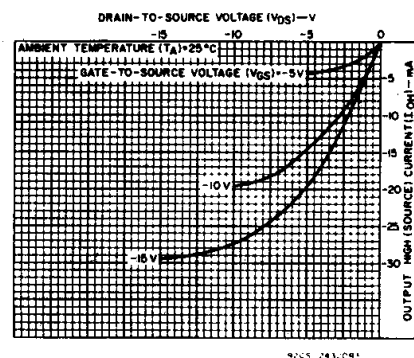


Fig. 3 — Typical output high (source) current characteristics.

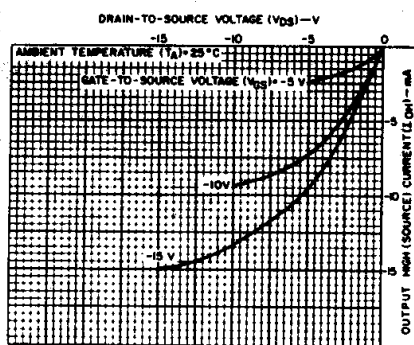


Fig. 4 — Minimum output high (source) current characteristics.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40102B, CD40103B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$,
 Input $t_r, t_f = 20\text{ ns}$, $R_L = 200\text{ k}\Omega$

Characteristic	Conditions VDD (V)	Limits All Packages			Units
		Min.	Typ.	Max.	
Propagation Delay Time (tPHL, tPLH):					
Clock-to-Output (See Fig. 6)	5	—	300	600	ns
Note 1	10	—	130	260	
	15	—	95	190	
Carry In/Counter Enable-to-Output	5	—	200	400	ns
Note 1	10	—	90	180	
	15	—	65	130	
Asynchronous Preset Enable-to-Output	5	—	650	1300	ns
Note 1	10	—	300	600	
	15	—	200	400	
Clear-to-Output	5	—	375	750	ns
Note 1	10	—	180	360	
	15	—	100	200	
Transition Time (tTHL, tTLH)	5	—	100	200	ns
Note 1	10	—	50	100	
	15	—	40	80	
Minimum Clock Pulse Width (tW)	5	—	150	300	ns
Note 1	10	—	90	180	
	15	—	40	80	
Minimum CLR Pulse Width (tW)	5	—	160	320	ns
Note 1	10	—	80	160	
	15	—	50	100	
Minimum APE Pulse Width (tW)	5	—	180	360	ns
Note 1	10	—	80	160	
	15	—	60	120	
Minimum APE Removal Time (tRM)	5	—	110	220	ns
Note 1	10	—	50	100	
	15	—	35	70	
Minimum SPE Set-Up Time (tSU)	5	—	140	280	ns
Note 1	10	—	70	140	
	15	—	50	100	
Minimum CI/CE Setup Time (tSU)	5	—	250	500	ns
Note 1	10	—	125	250	
	15	—	75	150	
Minimum JAM Set-Up Time (tSU) (Synchronous presetting)	5	—	100	200	ns
Note 1	10	—	40	80	
	15	—	30	60	
Maximum Clock Input Frequency (fCL) (See Fig. 7)	5	0.7	1.4	—	MHz
Note 1	10	1.8	3.6	—	
	15	2.4	4.8	—	
Input Capacitance (CIN)			5	7.5	pF

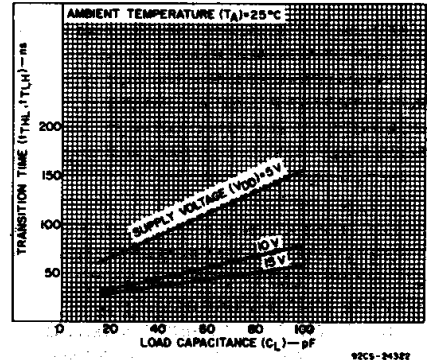


Fig. 5 — Typical transition time as a function of load capacitance.

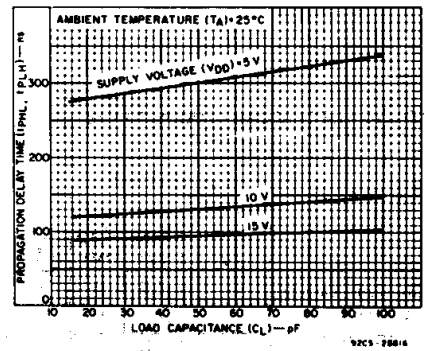


Fig. 6 — Typical propagation delay time as a function of load capacitance (clock to CO/ZD).

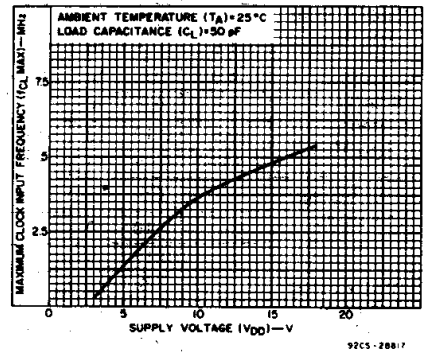


Fig. 7 — Typical maximum clock input frequency as a function of supply voltage.

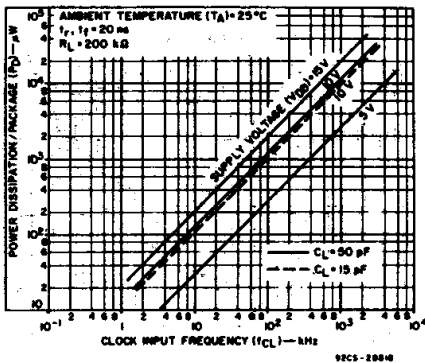


Fig. 8 — Typical dynamic power dissipation as a function of frequency.

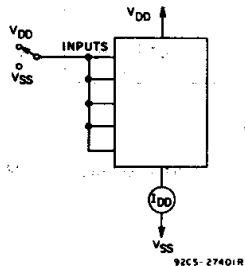


Fig. 9 — Quiescent device current test circuit.

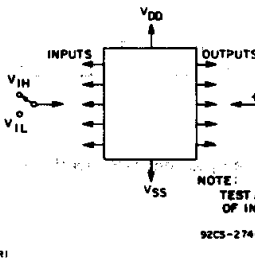


Fig. 10 — Input voltage test circuit.

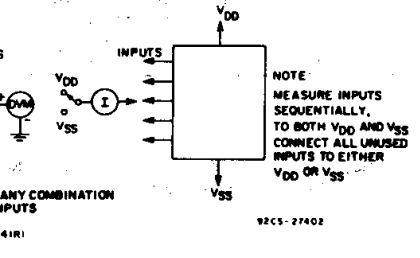


Fig. 11 — Input current test circuit.

CD40102B, CD40103B Types

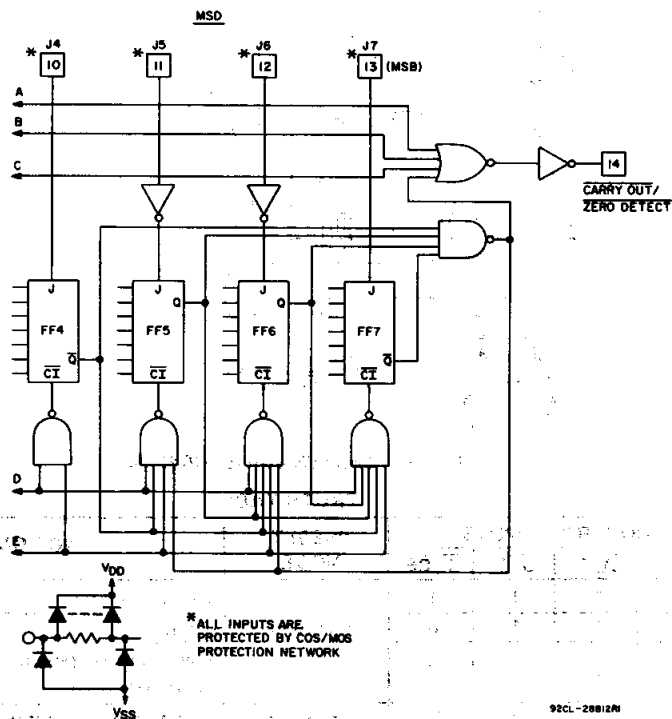
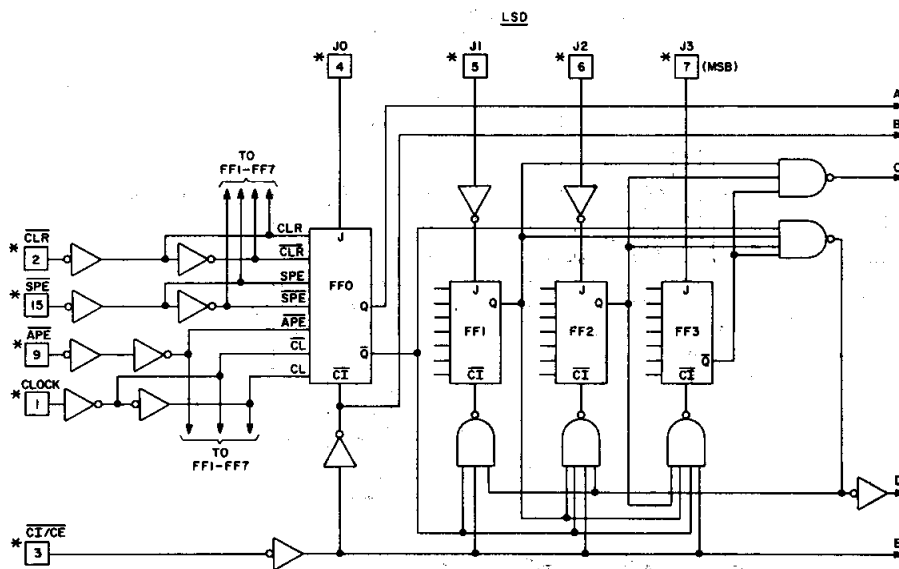


Fig. 12 - Logic diagram for CD40102B.

CD40102B, CD40103B Types

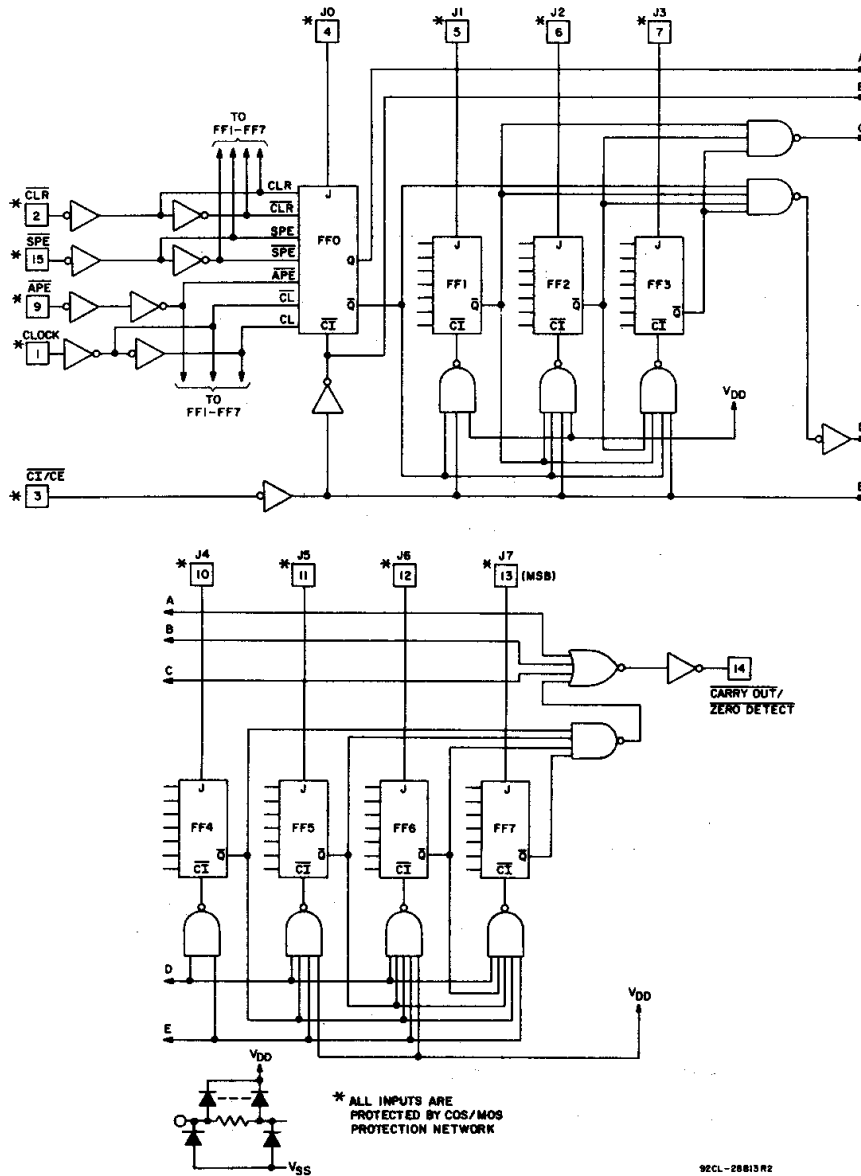


Fig. 13 - Logic diagram for CD40103B.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
CLR	APE	SPE	CI/CE		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down*
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes: 1. 0 = Low level
1 = High level
X = Don't care

- Clock connected to clock input
- Synchronous operation: changes occur on negative-to-positive clock transitions
- JAM inputs: CD40102B BCD; MSD = J7, J6, J5, J4 (J7 is MSB)
LSD = J3, J2, J1, J0 (J3 is MSB)
CD40103B Binary; MSB = J7, LSB = J0

*At zero count, the counters will jump to the maximum count on the next clock transition to "High."

CD40102B, CD40103B Types

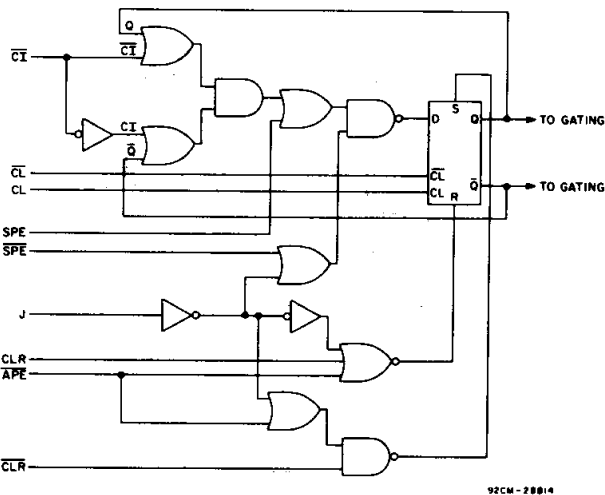


Fig. 14 - Detail logic diagram for flip-flops, FFO - FF7, used in logic diagrams for CD40102B and CD40103B.

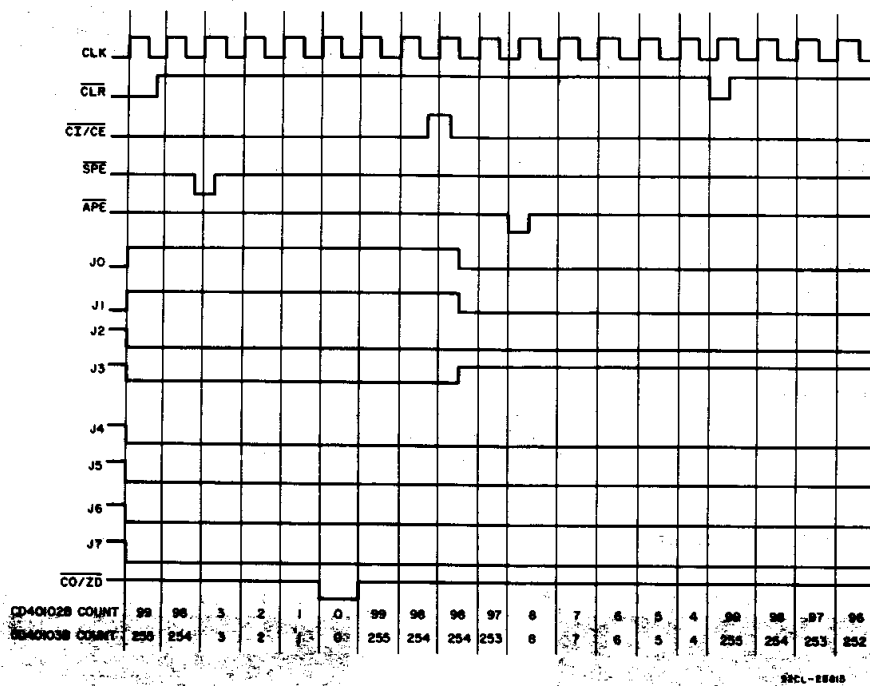
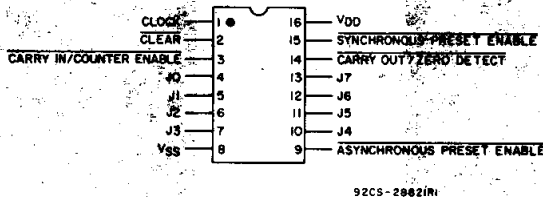


Fig. 15 - Timing diagram for CD40102B and CD40103B.



CD40102B,
CD40103B
TERMINAL ASSIGNMENT

CD40102B, CD40103B Types

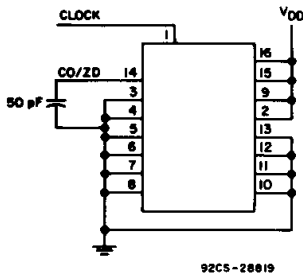


Fig. 16 - Maximum clock frequency test circuit.

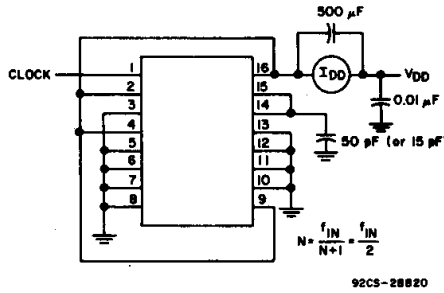


Fig. 17 - Dynamic power dissipation test circuit (÷2 mode).

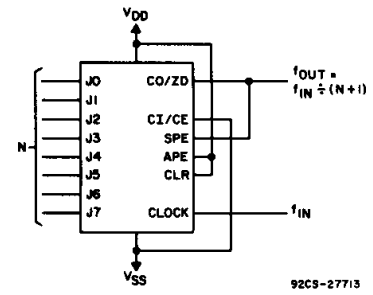


Fig. 18 - Divide-by-"N" counter.

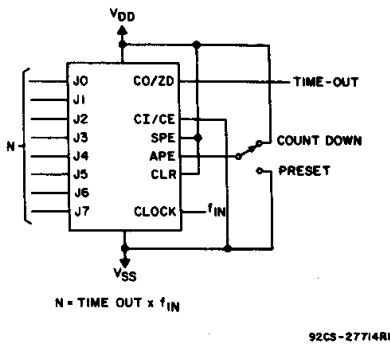


Fig. 19 - Programmable timer.

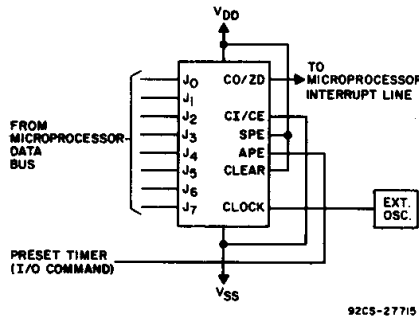
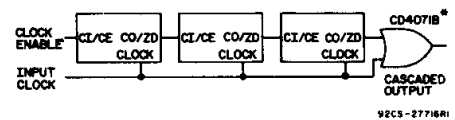


Fig. 20 - Microprocessor interrupt timer.



* An output spike (160 ns @ $V_{DD} = 5V$) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Fig. 21 - Synchronous cascading.

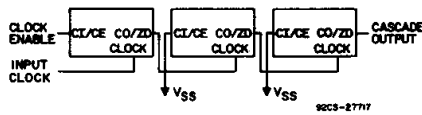
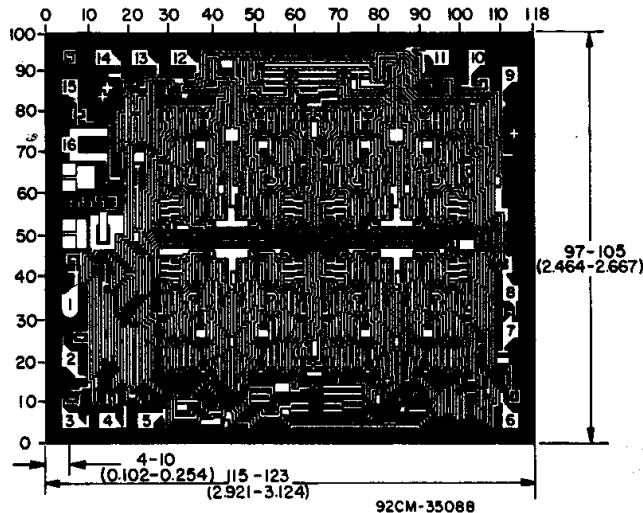


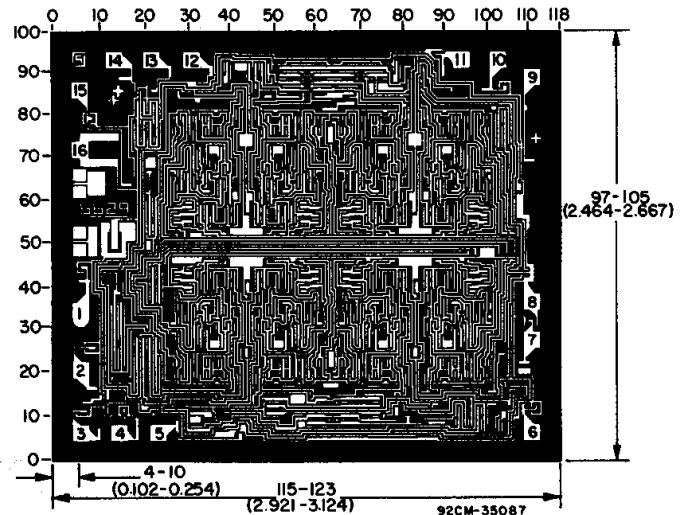
Fig. 22 - Ripple cascading.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD40102B.



Dimensions and pad layout for CD40103B.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40102BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40102BE	Samples
CD40102BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40102BE	Samples
CD40102BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40102B	Samples
CD40102BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0102B	Samples
CD40102BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0102B	Samples
CD40102BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0102B	Samples
CD40103BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40103BE	Samples
CD40103BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40103BE	Samples
CD40103BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40103BF	Samples
CD40103BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40103BF3A	Samples
CD40103BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40103B	Samples
CD40103BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40103B	Samples
CD40103BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0103B	Samples
CD40103BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0103B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40103B, CD40103B-MIL :

- Catalog: [CD40103B](#)
- Military: [CD40103B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40102BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40102BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40102BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD40102BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

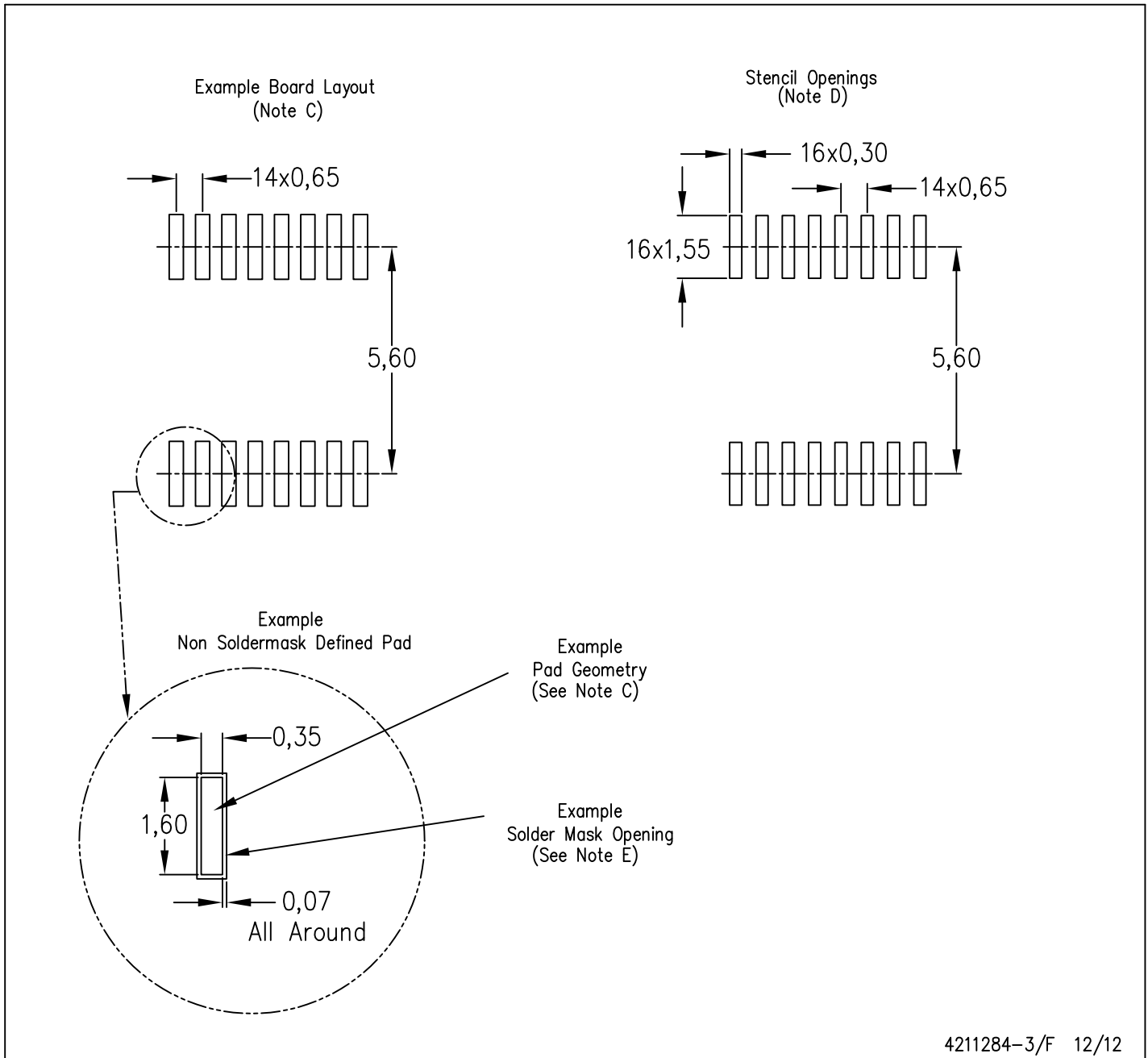


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com