nRF54L15 DK Hardware

v0.9.1

User Guide

4503_209 / 2024-12-04

NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
December 2024	Editorial update
November 2024	First release

Environmental and safety notices

Power supply

The nRF54L15 DK must be powered by a PS1 class (IEC 62368-1) power supply with maximum power less than 15 W.

Skilled persons

The nRF54L15 DK is intended for use only by skilled persons.

A skilled person is someone with relevant education or experience that enables them to identify potential hazards and takes appropriate action to reduce the risk of injury to themselves and others.

Hot surface

In the event of a fault, touchable surfaces can heat up significantly.

Electrostatic discharge

The nRF54L15 DK is susceptible to *Electrostatic Discharge (ESD)*.

To avoid damage to your device, it should be used in an electrostatic free environment, such as a laboratory.

Environmental Protection

Waste electrical products should not be disposed of with household waste.

Please recycle where facilities exist. Check with your local authority or retailer for recycling advice.

1 Introduction

The nRF54L15 DK is a hardware development platform used to design and develop application firmware on the nRF54L15 *System on Chip (SoC)*.

Key features

- nRF54L15 SoC in QFN48 package
- Support for the following wireless protocols:
  - *Bluetooth*® Low Energy
  - NFC
  - 802.15.4
  - Thread®
  - 2.4 GHz proprietary
- 2.4 GHz and NFC antennas
- *Microwave coaxial connector with switch (SWF)* RF connector for direct RF measurements
- User-programmable LEDs (4) and buttons (4)
- SEGGER J-Link OB programmer/debugger
- Two *Universal Asynchronous Receiver/Transmitter (UART)* interfaces through virtual serial ports
- USB connection to debugger for debugging, programming, and power
- Pins for measuring power consumption
- nPM1300 PMIC providing a 1.8 V to 3.3 V user-programmable power supply from USB

Kit content

The nRF54L15 DK includes hardware, preprogrammed firmware, documentation, hardware schematics, and layout files.

The nRF54L15 DK (PCA10156) comes with an NFC antenna.

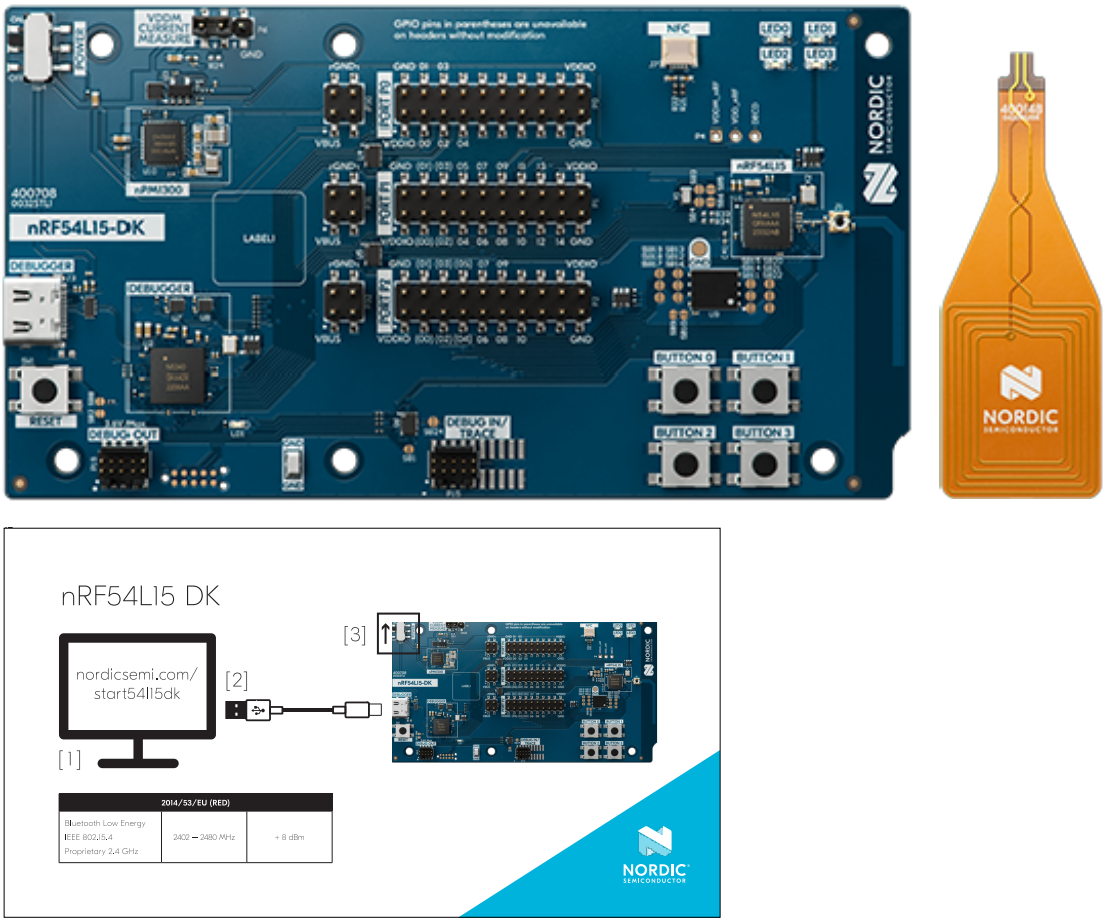

Figure 1: nRF54L15 DK (PCA10156) and NFC antenna

The hardware design files for the nRF54L15 DK are available on the nRF54L15 DK product page. They include the following resources:

- Schematics
- *Printed Circuit Board (PCB)* layout files
- Bill of materials
- Gerber files

2 Hardware description

The main components of the DK include the nRF54L15 *SoC* and hardware peripherals that add functionality and configuration options.

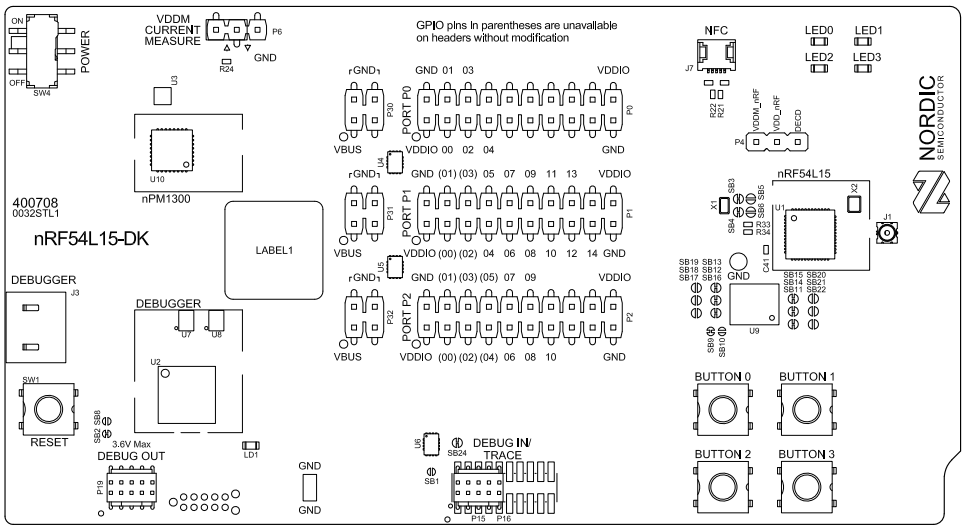

Figure 2: nRF54L15 DK front view

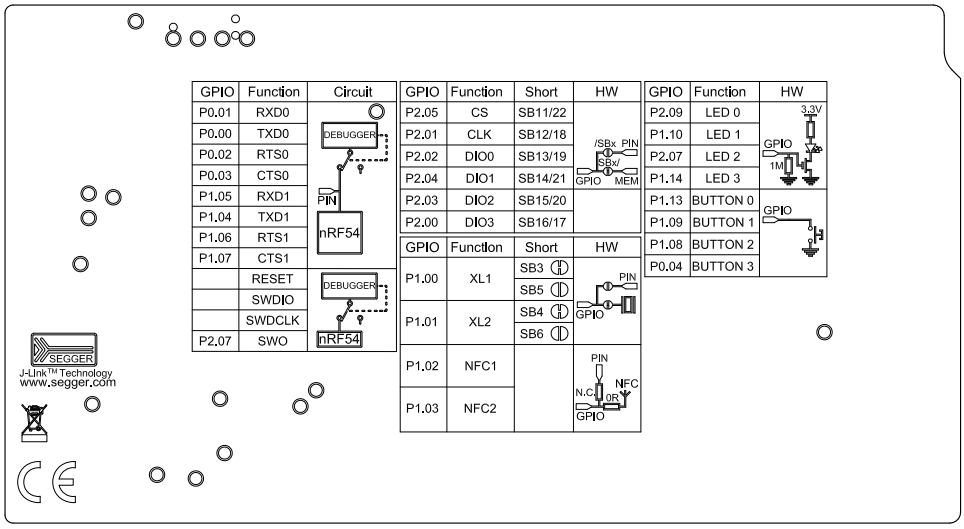

Figure 3: nRF54L15 DK back view

2.1 Block diagram

The block diagram illustrates the nRF54L15 DK functional architecture.

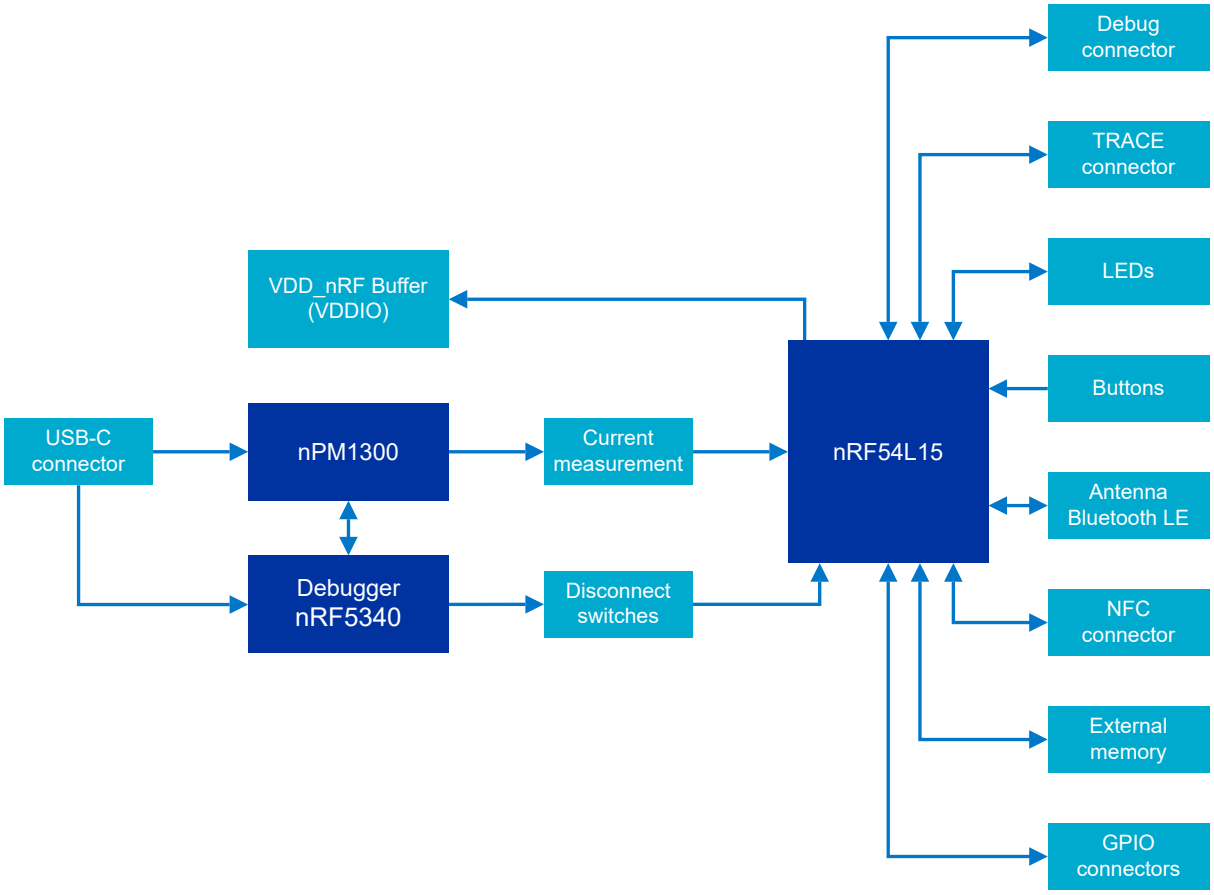

Figure 4: Block diagram

2.2 Power supply

The nRF54L15 DK is fully powered through USB connector **J3** for the debugger (5 V).

2.2.1 VDD power sources

The 5 V domain powers the main supply voltage (P5V0).

This domain consists of the following:

- Buck regulator programmable from 1.8 to 3.3 V
- Voltage follower configured to VDD_nRF of the nRF54L15 I/O voltage

BUCK supplies nRF54L15 VDDM input with a default voltage of 1.8 V, setting it in Normal Voltage Mode. To change the VDDM voltage, use the Board Configurator GUI.

The buffered VDD_nRF is called VDDIO. VDDIO also supplies power to the debugger. The DK uses the VDD_nRF voltage follower to make sure that leakage currents are not drawn from the nRF54L15 device during low current measurements.

> **Note:** On the nRF54L15 DK v0.9.1, the VDDM pin provides the main power source to the nRF54L15 SoC. In later versions and reference designs, VDDM pin 48 is called VDD and shorted to VDD pin 47.

For more information about power sources, see nRF54L15 SoC direct supply on page 9.

2.2.2 nRF54L15 SoC direct supply

The application can be powered directly from a source in isolation without powering the rest of the nRF54L15 DK. The 5 V domain must be supplied from the debugger USB connector **J3** to ensure the pins of the nRF54L15 *SoC* are not connected to unpowered devices.

Remove the jumper to connect the external source to the external supply connector **P6**. The allowed voltage range is from 1.8 V to 3.6 V.

Since only the nRF54L15 is supplied from this source, it is important that the 5 V domain is supplied from the interface debugger USB connector **J3** to ensure the pins of the nRF54L15 are not connected to unpowered devices.

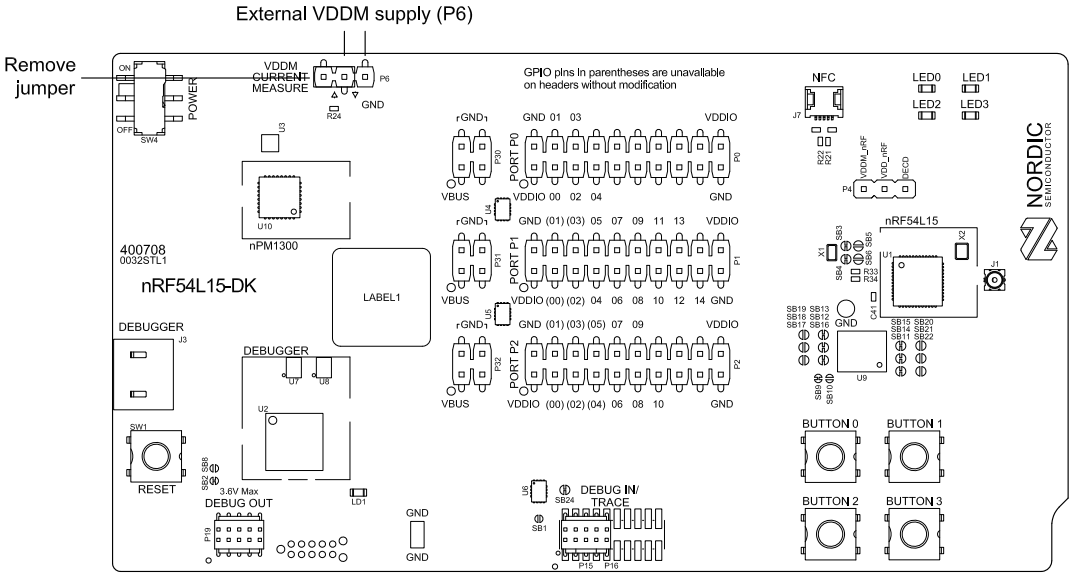

Figure 5: External VDDM supply

2.3 External memory

The nRF54L15 DK has a 64 Mb external flash memory. The memory is a multi-I/O memory supporting both *Serial Peripheral Interface (SPI)* and *Quad Serial Peripheral Interface (QSPI)*.

The memory is connected to the chip using the following GPIOs.

GPIO	Flash memory pin	Solder bridge for memory use (default: shorted)	Solder bridge for GPIO use (default: open)
P2.05	CS	SB11	SB22
P2.01	CLK	SB12	SB18
P2.02	SIO_0/SI	SB13	SB19
P2.04	SIO_1/SO	SB14	SB21
P2.03	SIO_2/WP	SB15	SB20
P2.00	SIO_3/HOLD	SB16	SB17

Table 1: Flash memory GPIO usage and connecting solder bridges

In addition to onboard external memory, a GPIO can be used for additional tasks from the **P2** connector. To enable this, cut solder bridges **SB11**–**SB16** and short solder bridges **SB17**–**SB22** to make the GPIOs available on the **P2** connector and usable for other purposes. See the following figure for more information.

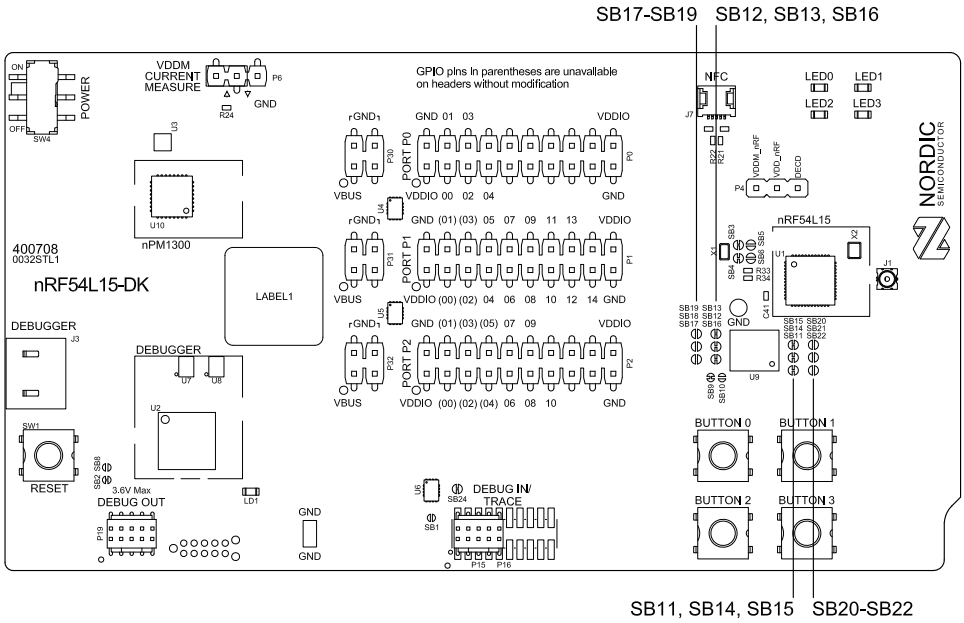

Figure 6: Configuring GPIOs for external memory

Note: If debugging the QSPI communication is needed, solder bridges **SB17**–**SB22** can be shorted without cutting solder bridges **SB11**–**SB16**, but the pins should not be driven externally.

By default, the VDDIO domain powers external memory. The power to the external memory can be configured to come from the VDD_nRF domain instead by using solder bridges **SB9** and **SB10**. If VDD_nRF is selected, the power consumption of the external memory is added to the nRF54L15 current measured on **P6**. See the following table for configuration.

Power source	Solder bridge	Default state
VDD_IO	**SB9**	Shorted
VDD_nRF	**SB10**	Open

Table 2: Flash memory power source configuration

2.4 Connector interface

Access to the nRF54L15 GPIOs is available from connectors **P0**, **P1**, and **P2**.

The **P6** connector and **P4** test points provides access to ground and power on the nRF54L15 DK.

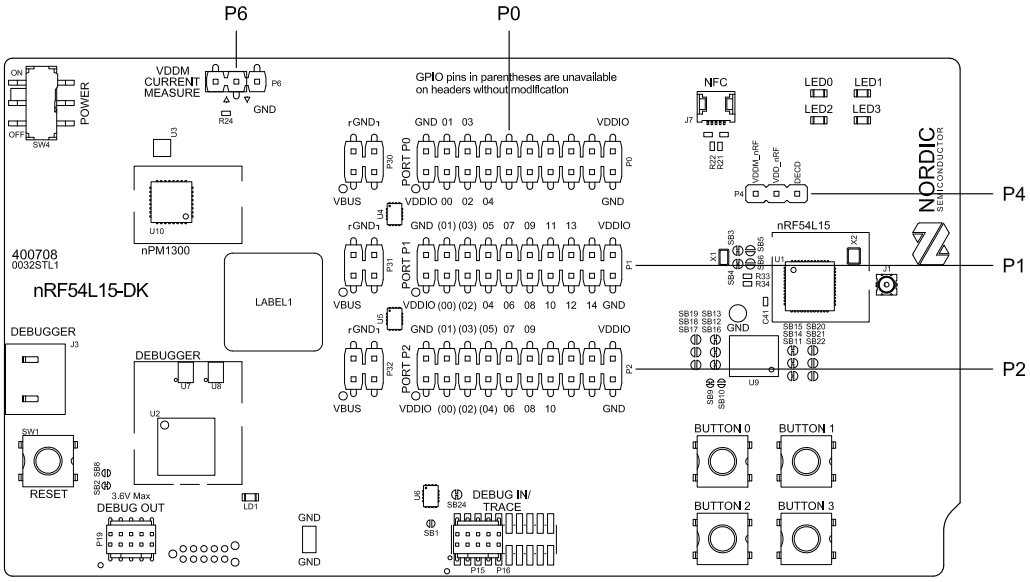

Figure 7: nRF54L15 DK connectors

Pin maps

P0 signal	Function	Peripheral	Default connected on P0
P0.00	UART0_TXD		Yes
P0.01	UART0_RXD		Yes
P0.02	UART0_RST		Yes
P0.03	UART0_CST		Yes
P0.04		Button 3	Yes

Table 3: P0 pin map

P0 signal	Function	Peripheral	Default connected on P1
P1.00	32.768 kHz, XL1		No, solder bridges must be configured
P1.01	32.768 kHz, XL2		No, solder bridges must be configured
P1.02	NFC1		No, 0R resistors must be configured
P1.03	NFC2		No, 0R resistors must be configured
P1.04	UART1_TXD		Yes
P1.05	UART1_RXD		Yes
P1.06	UART1_RST		Yes
P1.07	UART1_CTS		Yes
P1.08		Button 2	Yes
P1.09		Button 1	Yes
P1.10		LED 1	Yes
P1.11			Yes
P1.12			Yes
P1.13		Button 0	Yes
P1.14		LED 3	Yes

Table 4: P1 pin map

P2 signal	Function	Peripheral	Default connected on P2
P2.00	SPI_IO3	External flash	No, solder bridges must be configured
P2.01	SPI_CLK	External flash	No, solder bridges must be configured
P2.02	SPI_IO0	External flash	No, solder bridges must be configured
P2.03	SPI_IO2	External flash	No, solder bridges must be configured
P2.04	SPI_IO1	External flash	No, solder bridges must be configured
P2.05	SPI_CS	External flash	No, solder bridges must be configured
P2.06	Trace CLK		Yes
P2.07	Trace [0]	LED 2	Yes
P2.08	Trace [1]		Yes
P2.09	Trace [2]	LED 0	Yes
P2.10	Trace [3]		Yes

Table 5: P2 pin map

Connectors **P3**, **P5**, and **P7** are power supply pins that each provide 5.0 V for shields connected to GPIO ports.

P3, P5, P7 signal	Function
1	VBUS from **J3**
2	Ground
3	N.C.
4	Ground

Table 6: P3, P5, and P7 signal map

2.5 Buttons and LEDs

The four buttons and four LEDs on the nRF54L15 DK are connected to dedicated GPIOs on the nRF54L15 *SoC*.

Part	GPIO
Button 0	`P1.13`
Button 1	`P1.09`
Button 2	`P1.08`
Button 3	`P0.04`
LED 0	`P2.09`
LED 1	`P1.10`
LED 2	`P2.07`
LED 3	`P1.14`

Table 7: Button and LED connections

The buttons are active low, which means that input is connected to ground when the button is activated. The buttons do not have an external pull-up resistor, so pins `P0.04`, `P1.08`, `P1.09`, and `P1.13` must be configured as input with an internal pull-up resistor to use the buttons.

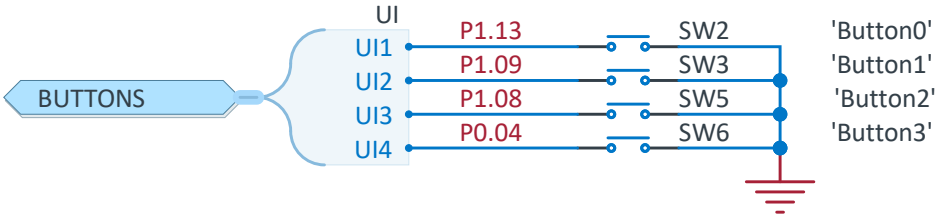

Figure 8: Button configuration

The LEDs are active high, meaning that writing a logical `1` to the output pin turns on the LED. The LEDs are not directly connected to the nRF54L15 GPIOs, but are buffered by a transistor. The transistor gate has a 1 MΩ resistor to GND.

The main power supplying the LEDs can be disabled if needed. This can only be done through the Board Configurator GUI.

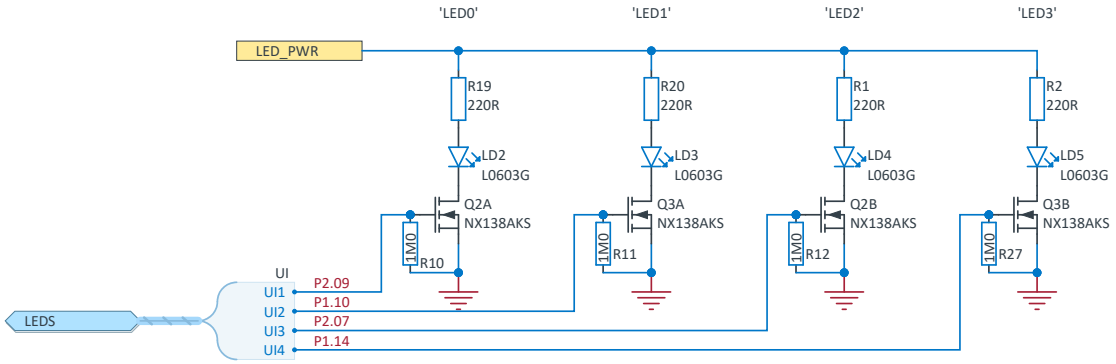

Figure 9: LED configuration

2.6 32.768 kHz crystal

The nRF54L15 *SoC* can use the optional 32.768 kHz crystal **X1** for higher accuracy and lower average power consumption.

On the nRF54L15 DK, **P0.00** and **P0.01** are used for the 32.768 kHz crystal by default and are not available as GPIO on the connectors.

If **P0.00** and **P0.01** are needed as normal I/Os, then the 32.768 kHz crystal **X1** can be disconnected and the GPIO routed to the connectors. Cut the solder bridges on **SB3** and **SB4**, and solder **SB5** and **SB6**. See the following figure for reference.

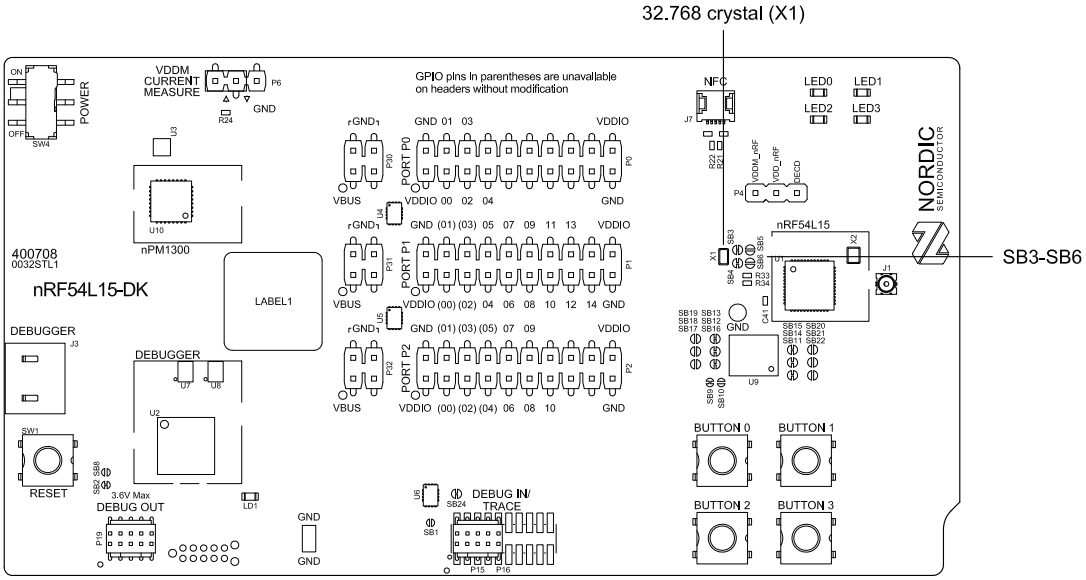

*Figure 10: Configure **P0.00** and **P0.01***

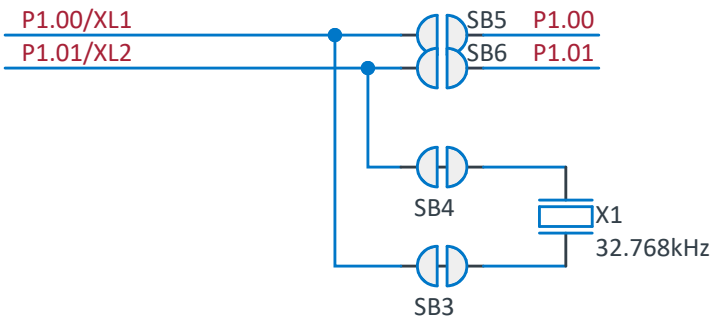

*Figure 11: 32.768 kHz crystal and **SB3–SB6***

2.7 NFC antenna interface

The nRF54L15 DK supports an NFC tag.

NFC-A Listen Mode operation is supported on the nRF54L15 *SoC*. The NFC antenna input is available on connector **J7** on the nRF54L15 DK.

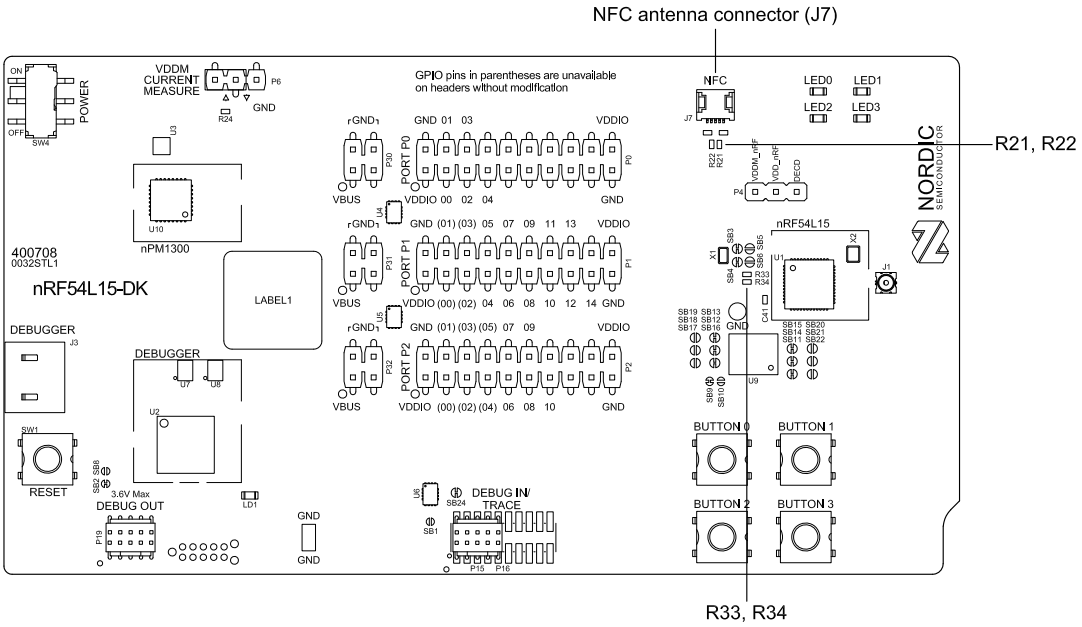

Figure 12: NFC antenna connector

NFC uses pins **NFC1** and **NFC2** to connect the antenna. These pins are shared with GPIOs **P1.02** and **P1.03**. The PROTECT field of the NFCPINS register in *User Information Configuration Registers (UICR)* defines the usage of these pins and their protection level against abnormal voltages. The content of the NFCPINS register is reloaded at every reset.

Configuring NFC pins as GPIOs

The NFC pins are enabled by default. NFC can be disabled and GPIOs enabled by setting the CONFIG_NFCT_PINS_AS_GPIOS to `y`. See Configuring and building for instructions.

Pins **P1.02/NFC1** and **P1.03/NFC2** are by default configured to use the NFC antenna. To use these pins as GPIO, do not connect **R21** and **R22** and short **R33** and **R34** with a 0 Ω resistor.

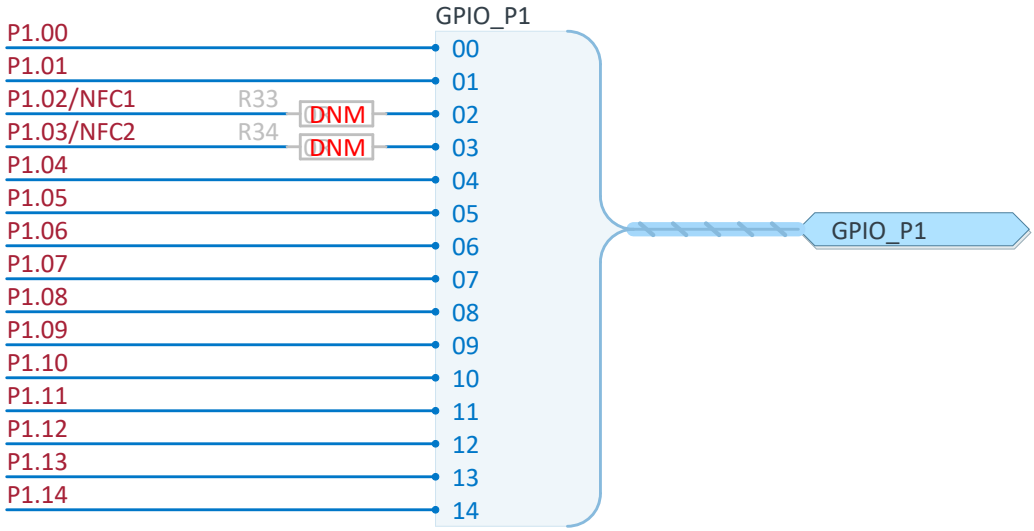

Figure 13: NFC GPIOs

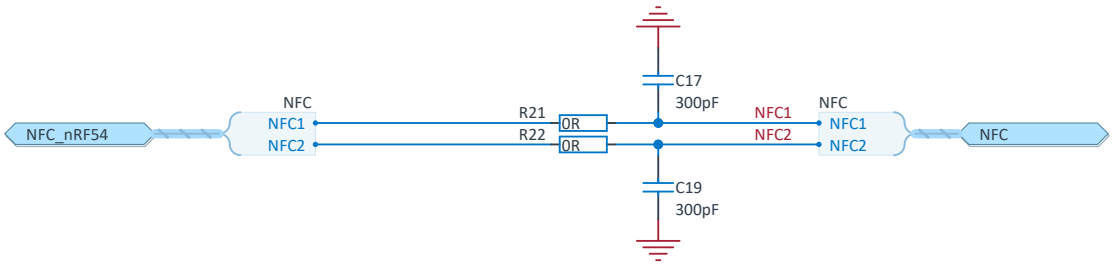

Figure 14: NFC network

2.8 Solder bridge configuration

The nRF54L15 DK has a range of solder bridges for enabling or disabling functionality on the *Development Kit (DK)*. Changes to solder bridges are not needed for normal use of the DK.

The following table is an overview of the solder bridges on the nRF54L15 DK.

Solder bridge	Default	Function
SB1	Open	Short to connect RESET button line to nRF54L15
SB2	Closed	Cut to disconnect debugger from the RESET button line
SB3	Closed	Cut to disconnect the 32.768 kHz on **P1.00**
SB4	Closed	Cut to disconnect the 32.768 kHz on **P1.01**
SB5	Open	Short to enable **P1.00** as normal GPIO
SB6	Open	Short to enable **P1.01** as normal GPIO
SB8	Open	Short **R23**, 100 k pull-up resistor to the RESET button line
SB9	Closed	Cut to disconnect VDDIO from **U9** external flash power
SB10	Open	Short to connect **U9** external flash to VDD_nRF domain
SB11	Closed	Cut to disconnect the SPI external memory from **P2.05**
SB12	Closed	Cut to disconnect the SPI external memory from **P2.01**

Solder bridge	Default	Function
SB13	Closed	Cut to disconnect the SPI external memory from **P2.02**
SB14	Closed	Cut to disconnect the SPI external memory from **P2.04**
SB15	Closed	Cut to disconnect the SPI external memory from **P2.03**
SB16	Closed	Cut to disconnect the SPI external memory from **P2.00**
SB17	Open	Short to enable **P2.00** as a normal GPIO
SB18	Open	Short to enable **P2.01** as a normal GPIO
SB19	Open	Short to enable **P2.02** as a normal GPIO
SB20	Open	Short to enable **P2.03** as a normal GPIO
SB21	Open	Short to enable **P2.04** as a normal GPIO
SB22	Open	Short to enable **P2.05** as a normal GPIO
SB24	Closed	Cut to disconnect **P2.07** from debugger if used as SWO pin

Table 8: Solder bridge configuration

2.9 Board control

The debugger contains a board controller that controls the signals which enable and disable features on the nRF54L15 DK.

All features on the nRF54L15 DK have a default setting that is applied at the first boot. The configuration of the board controller can be changed through nRF Connect for Desktop's Board Configurator application. For more information, see Board Configurator app.

3 Program and debug

The debugger on the nRF54L15 DK programs and debugs the nRF54L15 application firmware.

3.1 Debugger

The debugger on the nRF54L15 DK runs SEGGER J-Link *Onboard (OB)* interface firmware.

3.1.1 RESET button

The nRF54L15 DK is equipped with a RESET button **SW1** connected to the debugger. It resets the nRF54L15 *SoC* or any device connected to the external programming connectors.

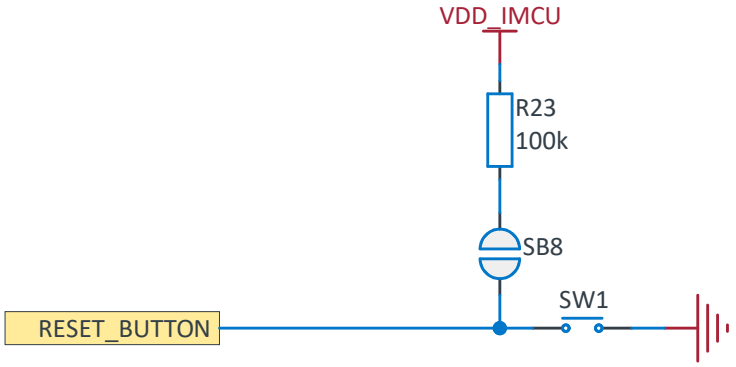

Figure 15: nRF54L15 DK RESET button

The RESET button can be routed directly to nRF54L15 through **SB1** and **SB2**. An optional pull-up resistor can be connected through **SB8** to the RESET button node.

3.1.2 Virtual serial ports

The debugger features two virtual serial ports, each with a *UART* interface.

The serial ports have the following features:

- Flexible baud rate setting up to 1 Mbps (baud rate 921,600 bps is not supported)
- Dynamic *Hardware Flow Control (HWFC)*
- Tri-stated UART lines when no terminal is connected

The following table lists the nRF54L15 *SoC* UART GPIO pins and their signals.

Signal	nRF54L15 UART_0 - Serial Port 0	nRF54L15 UART_1 - Serial Port 1
TXD	P0.00	P1.04
RXD	P0.01	P1.05
RTS	P0.02	P1.06
CTS	P0.03	P1.07

Table 9: nRF54L15 GPIOs mapped to serial port/UART signals

The UART pins connected to the debugger are tri-stated when no terminal is connected to the virtual serial port on the computer. The terminal software must send a *Data Terminal Ready (DTR)* signal to configure the UART debugger pins.

P0.02/P1.06 *Request to Send (RTS)* and **P0.03/P1.07** *Clear to Send (CTS)* can be used for other purposes when HWFC is disabled on the SoC.

The UART signals are routed to the debugger through analog switches **U4** and **U5**.

UART pins for other tasks

For each UART instance, the TXD/RXD signals as a group and RTS/CTS signals as a group can only be disconnected from the debugger together using one switch. This can be done through the Board Configurator GUI.

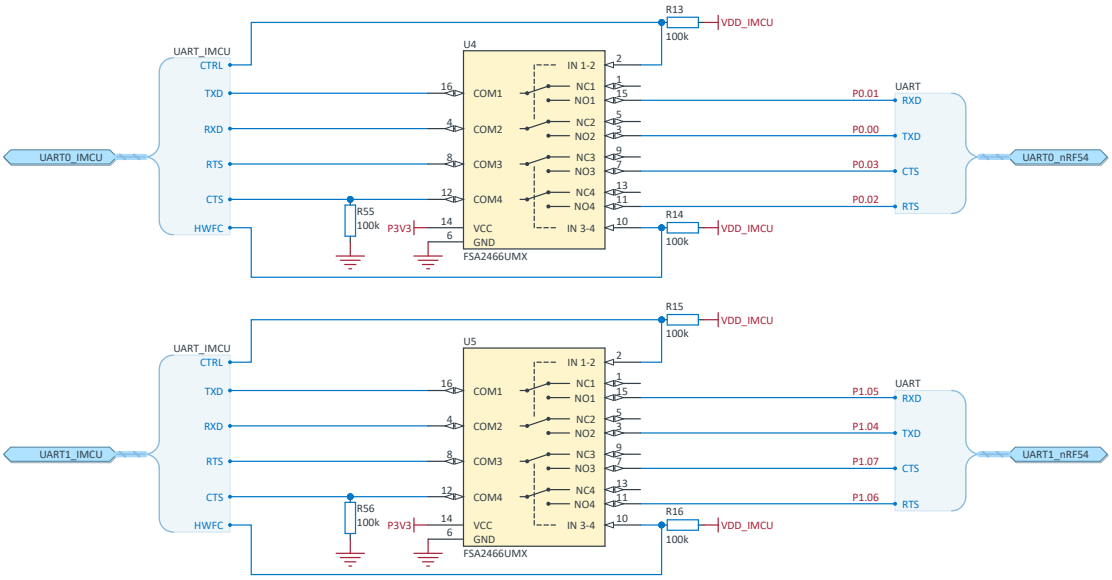

Figure 16: Analog switches between debugger and nRF54L15 DK

3.1.3 Dynamic hardware flow control

When the debugger receives a *DTR* signal from a terminal, it performs automatic *HWFC* detection.

HWFC detection

Automatic HWFC detection is done by driving *CTS* from the debugger and evaluating the state of *RTS* when data is first sent or received. If the state of RTS is high, it is assumed HWFC is not in use. If HWFC is not detected, pins **P0.03/P1.07** (CTS) and **P0.02/P1.06** (RTS) are free for the nRF application to use.

After a power-on reset of the debugger, all UART lines are tri-stated when no terminal is connected to the virtual serial port. If HWFC has been used and detected, **P0.03/P1.07** (CTS) is driven by the debugger until a power-on reset has been performed or until a new DTR signal is received and the detection is redone.

The debugger has a pull-down 100 kΩ resistor connected from CTS to ground.

3.2 Debug input and trace

Use the Debug In connector **P15** to connect external debuggers.

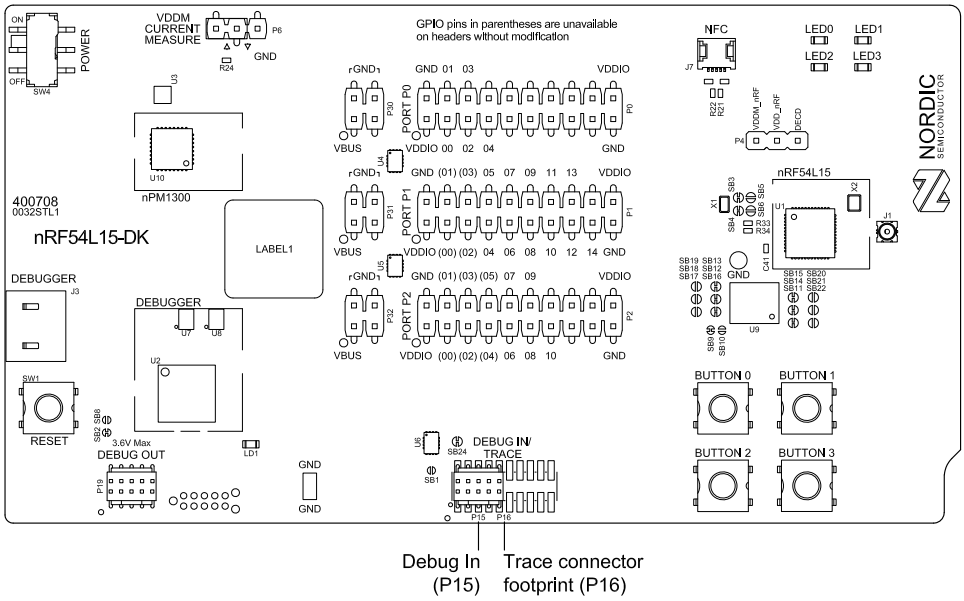

Figure 17: Debug input and trace connectors

For trace, a 20-pin connector footprint **P16** is available. If trace functionality is required, it is possible to mount a 1.27 mm 2x10 pin pitch surface-mount pin header.

The Debug In connector **P15** partially shares the same footprint, so the 2x5 SWD Debug In **P15** connector must first be removed.

GPIO	Trace	Default use
P2.06	TRACECLK	
P2.07	TRACEDATA[0]	LED2
P2.08	TRACEDATA[1]	
P2.09	TRACEDATA[2]	LED0
P2.10	TRACEDATA[3]	

Table 10: Default and Trace GPIOs

The reference voltage for the debug input and trace is connected to **VDDIO**.

3.3 Debug out for programming external boards

The nRF54L15 DK supports programming and debugging external boards with an nRF51, nRF52, nRF53, and nRF54 Series *SoC*, or the nRF91 Series *System in Package (SiP)*.

To program or debug an external board, connect to the Debug out connector (**P19**) using a 10-pin cable.

Note: Power the external board separately from the DK. The VDDIO voltage on the external board must be within the range of 1.8 V to 3.6 V.

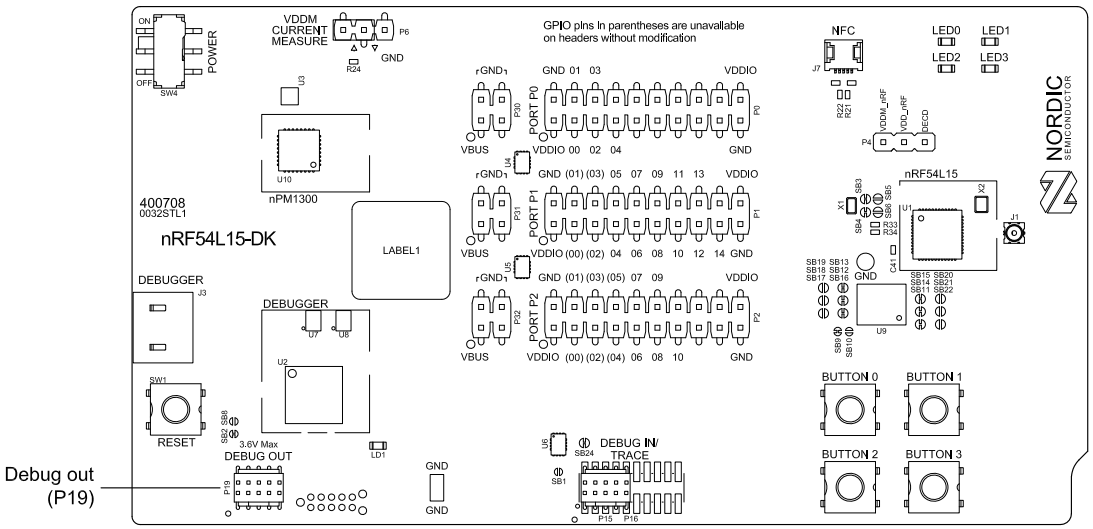

Figure 18: Debug output connector

3.3.1 Program an external board

Connect boards with a standard 10-pin *Serial Wire Debug (SWD)* connector to **P19**.

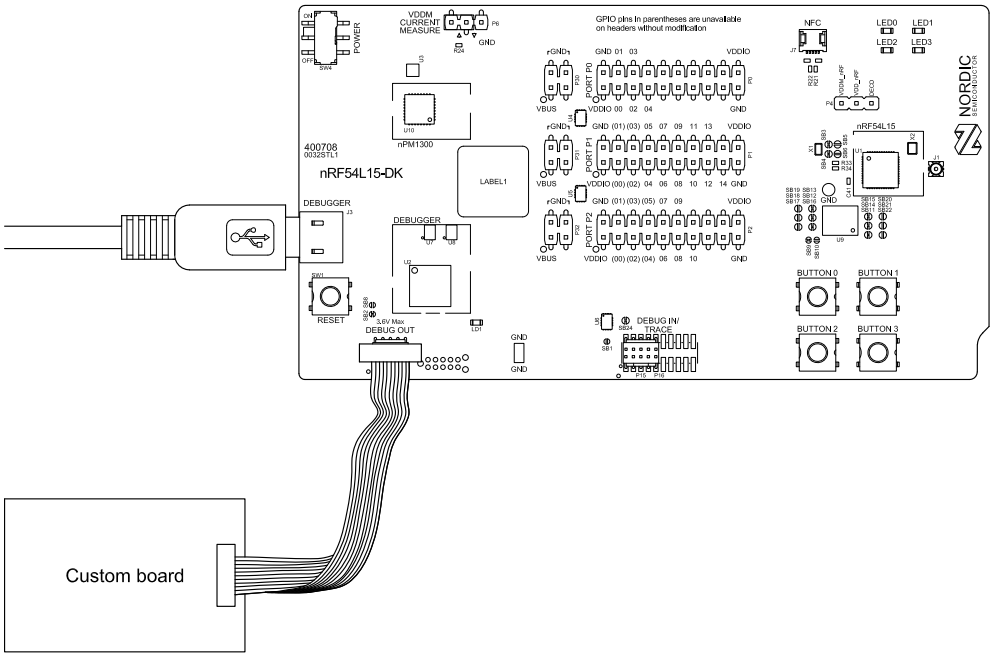

Figure 19: Connecting an external board to P19

Power the external board separately from the DK. The VDDIO voltage on the external board must be within the range of 1.8 V to 3.6 V.

The debugger programs or debugs the target chip on the external board instead of the onboard nRF54L15 *SoC* when pin 3 (**`SWD0_SELECT`**) of **P19** is connected to **GND** through the 10-pin flat cable.

The following figure and table describe the **P19** connector pinout.

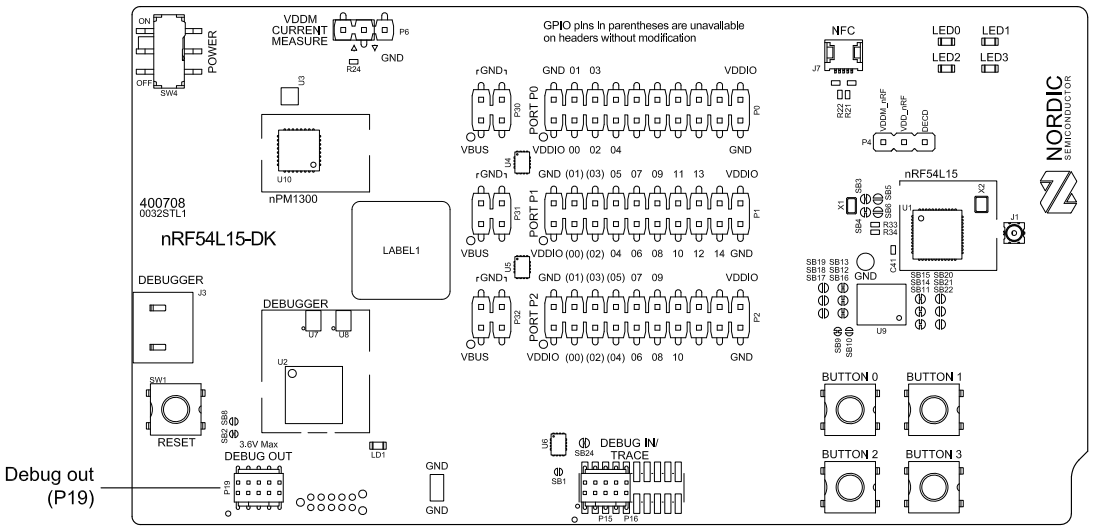

*Figure 20: Debug output connector **P19***

Pin number	Signal	Description
1	SWD0_VTG	I/O voltage reference input for SWD0 signals
2	SWD0_SWDIO	*SWD* data I/O
3	SWD0_SELECT	Debug out select signal, connect to ground on external board
4	SWD0_SWDCLK	Serial Wire Clock line
5	GND	Ground
6	SWD0_SW0	*Serial Wire Output (SWO)* line is not used for programming and debugging over SWD
7	N.C.	Not used
8	N.C.	Not used
9	N.C.	Not used
10	SWD0_RESET	Reset line

*Table 11: Connector **P19** pinout for programming external targets*

4 Measurements

Current and radio frequency (RF) can be measured on the nRF54L15 DK.

4.1 Current measurements

The current drawn by the application nRF54L15 *SoC* can be monitored on the nRF54L15 DK.

Current can be measured using any of the following test instruments:

- Power Profiler Kit II (PPK2)
- Oscilloscope
- Ampere meter
- Power analyzer

The following sections provide information on the DK measurement setup. If the PPK2 is used for measuring current, see the Power Profiler Kit II User Guide for additional instructions. Power analyzer measurements are not described in this document.

The application nRF54L15 SoC power supply is VDDM (1.8 V to 3.6 V). The nRF54L15 DK can measure current on VDDM using **P6**.

> **Note:** The current measurement is unreliable if a serial terminal is connected to the virtual serial port.

For more information on current measurement, see the tutorial Current measurement guide: Introduction.

4.1.1 Set up the DK

Perform the following to prepare the *DK* for measuring current:

- Consider disconnecting the virtual serial port connections between the debugger and the nRF54L15 *SoC* using the analog switches as described in Virtual serial ports on page 18.
- Use the analog switch on the *SWD* interface that can disconnect the programming interface connections between the debugger and the nRF54L15.

To reprogram the nRF54L15 while the DK is prepared for current measurements, remove measurement devices from **P6**.

4.1.2 Measure current profile with an oscilloscope

An oscilloscope can be used to measure the average current over a given time interval and capture the current profile.

1. Prepare the *DK* as described in Set up the DK.
2. Mount a 10 Ω resistor on the footprint for **R24**.
3. Set the oscilloscope to differential mode or a mode that is similar.
4. Connect the oscilloscope using two probes on the pins of the **P22** connector, as shown in the following figure.
5. Calculate or plot the instantaneous current from the voltage drop across the 10 Ω resistor by taking the difference of the voltages measured on the two probes.

The voltage drop is proportional to the current. The 10 Ω resistor causes a 10 mV drop for each 1 mA drawn by the circuit being measured.

The plotted voltage drop can be used to calculate the current at a given point in time. The current can then be averaged or integrated to analyze current and energy consumption over a period.

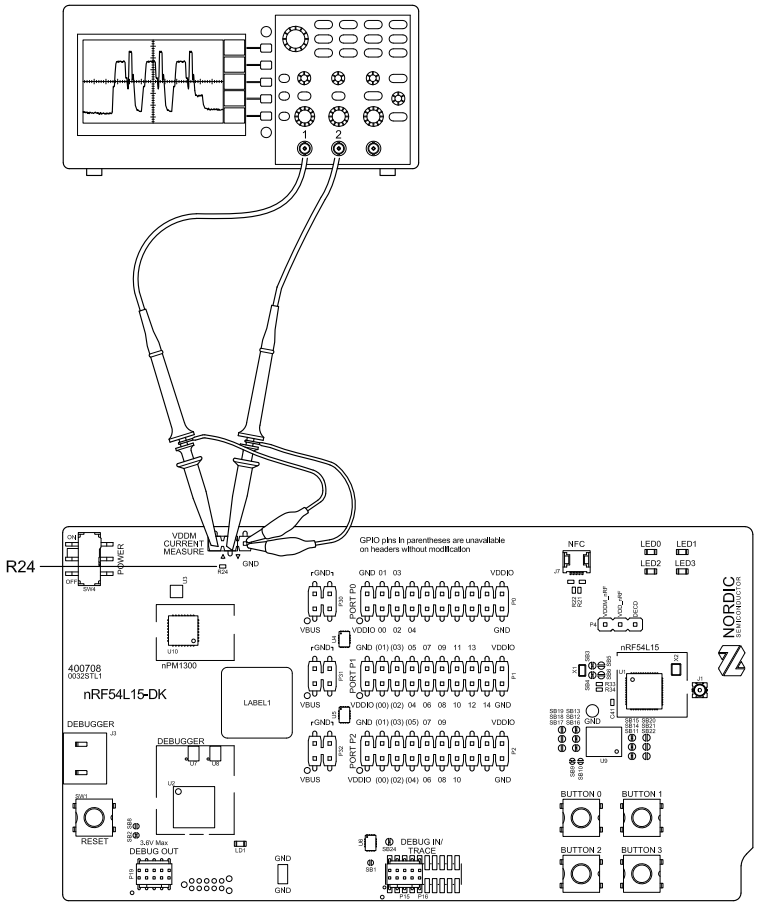

Figure 21: Current measurement with an oscilloscope

To reduce noise, do the following:

- Use probes with 1x attenuation.
- Enable averaging mode to reduce random noise.
- Enable high-resolution function if available.

Use a minimum of 200 kSa/s (one sample every 5 µs) to get the correct average current measurement.

4.1.3 Measure average current with an ampere meter

The average current drawn by the application nRF54L15 *SoC* can be measured using an ampere meter. This method monitors the current in series with the nRF device. A true *Root Mean Square (RMS)* ampere meter is recommended.

1. Prepare the *DK* as described in Set up the DK.
2. Connect an ampere meter between the pins of connector **P6** as shown in the following figure.
3. Set the average timing of the ampere meter to a long interval, such as 1 s or longer.
4. Set the dynamic range of the ampere meter between 1 µA and 15 mA, so that it is wide enough to provide accurate measurements.

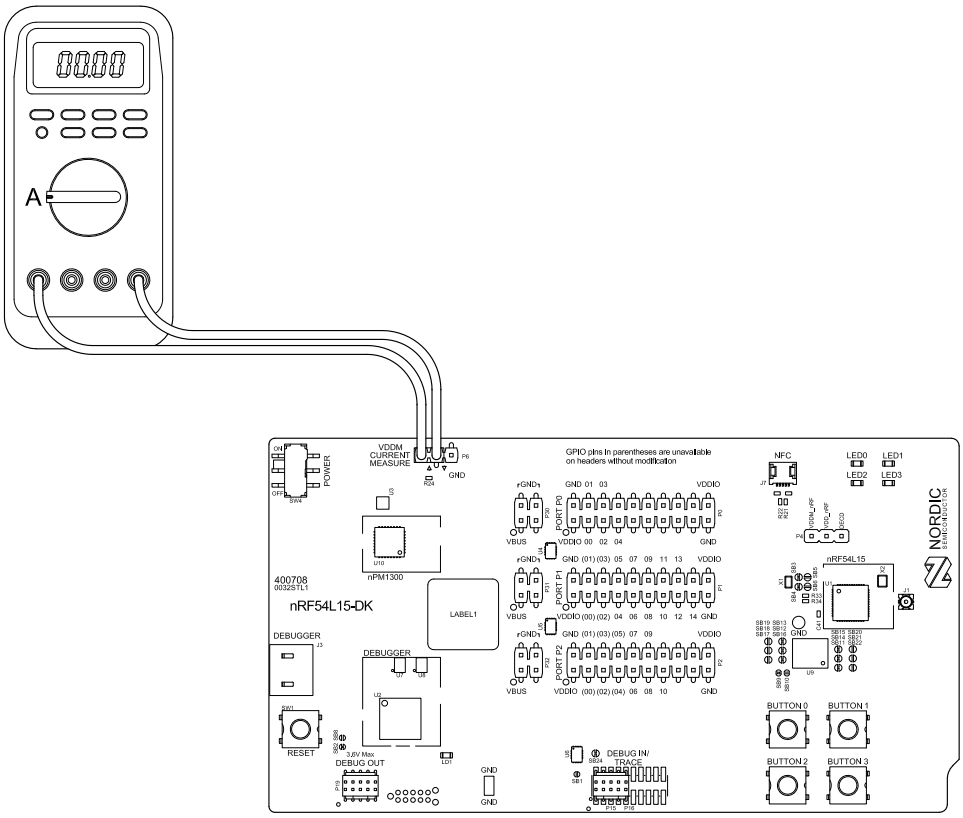

Figure 22: Current measurement with an ampere meter

4.2 RF measurements

The nRF54L15 DK is equipped with a small coaxial connector (**J1**) to measure the RF signal with a spectrum analyzer.

The connector is an SWF type (Murata part no. MM8130-2600) with an internal switch. By default, when a cable is not attached, the RF signal is routed to the onboard trace antenna.

In this example, a test probe (Murata part no. MXHS83QE3000) is used with a standard *SubMiniature Version A (SMA)* connection on the other end for connecting instruments. The test probe is not included in the kit. When connecting the test probe, the internal switch in the SWF connector disconnects the onboard antenna and connects the RF signal from the nRF54L15 *SoC* to the test probe.

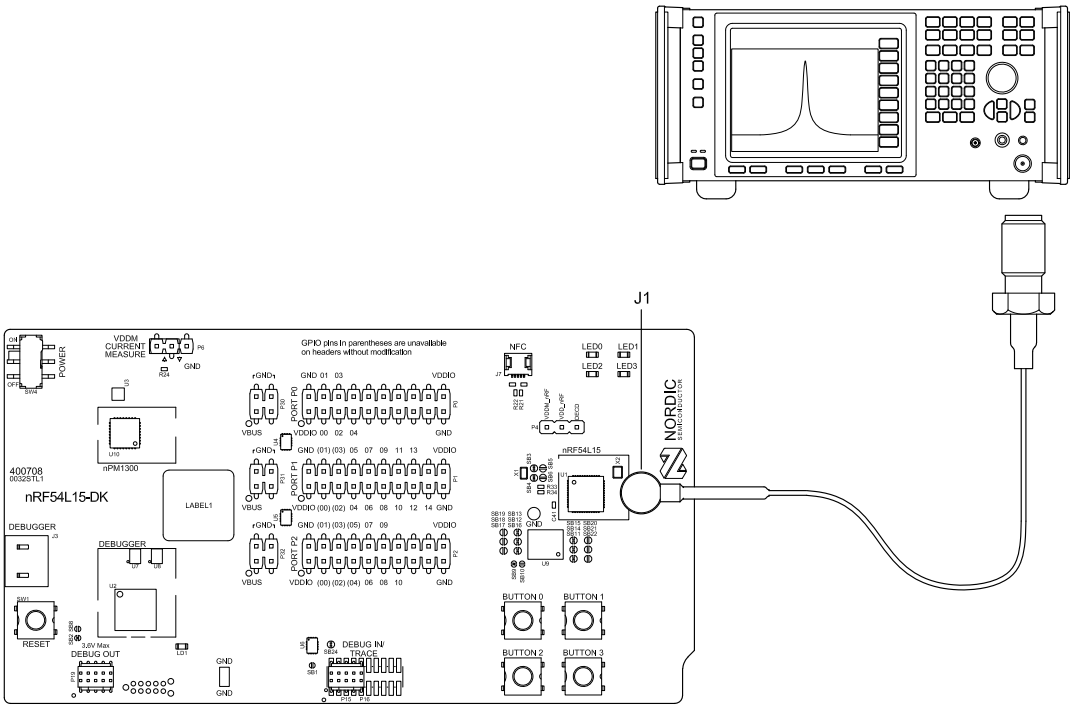

Figure 23: Connecting a spectrum analyzer

The connector and test probe add loss to the RF signal. See the following table for more information or consult the test probe user guide if you are using another model.

Frequency (MHz)	Loss (dB)
2440	1.0
4880	1.7
7320	2.6

Table 12: Typical loss in connector and test probe, using Murata part no. MXHS83QE3000

Glossary

Clear to Send (CTS)

In flow control, the receiving end is ready and telling the far end to start sending.

Data Terminal Ready (DTR)

A control signal in RS-232 serial communications transmitted from data terminal equipment, such as a computer, to data communications equipment.

Development Kit (DK)

A hardware development platform used for application development.

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Hardware Flow Control (HWFC)

A handshaking mechanism used to prevent an overflow of bytes in modems. It uses two dedicated pins on the RS-232 connector, Request to Send and Clear to Send.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

Lithium-polymer (Li-Poly)

A rechargeable battery of lithium-ion technology using a polymer electrolyte instead of a liquid electrolyte.

Mass Storage Device (MSD)

Any storage device that makes it possible to store and port large amounts of data in a permanent and machine-readable fashion.

Microwave coaxial connector with switch (SWF)

A small, RF surface-mount switch connector series for wireless applications.

NFC-A Listen Mode

Initial mode of an NFC Forum Device when it does not generate a carrier. The device listens for the remote field of another device. See Near Field Communication (NFC).

Onboard (OB)

A function that is delivered on the chip microcontroller.

Operational Amplifier (op-amp)

A high-gain voltage amplifier that has a differential input and, usually, a single output.

Printed Circuit Board (PCB)

A board that connects electronic components.

Quad Serial Peripheral Interface (QSPI)

A Serial Peripheral Interface (SPI) controller that allows the use of multiple data lines.

Receive Data (RXD)

A signal line in a serial interface that receives data from another device.

Request to Send (RTS)

In flow control, the transmitting end is ready and requesting the far end for a permission to transfer data.

Root Mean Square (RMS)

An RMS meter calculates the equivalent Direct Current (DC) value of an Alternating Current (AC) waveform. A true RMS meter can accurately measure both pure waves and the more complex nonsinusoidal waves.

Serial Peripheral Interface (SPI)

Synchronous serial communication interface specification used for short-distance communication.

Serial Wire Debug (SWD)

A standard two-wire interface for programming and debugging Arm® CPUs.

Serial Wire Output (SWO)

A data line for tracing and logging.

SubMiniature Version A (SMA)

A semi-precision coaxial RF connector for coaxial cables with a screw-type coupling mechanism.

System in Package (SiP)

Several integrated circuits, often from different technologies, enclosed in a single module that performs as a system or subsystem.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Transmit Data (TXD)

A signal line in a serial interface that transmits data to another device.

Universal Asynchronous Receiver/Transmitter (UART)

A hardware device for asynchronous serial communication between devices.

Universal Serial Bus (USB)

An industry standard that establishes specifications for cables and connectors and protocols for connection, communication, and power supply between computers, peripheral devices, and other computers.

User Information Configuration Registers (UICR)

Non-volatile memory registers used to configure user-specific settings.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nRF54L15 Datasheet
- nRF54L15 Errata

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