Industrial Application
Battery Monitoring IC

KA49517A
Product Brief

For additional information or question, please contact Nuvoton Technology Corporation Japan.
www.nuvoton.co.jp

■ IMPORTANT NOTICE

Regarding the specifications of this product, it is considered that you have agreed to the quality level and disclaimer described below.

Support for industry standards and quality standards

Functional safety standards for automobiles ISO26262	**No**
AECQ-100	**No**
Market failure rate	**50Fit**

Disclaimer

1. When the application system is designed using this IC, please design the system at your own risk. Please read, consider, and apply appropriate usage notes and description in this standard.

2. When designing your application system, please take into the consideration of break down and failure mode occurrence and possibility in semiconductor products. Measures on the systems such as, but not limited to, redundant design, mitigating the spread of fire, or preventing glitch, are recommended in order to prevent physical injury, fire, social damages, etc. in using the Nuvoton Technology Japan Corporation (hereinafter referred to as NTCJ) products.

3. When using this IC, for each actual application systems, verify the systems and the all functionality of this IC as intended in application systems and the safety including the long-term reliability at your own risk

4. Please use this IC in compliance with all applicable laws, regulations and safety-related requirements that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. NTCJ shall not be held responsible for any damage incurred as a result of this IC being used not in compliance with the applicable laws, regulations and safety-related requirements.

5. This IC does not have any security functions using cryptographic algorithms, such as authentication, encryption, tampering detection.

6. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular industry standard (e.g., ISO 9001, IATF 16949, ISO 26262, etc.), this IC is neither designed nor intended for use in such environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular industry standard.

7. Using IC that have been indicated as compliant with industry functional safety standards does not warrant that the application meets the requirements of industry functional safety standards. NTCJ shall not be held responsible for the application compliance with requirements of the particular industry functional safety standard.

8. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular quality standard (e.g., AECQ-100, etc.), this IC is neither designed nor intended for use in such the environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular quality standard.

9. In case of damages, costs, losses, and/or liabilities incurred by NTCJ arising from customer's non-compliance with above from 1 to 8, customer will indemnify NTCJ against every damages, costs, losses and responsibility.

Characteristics

- Maximum support 17 battery cells in series
- 10mV measurement accuracy with 14 bits voltage ADC for cell voltage, and 5 channels analog input measurement for Thermistor
- Built-in 16 bits Low speed Current measurement ADC (Coulomb Counter) and 15 bits High speed Current measurement ADC
- Low–side Sense resistor Current measurement and monitoring
- Operation mode - Active, Standby/Low power; Sleep and Shutdown
- SPI serial communication interface up to 1MHz clock with CRC code correction and watchdog timer
- Built-in ALARM pins for overvoltage, undervoltage, overcurrent and short circuit detection and protection feature
- Built-in cell balancing MOSFET, support external cell balance MOSFET operation as well
- 3 channels General GPIO and 2 channels high voltage output GPOH
- Interrupt signal provision for MCU to notify state of operation as well as measurement cycle indication at the available GPIO pins
- High-side N-MOSFET driver: Charge (CHG) & Discharge (DIS) with built-in charge pump and FETOFF control pin
- Built in controllable fuse driver for cell OV and overcurrent monitoring algorithm to serve as secondary protection system
- Regulator (REG_EXT) for external circuit power provision with selectable output setting 5V/3.3V/2.5V, and 50mA drive ability
- Safety Diagnostic function for measurement related check and FET driver check to enhance the total diagnostic coverage of the chip
- Package : TQFP 64L (10x10x1mm^3, Lead Pitch 0.5mm)

Overview

KA49517A is a battery monitoring IC with protection function. With high resolution ADC built-in, KA49517A is capable to measure battery cell voltage and current level accurately.

Through SPI serial interface, microcontroller unit (MCU) is able to read the status and measured result by KA49517A.

The ALARM pins alert the MCU with the abnormal condition such as over voltage (OV), under voltage (UV),

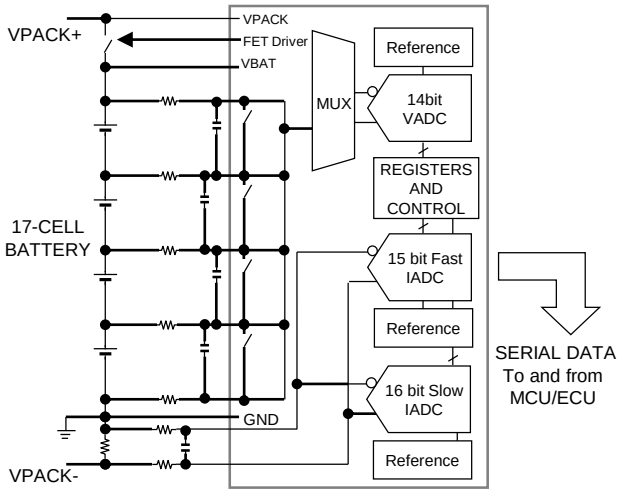
over current (OC) and short circuit (SC).

KA49517A can support an application with up to 17 batteries cells in series or a maximum voltage of 85V, it is suitable for application with high input voltage such as E-bike, UPS etc.

Applications

- Pedelec, e-Bike, UPS, Server Backup System, Power Tool, Energy Storage Systems etc

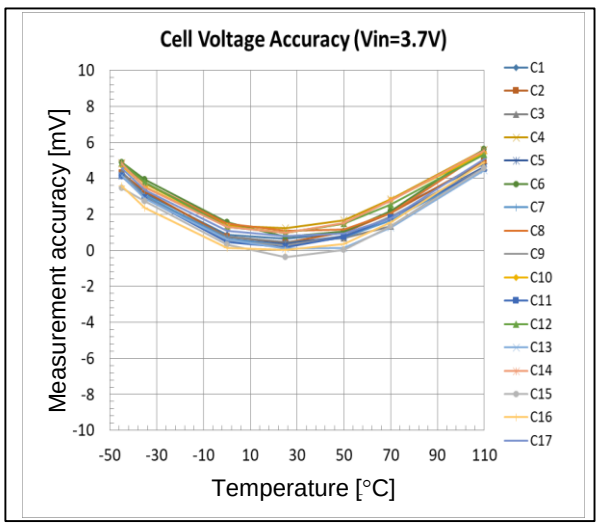
System Block Diagram



Notes: This is just an example of a circuit set: it is not guaranteed to function identically to the final production version. When designing a set for production, make sure to carefully evaluate and verify the circuitry.

Representation Characteristics

Measurement accuracy



Application circuit example (17cells connection), VBAT=62.9V , cell voltage ΔCn (C_n-C_{n-1}) = 3.7V

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Absolute Maximum Ratings

Parameter	Symbol *1	Rating	Unit	Notes
Supply voltage	V_{VBAT} to GND	-0.3 to 130	V	*5
	V_{CVDD} to GND	-0.3 to 6.4	V	*2
	V_{VDD55} to GND	-0.3 to 6.4	V	*2
	V_{VDD18} to GND	-0.3 to 2.3	V	*2
	V_{REGEXT} to GND	-0.3 to 6.4	V	*2
Input Voltage Range	Cn (n=10 ～17)	-0.3 to V_{VBAT}	V	
	Cn (n=1～9)	-0.3 to 38 + 11*(N-1)	V	
	C0	-0.3 to 38	V	
	SEN, SCL, SDI, FETOFF, GPIOn (n=1～3)	-0.3 to V_{CVDD}+0.3	V	*3
	TMONIn (n=1～5), REGSEL	–0.3 to V_{VDD55}+0.3	V	*3
	SRP.SRN	-0.5 to 2.0	V	
	VPC	-0.3 to 130	V	
	LDM	-0.3 to 130	V	
	SHDN	-0.3 to 6.4	V	
Output Voltage Range	ALARM1,SDO,NRST	-0.3 to V_{CVDD}+0.3	V	
	GPOHn (n=1～2)	-0.3 to 130	V	
	REGB	-0.3 to 14	V	
Output Current Range	ALARM1,SDO,NRST GPIOn (n=1～3)	-6.0 to +6.0 (-12.0 to +12.0)	mA	*4
	REGB	-3.5 to 3.5	mA	
	REGEXT	-50.0 to 0	mA	*6
Allowable Voltage Between Pins	C_n - C_{n-1} (n=1～17)	-0.3 to 11	V	
Operating junction temperature	T_j	-40 to 125	°C	*2
Storage temperature	T_{stg}	-55 to 125	°C	*2

Notes: Stresses that exceed the absolute maximum ratings may cause fatal damage to the product.
This specifies the maximum rating for stress.
It is NOT a guaranteed operating region because it exceeds the recommended operating conditions.
The reliability of the IC may be affected if it is kept under absolute maximum rating conditions for long periods.
Applied external current and voltage to pins should also not exceed the absolute maximum ratings listed here.

*1: GND is the voltage of pins GND1, GND2, and GND3 which are connected inside the device.
Connect these pins on the board and apply the same voltage.

*2: The maximum ratings are allowable unless the power consumption exceeds the power dissipation ratings.

*3: V_{CVDD} is the voltage of CVDD. V_{VDD55} is the voltage of VDD55. It should not exceed the rated 6.4 V.

*4: + Polarity is the direction in which current flows into the IC pins.
– Polarity is the direction in which current flows out from the IC pins.

*5: V_{VBAT} is the voltage of VBAT. It should not exceed the rated 130V.

*6: The output circuit consists of both external components and internal circuitry.
Refer to the application circuit diagram.

Power Dissipation Ratings

Package	θj-a	θj-c	P_D (Ta = 25°C)	P_D (Ta=105°C)	Note
TQFP 64L (10x10x1mm^3, Lead Pitch 0.5mm)	37.7 °C/W	2.7 °C/W	2.65 W	0.53 W	*1

Notes: These characteristics are the reference values for design.
Refer to the PD-Ta characteristics diagram in the package specifications. Thermal design with a sufficient margin is recommended based on the conditions of supply voltage, load, and ambient temperature.

*1: Mounting board: Glass epoxy 4-layer board without soldered heat spreader measuring 50 mm x 50 mm x 0.8 mm
Wiring layer thickness: all layers 0.035 mm, proportion of copper foil: 57% / 100% / 100% / 57%

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Recommended Operating Conditions

Below items must be within the range of Recommended Operating Conditions.

Parameter	Symbol *1	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{VBAT}	12.5	62.9	85	V	*2
	V_{CVDD}	3.0	5.0	5.5	V	
Input Voltage Range	C_n - C_{n-1} (n=1～17)	1.0	—	4.8	V	*3
	SEN, SCL, SDI	0	—	V_{CVDD}	V	
	TMONIn (n=1～5)	0	—	V_{VDD55}	V	
	GPIOn (n=1～3)	0	—	V_{CVDD}	V	
	REGSEL	0	—	V_{VDD55}	V	
	SRP,SRN	-0.18	—	0.18	V	
	VPC	0	—	85	V	
	LDM	0	—	85	V	
	SHDN	0	—	V_{VDD55}	V	
Operating Ambient Temperature	Ta_{opr}	–40	25	105	℃	

*1: GND is the voltage of pins GND1, GND2, and GND3, which are connected inside the device. Connect these pins on the board and apply the same voltage.

*2 : The recommended operating supply range varies due to the characteristics of the external Nch BJT connected to VDD55. Use the parts described in the recommended circuit.

*3: The C_n - C_{n-1} voltage measurement accuracy is not guaranteed if input is less than 2.0 V or more than 4.3 V. Moreover, the measurement accuracy is not guaranteed unless the following conditions are fulfilled.

C2 > 2.0 V, C17 > 12 V, VBAT – C17 > –2 V, VBAT - C16 > 1 V

* Cn (n = 1 to 17) and VBAT voltage in this conditions are in reference to GND.
* Similarly for the monitoring system, replace the above condition Cn (n = 1 to 17) with CBn (n = 1 to 17).

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SUPPLY CURRENT*1							
VBAT Active Mode	I_{BAT1}		—	3.6	4.5	mA	
VBAT Low Power Mode	I_{BAT2}	INTMSEL=10 20ms intermittent mode	—	1.35	1.75	mA	*2
VBAT Standby Mode	I_{BAT3}	VDD55=Low Power, REGEXT=Low Power Coulomb Counter=off FDRV=power reduction mode INTMSEL=00 Communication=off	—	0.22	0.30	mA	
VBAT Sleep Mode	I_{BAT4}	VDD55=Low Power, REG18=Low Power, REGEXT=off, Communication=off	—	80	130	μA	
VBAT Shutdown Mode	I_{BAT5}		—	0	1	μA	
VDD55							
VDD55 Output Voltage	V_{VDD55}		5.3	5.5	5.8	V	
VDD55 Base Current1	IB_{VDD551}	High Power mode; Temp=25ºC; VBAT=62.9V	0.75	1.025	1.30	mA	
VDD55 Base Current2	IB_{VDD552}	Low Power mode; Temp=25ºC; VBAT=62.9V	0.4	0.65	0.9	mA	
REGEXT							
REGEXT Output Voltage1	V_{EXT1}	REGSEL pin=L	4.75	5	5.25	V	
REGEXT Output Voltage2	V_{EXT2}	REGSEL pin=H	3.05	3.3	3.55	V	
REGEXT Output Voltage3	V_{EXT3}	REGSEL pin=Float	2.3	2.5	2.7	V	
REGEXT Output Current1	I_{EXT1}	Normal mode	0	—	50	mA	
REGEXT Output Current2	I_{EXT2}	Low Power mode	0	—	10	mA	
REG18							
REG18 output Voltage	V_{REG18}	No load condition	1.78	1.85	1.92	V	

*1 : Current consumption is based on the following settings.
- Consumption current is measured based total current from VBAT pin (pin 14) and VDD55 pin (pin 28).
- LDM pin is HIZ condition unless specified ;All pins no load ;SEN, SCL, and SDI = Low
- Unless otherwise specified, all registers are in the default setting.
  If VDD55 and CVDD are supplying an external load, this extra current should be included additionally .

*2 : Design reference value not tested during final production inspection.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN1}	C_n - C_{n-1} (n=1～17)	0	—	5	V	*4
Voltage Resolution	V_{RES1}	14bits $V_{RES1} = 5 / 2^{14}$	-—	0.3	—	mV	*4
Voltage Accuracy1	V_{ACC_VC1}	ΔCn = 2.0V ～ 4.3 V	–5	—	5	mV	*1 to *3
Voltage Accuracy2	V_{ACC_VC2}	ΔCn = 2.0V ～ 4.3 V Ta = –30℃ ～ 75℃	–10	—	10	mV	*4
Voltage Accuracy3	V_{ACC_VC3}	ΔCn = 2.0V ～ 4.3 V Ta = –40℃ ～ 85℃	–15	—	15	mV	*4
Conversion Time	t_{conv}	time/cell	—	50	—	μs	*4
Cell Measurement Input Current	I_{IN}	Active mode	–5	—	5	μA	
Input Leakage Current	I_{LK}	Shutdown mode	–1	—	1	μA	
OVER / UNDER VOLTAGE DETECTOR (OV / UV)							
OV detection threshold step	V_{ACC_OV}	2.0～4.5V@6bit	—	50	—	mV	*4
UV detection threshold step	V_{ACC_UV}	0.5～3.0V@6bit	—	50	—	mV	*4
VPACK CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN2}		0	—	110	V	*4
Voltage Resolution	V_{RES2}	14bits	—	6.7	—	mV	*4
Voltage Accuracy1	V_{ACC_VPACK1}	V_{VPACK} = 12.5V ～ 76.5V	–1	—	1	V	*1 to *3
Voltage Accuracy2	V_{ACC_VPACK2}	V_{VPACK} = 12.5V ～ 76.5V T_a = –30℃ ～ 75℃	–1	—	1	V	*4

*1 : The C_n - C_{n-1} voltage measurement accuracy is not guaranteed if input is less than 2.0 V or more than 4.3 V. Moreover, the measurement accuracy is not guaranteed unless the following conditions are fulfilled.
C2 > 2.0 V, C17 > 12 V, VBAT – C17 > –2 V, VBAT - C16 >1 V
* Cn (n = 1 to 17) and VBAT voltage in this conditions are in reference to GND.

*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting. The value in the parenthesis is the accuracy after soldering and aging.

*3 : Measurement accuracy value including consideration of input average current and input leakage current.

*4 : Design reference value not tested during final production inspection.

*5 : Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
Cell (Monitoring) voltage resolution, $V_{RES1} = V_{IN1} / 2^{14} = 5 / 2^{14}$ = 0.3mV approx.
Vpack voltage resolution, $V_{RES2} = V_{IN2} / 2^{14} = 110 / 2^{14}$ = 6.7mV approx

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TMONI1-5 VOLTAGE MONITOR							
Input Voltage Range	V_{IN3}		0	—	5	V	*1
Voltage Resolution	V_{RES3}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_TMONI1}	VIN = 0.4V～4.7V Not use Pull-up Resistance	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_TMONI2}	VIN = 0.4V～4.7V Not use Pull-up Resistance T_a = –30℃ ～ 75℃	–10	—	10	mV	*1
Voltage Accuracy3	V_{ACC_TMONI3}	VIN = 0.4V～4.7V Not use Pull-up Resistance T_a = –40℃ ～ 85℃	–15	—	15	mV	*1
Input Pull-up Resistance	R_{PU}		7	10	13	kΩ	
Input Pull-up Resistance Temperature coefficient	RT_{PU}	T_a = –30℃ ～ 75℃ (with reference to 25℃)	–1.0	—	1.0	%	*1
GPIO1-2 VOLTAGE MONITOR							
Input Voltage Range	V_{IN4}		0	—	5	V	*1
Voltage Resolution	V_{RES4}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_GPIO1}	VIN = 0.4V～4.7V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_GPIO2}	VIN = 0.4V～4.7V T_a = –30℃ ～ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_GPIO3}	VIN = 0.4V～4.7V T_a = –40℃ ～ 85℃	–20	—	20	mV	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
TMONI voltage resolution, $V_{RES3} = V_{IN3}(Max.) / 2^{14} =$ 5 / 2^{14} = 0.3mV approx.
GPIO voltage resolution, $V_{RES4} = V_{IN4}(Max.) / 2^{14} =$ 5 / 2^{14} = 0.3mV approx.
*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.
*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VDD55 VOLTAGE MONITOR							
Input Voltage Range	V_{IN5}		0	—	7.5	V	*1
Voltage Resolution	V_{RES5}	14bits	—	0.5	—	mV	*1
Voltage Accuracy1	V_{ACC_VDD551}	VIN = 5.5V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_VDD552}	VIN = 5.5V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_VDD553}	VIN = 5.5V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1
REGEXT VOLTAGE MONITOR							
Input Voltage Range	V_{IN6}		0	—	7.5	V	*1
Voltage Resolution	V_{RES6}	14bits	—	0.5	—	mV	*1
Voltage Accuracy1	$V_{ACC\_REGEXT1}$	VIN = 5V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	$V_{ACC\_REGEXT2}$	VIN = 5V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	$V_{ACC\_REGEXT3}$	VIN = 5V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
VDD55 voltage resolution, $V_{RES5} = V_{IN5}(Max.) / 2^{14} =$ 7.5 / 2^{14} = 0.5mV approx.
REGEXT voltage resolution, $V_{RES6} = V_{IN6}(Max.) / 2^{14} =$ 7.5 / 2^{14} = 0.5mV approx.

*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.

*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VDD18 VOLTAGE MONITOR							
Input Voltage Range	V_{IN7}		0	—	5	V	*1
Voltage Resolution	V_{RES7}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_VDD181}	VIN = 1.85V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_VDD182}	VIN = 1.85V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_VDD183}	VIN = 1.85V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1
CELL BALANCING CONTROL OUTPUT (CBn)							
Output Impedance	Z_{CB}	⊿Cn = 3.0V ~ 5.0V	—	12.5	20	Ω	
THERMAL SHUTDOWN							
Shutdown Threshold	T_{SD2}	Tj	150	175	200	°C	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
VDD18 voltage resolution, $V_{RES7} = V_{IN7}(Max.) / 2^{14} = 5 / 2^{14} = 0.3mV$ approx.

*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.

*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LOW SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN8}		-180	—	180	mV	*1
Voltage Resolution	V_{RES8}	16bits	—	5.493	—	μV	
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	*2
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*1
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-25	—	25	μV	
HIGH SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN9}		-180	—	180	mV	*1
Voltage Resolution	V_{RES9}	15bits	—	10.99	—	μV	*3
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	*2 *3
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*1
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-50	—	50	μV	*3
CURRENT PROTECTION (SRP,SRN)							
Over Current in Charge Detection Accuracy1	V_{CP_OCC}	Detection Threshold 5mV & 10mV	-4	—	4	mV	*1
Over Current in Charge Detection Accuracy2	V_{CP_OCC}	Detection Threshold from 15mV to 120mV	–10	—	10	mV	
Over Current in Discharge Detection Accuracy1	V_{CP_OCD}	Detection Threshold from 10mV to 100mV	–10	—	10	mV	
Over Current in Discharge Detection Accuracy2	V_{CP_OCD}	Detection Threshold from 100mV to 320mV	–10	—	10	%	
Short Circuit in Discharge Detection Accuracy1	V_{CP_SCD}	Detection Threshold from 20mV to 100mV	–10	—	10	mV	
Short Circuit in Discharge Detection Accuracy2	V_{CP_SCD}	Detection Threshold from 100mV to 640mV	–10	—	10	%	

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
$V_{RES8} = V_{IN8}(max.) / 2^{16} = 360mV / 2^{16} = 5.493\mu V$ approx. ; $V_{RES9} = V_{IN9}(max.) / 2^{15} = 360mV / 2^{15} = 10.99\mu V$ approx.
*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.
*3 : Values are for normal measurement mode only (not in V-I sync mode)

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage “H”	V_{IH1}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL1}		0	—	V_{CVDD} ×0.2	V	
Output Voltage “H”	V_{OH1}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL1}	I_{OL} = +1mA	–0.3	—	0.4	V	
GENERAL PURPOSE HV OUTPUT (GPO)							
Output Voltage “L”	V_{HVOL1}	I_{OL} = +1mA	–0.3	—	7.0	V	
DIGITAL INPUT(1) VPC							
Input Voltage “H”	V_{IH2}		4.0	—	—	V	
Input Voltage “L”	V_{IL2}		—	—	0.3	V	
Pull-down resistance	R_{IL2}		6	28	55	MΩ	
DIGITAL INPUT(2) LDM							
Input Voltage “H”	V_{IH3}	LDM pin voltage rising for load release detection	—	2.2	2.3	V	
Input Voltage “L”	V_{IL3}	LDM pin voltage falling for load current detection	1.9	2	—	V	
Pull-Up current source 1	I_{IL3_1}	LDM pin=2V ILDM setting=50uA	30	50	70	μA	
Pull-Up current source 2	I_{IL3_2}	LDM pin=2.2V ILDM setting =400uA	200	400	600	μA	
DIGITAL INPUT(3) SHDN							
Input Voltage “H”	V_{IH4}		3.0	—	—	V	
Input Voltage “L”	V_{IL4}		—	—	0.1	V	
Pull-down resistance	R_{IL4}		200	820	1500	kΩ	

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DIGITAL INPUT(4) SDI,SCL,SEN,FETOFF							
Input Voltage “H”	V_{IH5}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL5}		0	—	V_{CVDD} ×0.2	V	
Input Leakage Current	I_{LK5}		-1	0	1	μA	
DIGITAL INPUT(5) REGSEL							
Input Voltage “H”	V_{IH6}	REGSEL pin=H For REGEXT=3.3V output settings	V_{VDD55} –0.3	—	—	V	
Input Voltage “L”	V_{IL6}	REGSEL pin=L For REGEXT=5V output settings	—	—	0.3	V	
Input Voltage Float	V_{FLT6}	REGSEL pin=Float For REGEXT=2.5V output settings	2	2.75	3.5	V	
DIGITAL OUTPUT(1) ALARM1,SDO							
Output Voltage “H”	V_{OH7}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL7}	I_{OL} = +1mA	–0.3	—	0.4	V	
DIGITAL OUTPUT(2) NRST							
Output voltage “L”	V_{OL8}	I_{OL} = 0 mA	–0.3	—	0.5	V	
Pull-up resistance	R_{IL8}	—	50	100	200	kΩ	

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
REGEXT UVLO							
UV detection voltage	V_{IL_UV1}	REGSEL pin=L	—	4	—	V	*1
UV release voltage	V_{IH_UV1}	REGSEL pin=L	—	4.2	—	V	*1
VDD55 UVLO							
UVLO detection voltage	V_{IL_UV2}		—	4.5	—	V	*1
UVLO release voltage	V_{IH_UV2}		—	4.75	—	V	*1
Nch. FET DRIVER							
Drive voltage (DIS=“H”)	V_{ON_DIS}	$V_{ON\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (CHG="H”)	V_{ON_CHG}	$V_{ON\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (DIS=“L”)	V_{OFF_DIS}	$V_{OFF\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	—	—	0.2	V	
Drive voltage (CHG=“L”)	V_{OFF_CHG}	$V_{OFF\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	—	—	0.2	V	
Rise time (DIS=“L” to ”H”)	tr	V_{DIS} = 0 to 4V C_L = 20nF	—	20	50	μs	*1
Rise time (CHG=“L” to ”H”)	tr	V_{CHG} = 0 to 4V C_L = 20nF	—	20	50	μs	*1
Fall time (DIS =“H” to ”L”)	tf	V_{DIS} = 90% to 10% C_L = 20nF	—	20	30	μs	*1
Fall time (CHG=“H” to ”L”)	tf	V_{CHG} = 90% to 10% C_L = 20nF	—	20	30	μs	*1

*1 :Design reference value not tested during final production inspection.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI Interface Timing (SEN, SDI, SCL, SDO)							
SCL Frequency	f_{SCL}	—	—	—	1	MHz	
SCL Duty Cycle	t_{DUTY}	—	45	50	55	%	
SEN Rising to SCL Rising	t_{SEN_LD}	—	100	—	—	ns	
SCL Falling to SEN Falling	t_{SEN_LG}	—	100	—	—	ns	
SEN "L" Width	t_{SEN_LO}	—	500	—	—	ns	
SDI Setup Time	t_{SDI_SU}	SDI valid to SCL falling	100	—	—	ns	
SDI Hold Time	t_{SDI_HD}	SCL falling to SDI valid	100	—	—	ns	
SDO Valid Time	t_{SDO_VD}	SCL rising to SDO valid $C_L \leqq 50$ pF	—	—	400	ns	
SDO Disable Time	t_{SDO_DIS}	SEN falling to SDO disable	—	—	400	ns	

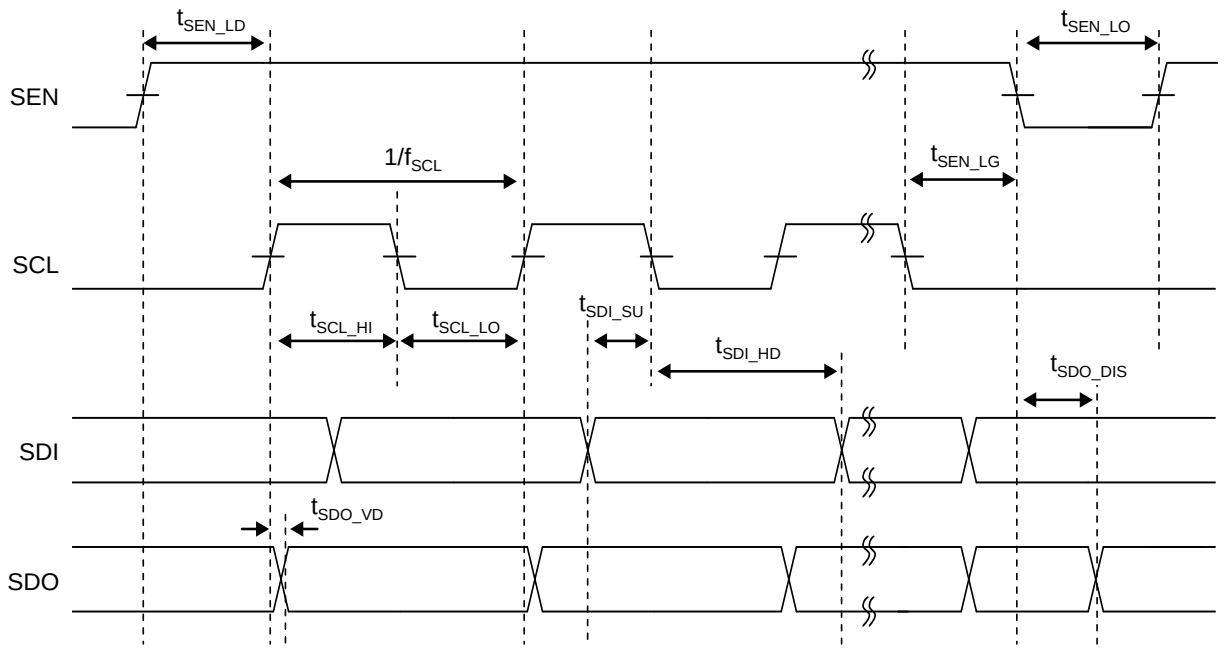
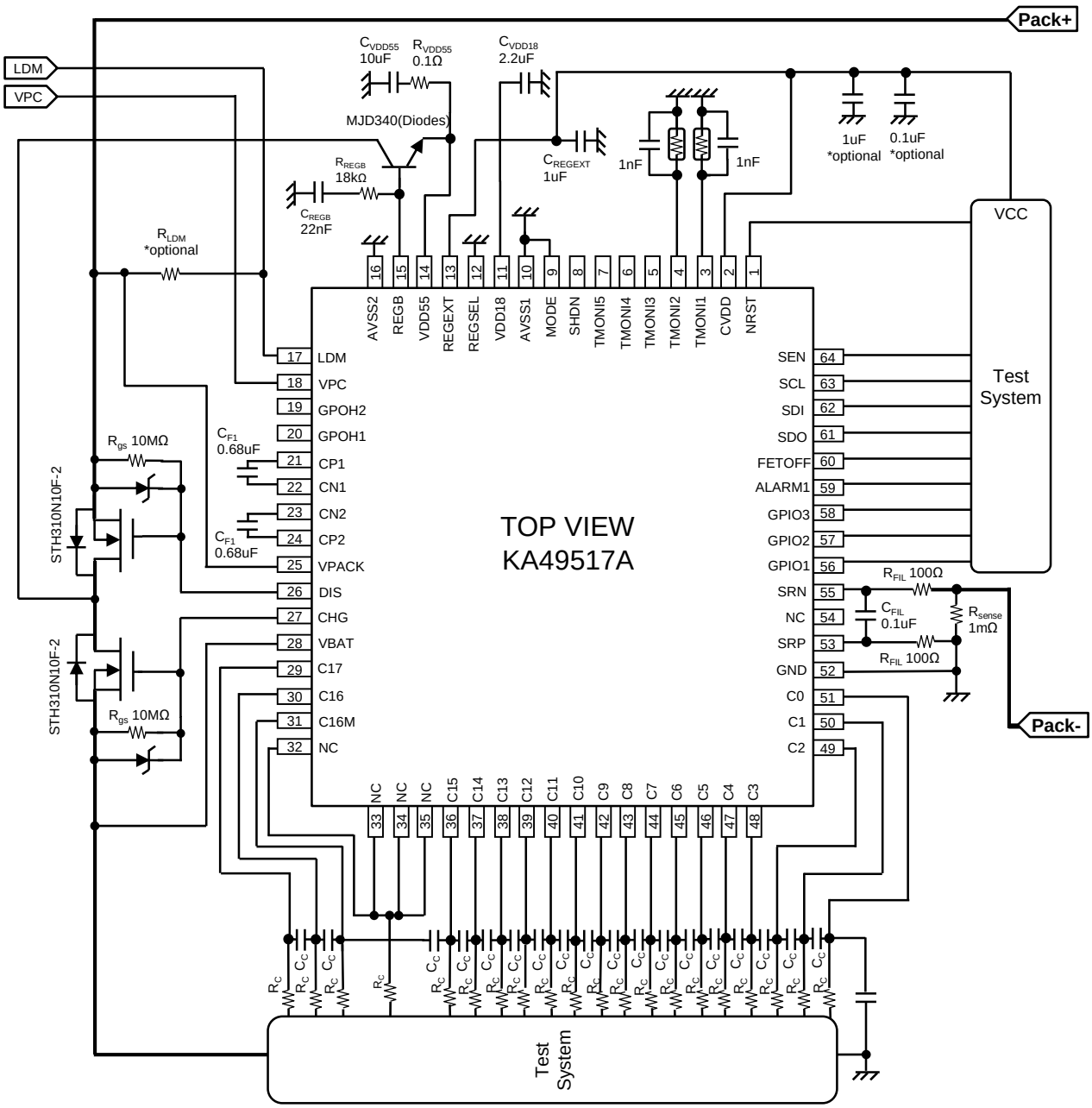


Fig.2.4.1 SPI Timing

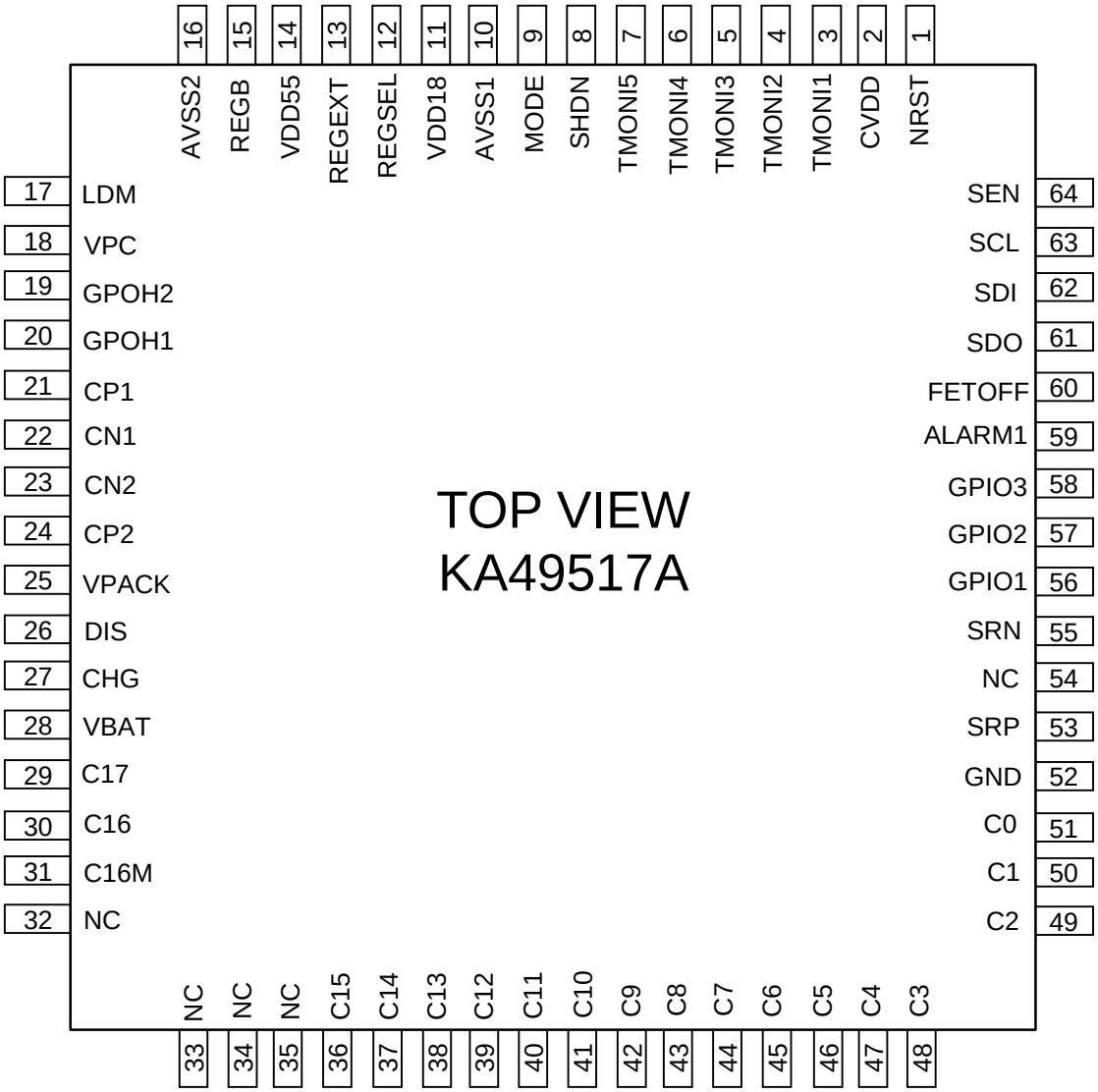
Electrical Characteristics (continued)

■Test Circuit

Electrical characteristics are tested under our recommended 17cell RC filter condition below.



*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD.
There is a requirement for the usage of REGEXT and CVDD total capacitor value.
Please refer to page 23 bottom note (*3) for more detail.


TOP VIEW
KA49517A
1 NRST
2 CVDD
3 TMONI1
4 TMONI2
5 TMONI3
6 TMONI4
7 TMONI5
8 SHDN
9 MODE
10 AVSS1
11 VDD18
12 REGSEL
13 REGEXT
14 VDD55
15 REGB
16 AVSS2
17 LDM
18 VPC
19 GPOH2
20 GPOH1
21 CP1
22 CN1
23 CN2
24 CP2
25 VPACK
26 DIS
27 CHG
28 VBAT
29 C17
30 C16
31 C16M
32 NC
33 NC
34 NC
35 NC
36 C15
37 C14
38 C13
39 C12
40 C11
41 C10
42 C9
43 C8
44 C7
45 C6
46 C5
47 C4
48 C3
49 C2
50 C1
51 C0
52 GND
53 SRP
54 NC
55 SRN
56 GPIO1
57 GPIO2
58 GPIO3
59 ALARM1
60 FETOFF
61 SDO
62 SDI
63 SCL
64 SEN

Pin Description

Pin	Pin name	Type	Description
1	NRST	O	Power Reset Output Pin（Open Drain）
2	CVDD	I (Supply)	Digital Voltage Supply
3	TMONI1	I	Analog Input Pin
4	TMONI2	I	Analog Input Pin
5	TMONI3	I	Analog Input Pin
6	TMONI4	I	Analog Input Pin
7	TMONI5	I	Analog Input Pin
8	SHDN	I	Shutdown Control “L”: Active / “H”: Shutdown
9	MODE	I	Test Mode pin for Manufacturer Use Only (Connect to DVSS always) *1
10	AVSS1	GND	Analog Ground
11	VDD18	O	1.85V LDO Output Pin for Internal Use
12	REGSEL	I	External 5V/3.3V/2.5V REGEXT output selection Pin
13	REGEXT	O	External 5V/3.3V/2.5V LDO Output Pin
14	VDD55	O	5.5V Regulator Output Pin
15	REGB	O	Base Pin for 5.5V Pre-regulator
16	AVSS2	GND	Analog Ground
17	LDM	I	Load Detect Pin
18	VPC	I	Wake Up Signal Pin - “L” Active / “H” Wake Up. Also for Charger Detect.
19	GPOH2	O	High Voltage General Purpose Output Pin 2 (Open Drain)
20	GPOH1	O	High Voltage General Purpose Output Pin 1 (Open Drain)

*1 An external pull-down resistor should be connected to MODE pin and it is internally connected to GND through a 1 kΩ resistor.

Pin Description (continued)

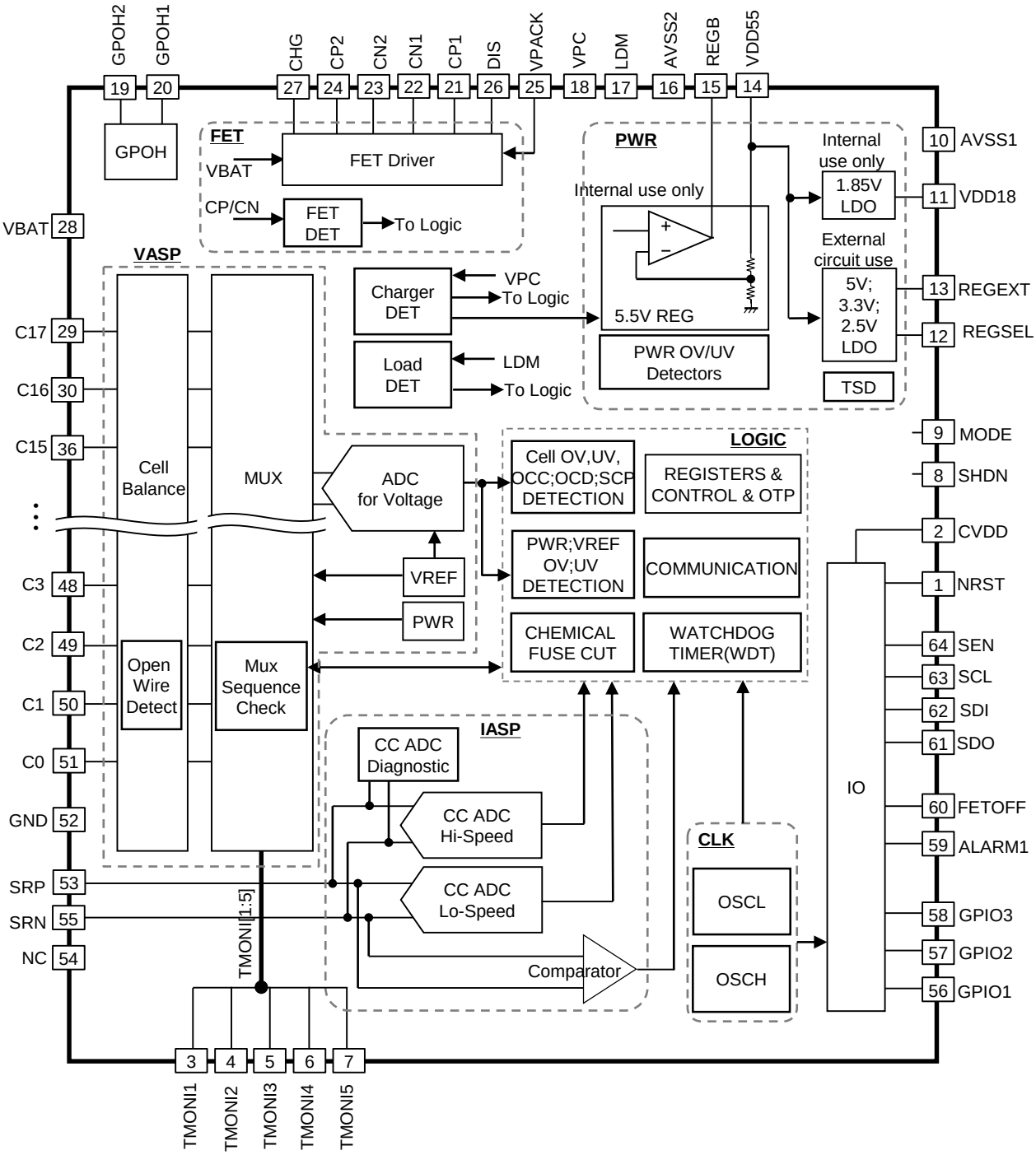
Pin	Pin name	Type	Description
21	CP1	O	Charge Pump Capacitor Pin (Positive Terminal for VPACK)
22	CN1	O	Charge Pump Capacitor Pin (Negative Terminal for VPACK)
23	CN2	O	Charge Pump Capacitor Pin (Negative Terminal for VBAT)
24	CP2	O	Charge Pump Capacitor Pin (Positive Terminal for VBAT)
25	VPACK	I (Supply)	Positive Terminal of Battery Pack to load or charger.
26	DIS	O	Discharge NMOSFET Gate Drive Pin
27	CHG	O	Charge NMOSFET Gate Drive Pin
28	VBAT	I (Supply)	Stacked Cells Highest Voltage Pin
29	C17	I	Cell 17 Input Pin (+ve)
30	C16	I	Cell 16 Input Pin (+ve) / Cell 17 Input Pin (-ve)
31	C16M	I	Cell 16 Input Pin (-ve)
32	NC	I	N.C. Pin
33	NC	I	N.C. Pin
34	NC	I	N.C. Pin
35	NC	I	N.C. Pin
36	C15	I	Cell 15 Input Pin (+ve) / Cell 16 Input Pin (-ve)
37	C14	I	Cell 14 Input Pin (+ve) / Cell 15 Input Pin (-ve)
38	C13	I	Cell 13 Input Pin (+ve) / Cell 14 Input Pin (-ve)
39	C12	I	Cell 12 Input Pin (+ve) / Cell 13 Input Pin (-ve)
40	C11	I	Cell 11 Input Pin (+ve) / Cell 12 Input Pin (-ve)

Pin Description (continued)

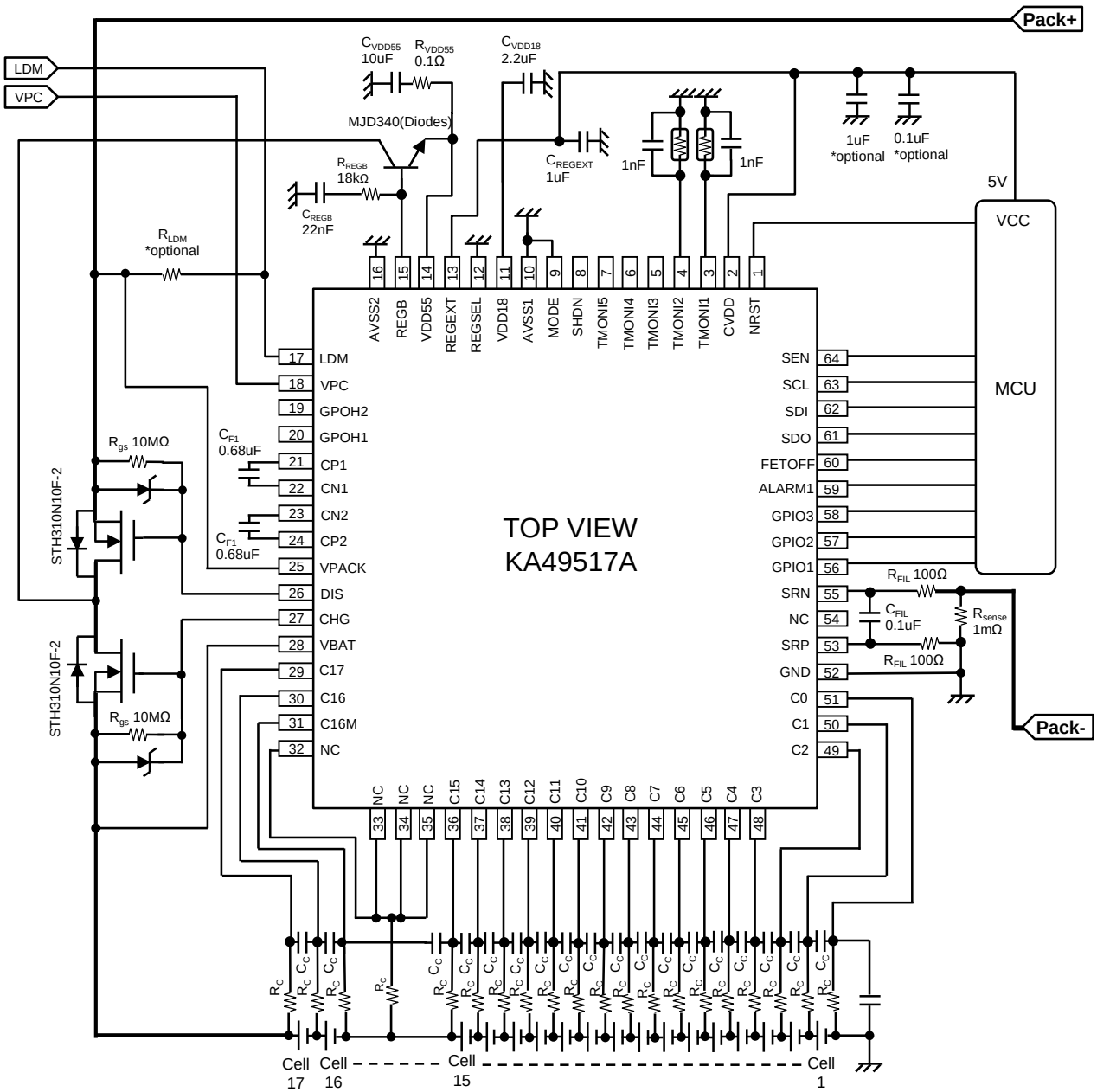
Pin	Pin name	Type	Description
41	C10	I	Cell 10 Input Pin (+ve) / Cell 11 Input Pin (-ve)
42	C9	I	Cell 9 Input Pin (+ve) / Cell 10 Input Pin (-ve)
43	C8	I	Cell 8 Input Pin (+ve) / Cell 9 Input Pin (-ve)
44	C7	I	Cell 7 Input Pin (+ve) / Cell 8 Input Pin (-ve)
45	C6	I	Cell 6 Input Pin (+ve) / Cell 7 Input Pin (-ve)
46	C5	I	Cell 5 Input Pin (+ve) / Cell 6 Input Pin (-ve)
47	C4	I	Cell 4 Input Pin (+ve) / Cell 5 Input Pin (-ve)
48	C3	I	Cell 3 Input Pin (+ve) / Cell 4 Input Pin (-ve)
49	C2	I	Cell 2 Input Pin (+ve) / Cell 3 Input Pin (-ve)
50	C1	I	Cell 1 Input Pin (+ve) / Cell 2 Input Pin (-ve)
51	C0	I	Cell 1 Input Pin (-ve)
52	GND	GND	Analog Ground
53	SRP	I	Shunt Resistor Positive Pin
54	NC	-	N.C. Pin
55	SRN	I	Shunt Resistor Negative Pin
56	GPIO1	I/O	General Purpose I/O Pin 1
57	GPIO2	I/O	General Purpose I/O Pin 2
58	GPIO3	I/O	General Purpose I/O Pin 3
59	ALARM1	O	ALARM1 Pin
60	FETOFF	I	CHG/DIS FET Control Pin - “L” Normal / “H” FET Forced OFF
61	SDO	O	SPI Interface Pin – Data Out *1
62	SDI	I	SPI Interface Pin – Data In *1
63	SCL	I	SPI Interface Pin – Clock *1
64	SEN	I	SPI Interface Pin – Enable *1

*1: An external capacitor may be required near the unused open pin to increase noise immunity.

Block Diagram



B. Application Circuit Example



*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD.
There is a requirement for the usage of REGEXT and CVDD total capacitor value.
Please refer to page 23 bottom note (*3) for more detail.

Recommended Constant of External Component

Item	Symbol	Constant				Note
		Min.	Typ.	Max.	Unit	
Constant of components connected to pins	C_{REGB}	—	22	—	nF	*1, *2
	R_{REGB}	—	18	—	kΩ	*2
	C_{VDD55}	—	10	—	μF	*1, *2
	R_{VDD55}	—	0.1	—	Ω	*2
	C_{VDD18}	—	2.2	—	μF	*1
	C_{REGEXT}	—	1	—	μF	*1,*3
	R_{GS}	—	10	—	MΩ	*2
	C_{F1}	—	0.68	—	μF	*1
	C_{F2}	—	0.68	—	μF	*1
	R_C	—	1	—	kΩ	*5
	C_C	—	1	—	μF	*1,*4
	R_{sense}	—	100	—	mΩ	*6
	R_{FIL}	—	100	—	Ω	
	C_{FIL}	—	0.1	—	μF	*1
	R_{LDM}	—	32.4	—	kΩ	*7

*1: Use of a ceramic capacitor is recommended.

*2: The parameters are applicable for system using an external NPN BJT (Diodes Inc MJD340), as shown in the recommended circuit.

*3: REGEXT can be used for as power supply for CVDD pin and external circuit. 1uF capacitor (C_{REGEXT}) is necessary at REGEXT output. It is recommended to connect a maximum of 1uF capacitor for CVDD pin and external circuit, which is compatible with default C_{VDD55} and VDD55 NPN device (Diodes Inc MJD340)

If it is necessary to increase these total capacitor value at CVDD pin and external circuit, the capacitor C_{VDD55} must be increased proportionally with about 5 times ratio to ensure stability. Please note start-up time of VDD55 and REGEXT would increase proportionally by doing this.

*4: Usage of C_n pin input filter Capacitor or Resistor of different value other than the recommended values, or, RC filter connection other than the 17 cells testing circuitry indicated in the Electrical Characteristics, will cause a shift in voltage accuracy.

*5: R_C can be selected based on the required internal MOS Cell Balance function.

It is important to maintain the current below its rated value.

*6: R_{sense} resistor design is based on actual load current needed. This value should not cause SRP and SRN pin to generate voltage out of the sensing range which will affect measurement accuracy.

*7: R_{LDM} allow user to adjust Load detector threshold based on system requirement.
By using R_{LDM} of 32.4k, it is possible to detect LDM threshold of 0.4V when load current of minimum 70uA is drawn at the pin in the case FET is open case.

Description of Functions

1. Battery Connection

The minimum required VBAT pin voltage is 12.5V to guarantee normal operation.

For application using less than 17 cells, all unused cells Cn pins should be connected as shown in figure below, user shall use cells connect to C17, C16, C1 and C2 pins first and followed by battery from lower cell. Please also note that although pin 32 ~ pin 35 are NC pins, they are to be connected as shown in the diagram below to ensure the best measurement performance of other cell pins

Battery cells connection sequence:

Connect the GND pin followed by VBAT pin. After that, it should be connected from the lower cell in turn.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → incrementally

Figures below are some system example. Minimum VBAT for 4 cells system must be higher than 12.5V.

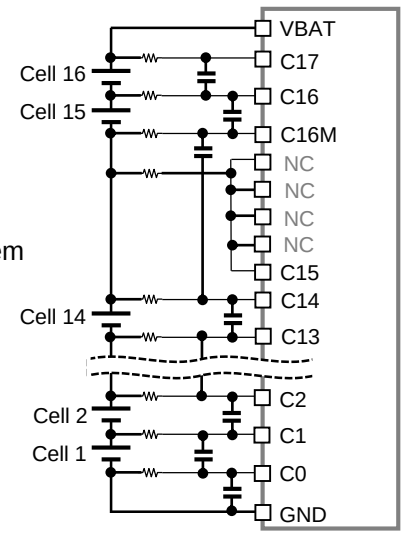


Fig.1.1.1
Example of
16 Cell System

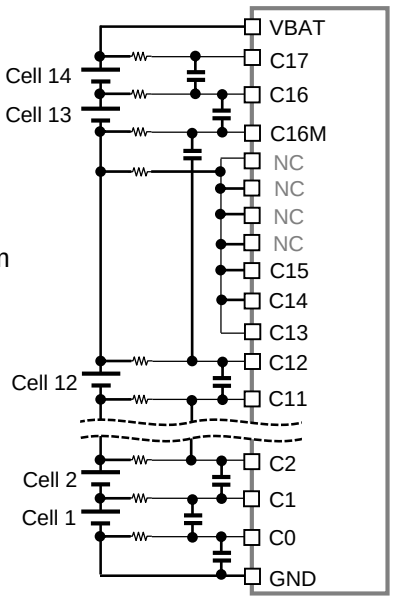


Fig.1.1.2
Example of
14 Cell System

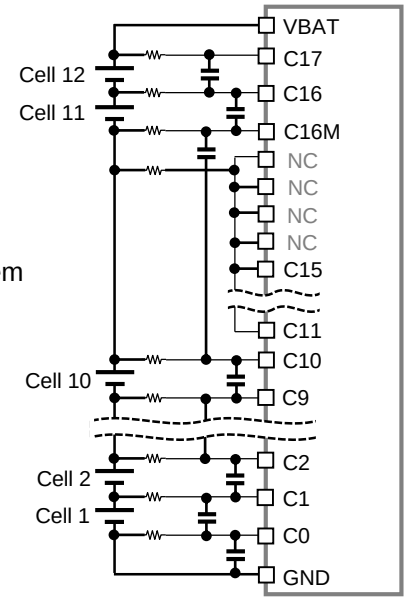


Fig.1.1.3
Example of
12 Cell System

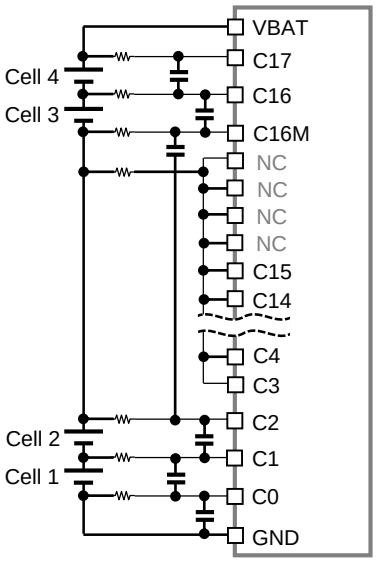
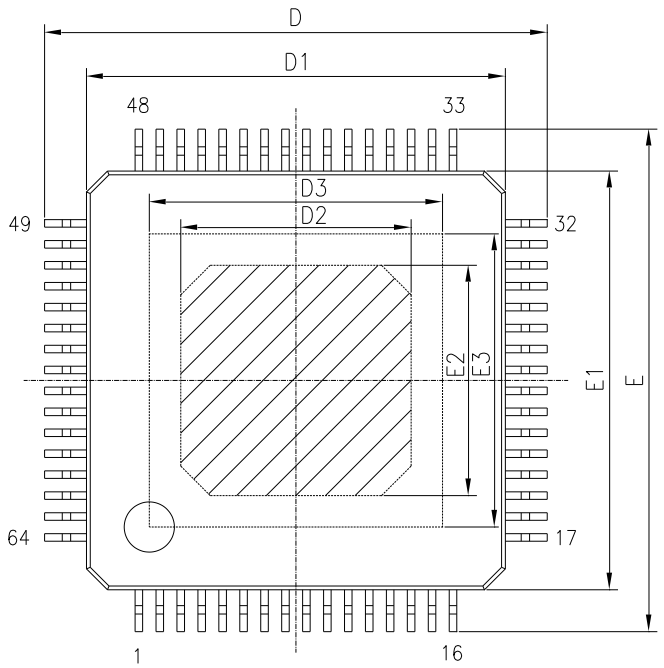


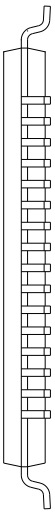
Fig.1.1.4
Example of
4 Cell System

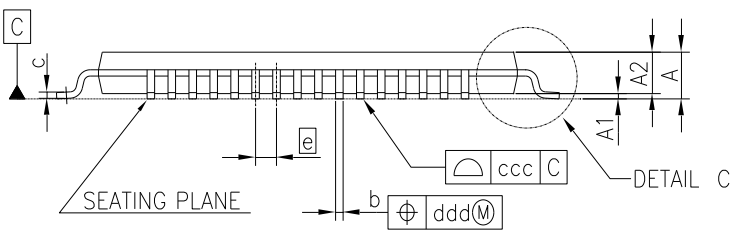
Dimensions

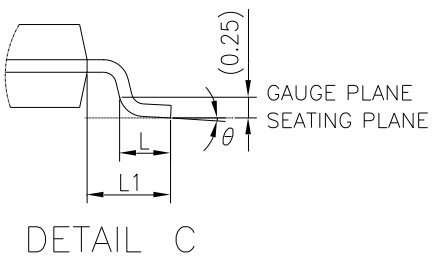
• TQFP 64L 10x10mm², Thickness 1mm, Lead Pitch 0.5mm, Lead Length 1mm, EP Size 5.5x5.5mm

Unit: mm









DETAIL C

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	0.10	0.20
A2		1.00REF	
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
D2	5.50	–	–
D3	–	–	7.00
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
E2	5.50	–	–
E3	–	–	7.00
L	0.45	0.60	0.75
L1		1.00REF	
b	0.15	0.20	0.25
c	0.10	0.15	0.20
e		0.50BSC	
ddd		0.10	
ccc		0.10	
θ	0.0°	–	8.0°

Usage Notes

1. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
2. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
3. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
4. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin - VBAT short, output pin – CVDD fault (Power supply fault), output pin-GND short (Ground fault), output-to-output-pin short (load short), or leakage current between pins. Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
5. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VBAT short, output pin to CVDD short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
6. Verify the risks which might be caused by the malfunctions of external components.

Revision History

Control Number Rev 1.00

Date	Page	Item	Before	After
25 Dec 2020	—	Initial Release	—	—

Control Number Rev 1.01

Date	Page	Item	Before	After
Jan Feb 2021	16,22	Bottom note		Added note *1
	23	Bottom note *3 updated		REGEXT can be used for as power supply for CVDD pin and external circuit. 1uF capacitor (CREGEXT) is necessary at REGEXT output. It is recommended to connect a maximum of 1uF capacitor for CVDD pin and external circuit, which is compatible with default CVDD55 and VDD55 NPN device (Diodes Inc MJD340) If it is necessary to increase these total capacitor value, the capacitor CVDD55 must be increased proportionally with about 5 times ratio to ensure stability. Please note start-up time of VDD55 and REGEXT would increase proportionally by doing this.
	6	Specs for I_{BAT5}	Min: 0uA Typ: -- Max: 1uA	Min: -- Typ: 0uA Max: 1uA
	7	Specs for V_{ACC_VC1} Added voltage accuracy room temp value	--	Added +-5mV specs

Control Number Rev 1.03

Date	Page	Item	Before	After
31 May 2021	6 ~ 15	Added Ambient Temp Ta value in the header portion	--	T_a = 25℃±2℃
	5	Power dissipation rating	38.6 'C/W	37.7 'C/W
30 June 2021	16,22		*1: There is a requirement for the usage of REGEXT and CVDD total capacitor value. Please refer to page 23 bottom note (*3) for more detail.	*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD. There is a requirement for the usage of REGEXT and CVDD total capacitor value. Please refer to page 23 bottom note (*3) for more detail.

Control Number Rev 1.05

Date	Page	Item	Before	After
21 September 2021	-	Document name	Product Standards	Product Brief

Control Number Rev 1.06

Date	Page	Item	Before	After
26 Jan 2022	-	Add important notice	--	1. Changed important notice on page2 2. Added usage notes on page27

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.