aP4890U --- 2.7 Watt Audio Power Amplifier

■ FEATURES

- 2.7W Into 4Ω from 5.0V power supply at THD+N = 10% (Typ.).
- 1.7W Into 8Ω from 5.0V power supply at THD+N = 10% (Typ.)
- 2.0V~5.5V Power supply. Low shutdown current.(TYP.=0.05uA)
- Low quiescent current.(TYP.=3.0mA) Thermal shutdown protection with auto recovery feature. „
- Advanced power ON/OFF pop reduction. „
- Lead free and green package available. (RoHS Compliant) „
- Space Saving Package
  -- 8-pin MSOP package. (without thermal pad)
  --- SOP8 package

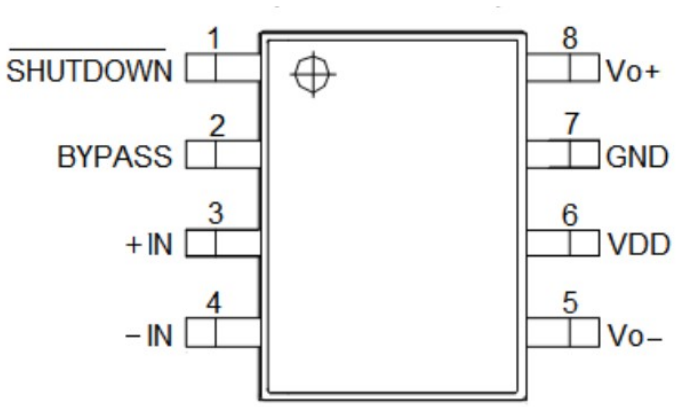
■ APPLICATION

- „ Boom Box.
- „ Education, Toy.
- „ MID,
- „ Portable electronic devices.
- „ Mobile Phones.

■ GENERAL DESCRIPTION

The AP4890U is a 2.7W audio power amplifier. It is capable of driving 4Ω speaker load at a continuous average output of 2.7W with less than 10% distortion (THD+N) from a 5.0V power supply and 8Ω speaker load at a continuous average output of 1.7W with less than 10% distortion (THD+N) from a 5.0V power supply. The AP4890U primarily designed for high quality application in other portable communication device. And the AP4890U audio amplifier features low power consumption shutdown mode. It is achieved by driving the shutdown pin with logic low. And the AP4890U has an internal thermal shutdown protection feature. The AP4890U audio amplifier was designed specifically to provide high quality output power with a minimal amount of external components.
The AP4890U does not require output capacitors, and the AP4890U is ideally suited for other low voltage applications or portable electronic devices where minimal power consumption is a primary requirement.

■ PIN CONFIGURATION



SYMBOL	Pin No.	DESCRIPTION
SHUTDOWN	1	Shutdown the device. (when LOW level is shutdown mode)
BYPASS	2	Bypass pin
+IN	3	Positive Input
-IN	4	Negative Input
Vo1(-)	5	Negative output
VDD	6	Power Supply
GND	7	Ground
Vo2(+)	8	Positive Output

■ APPLICATION CIRCUIT

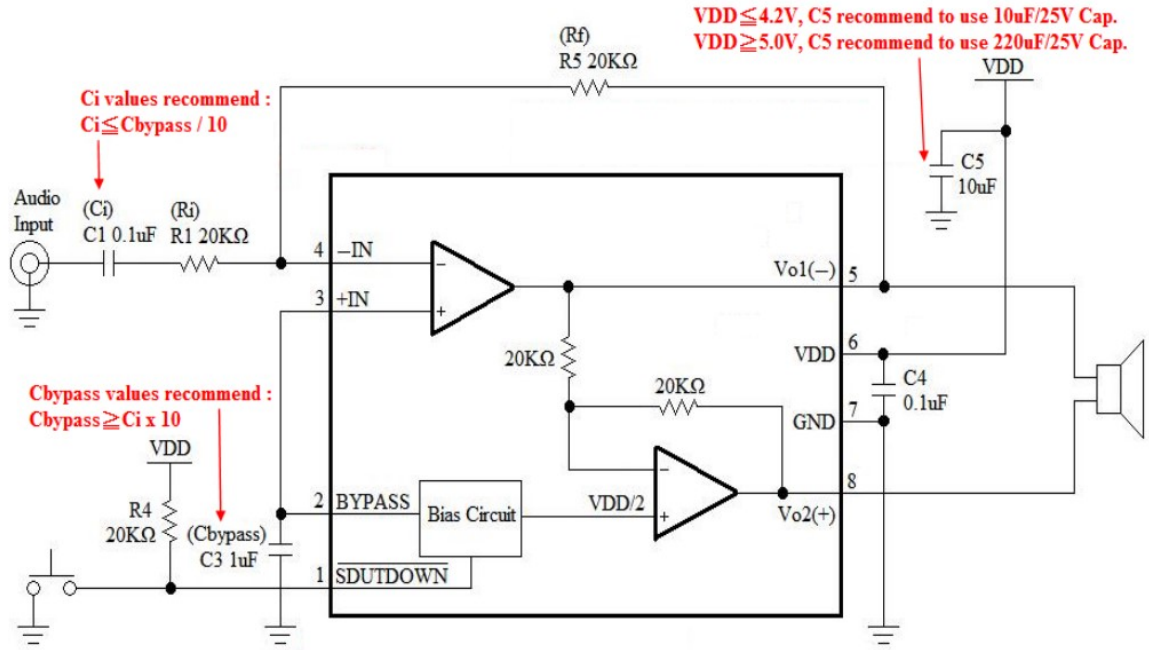


Figure 1. application schematic with Single –Ended input

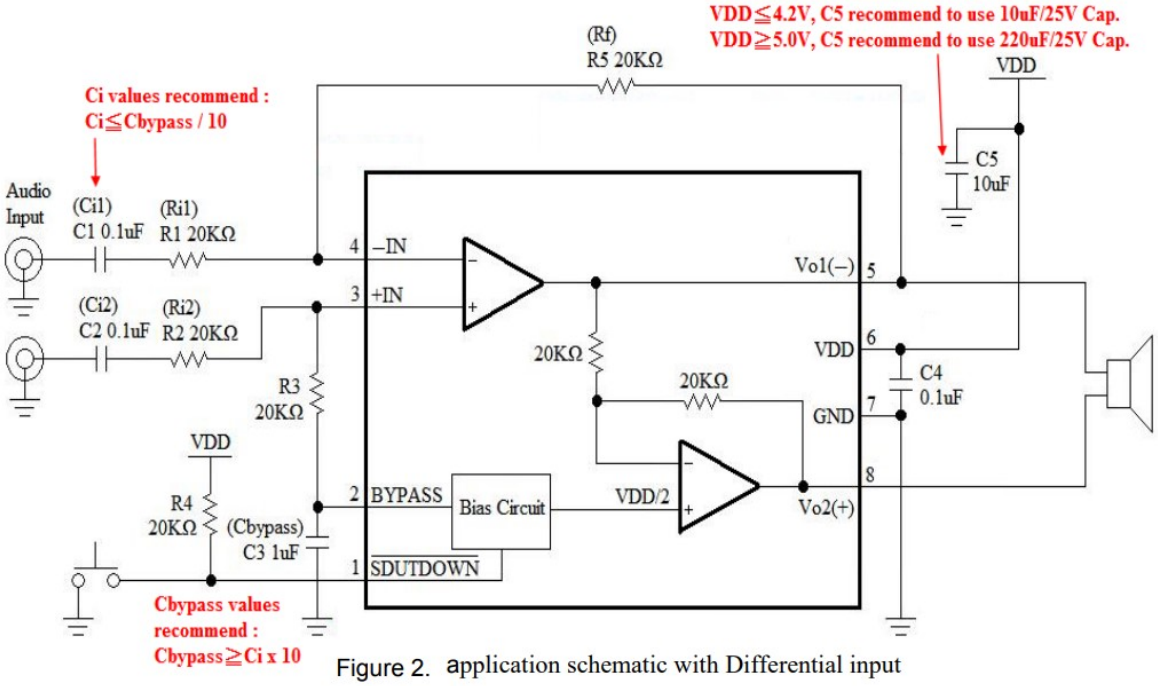


Figure 2. application schematic with Differential input

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	6.0	V
Operating Temperature	TA	-40 to 85 (I grade)	℃
Input Voltage	VI	-0.3V to VDD +0.3V	V
Storage Temperature	TSTG	-65 to 150	℃
Power Dissipation	PD	Internally Limited	W
ESD Susceptibility	VESD	2000	V
Junction Temperature	TJMAX	150	℃
Soldering Temperature (under 10 sec)	TSOLDER	260	℃

■ DC ELECTRICAL CHARACTERISTICS (TA=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX	UN
Power supply voltage	VDD	---	2.0	-	5.5	V
Quiescent Current	IQ	VDD=5.0V, Load=4Ω	-	3.0	9.0	mA
Shutdown Current	ISD	VDD=5.0V, VSD=0V		0.05	2.0	μA
Shutdown Voltage Input High	VSDIH	VDD=5.0V, VSD Mode = VDD	1.2	-	-	V
Shutdown Voltage Input Low	VSDIL	VDD=5.0V, VSD Mode = GND	-	-	0.4	V
Output Offset Voltage	VOS	VDD=5.0V, Load=4Ω	-	7.0	50.0	mV

PS : Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and TA = 25℃

■ OPERATING CHARACTERISTICS(1) (TA=25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UN
Power Supply Rejection Ratio	PSRR	Vripple = 200mV sine p-p, VDD=5.0V, RL=4Ω, Av=2. Input=GND.	1KHz	-	68.77	-	dB
			217Hz	-	55.60	-	
		Vripple = 200mV sine p-p, VDD=5.0V, RL=4Ω, Av=2. Input=Floating.	1KHz	-	68.31	-	
			217Hz	-	67.73	-	
Signal-to-noise ratio	SNR	VDD=5.0V,Av=2, f=20Hz~20KHz, Input=GND, RL=4Ω SPK,	A-weighting	-	38.7	-	uV
			None A-weighting	-	51.5	-	
Thermal shutdown temperature	TSD	Shutdown temp.		-	160	-	℃
		Restore temp.		-	**130**	-	

PS : Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VCC = VCC(TYP.) and TA = 25℃

▪ OPERATING CHARACTERISTICS(2) (TA=25℃)

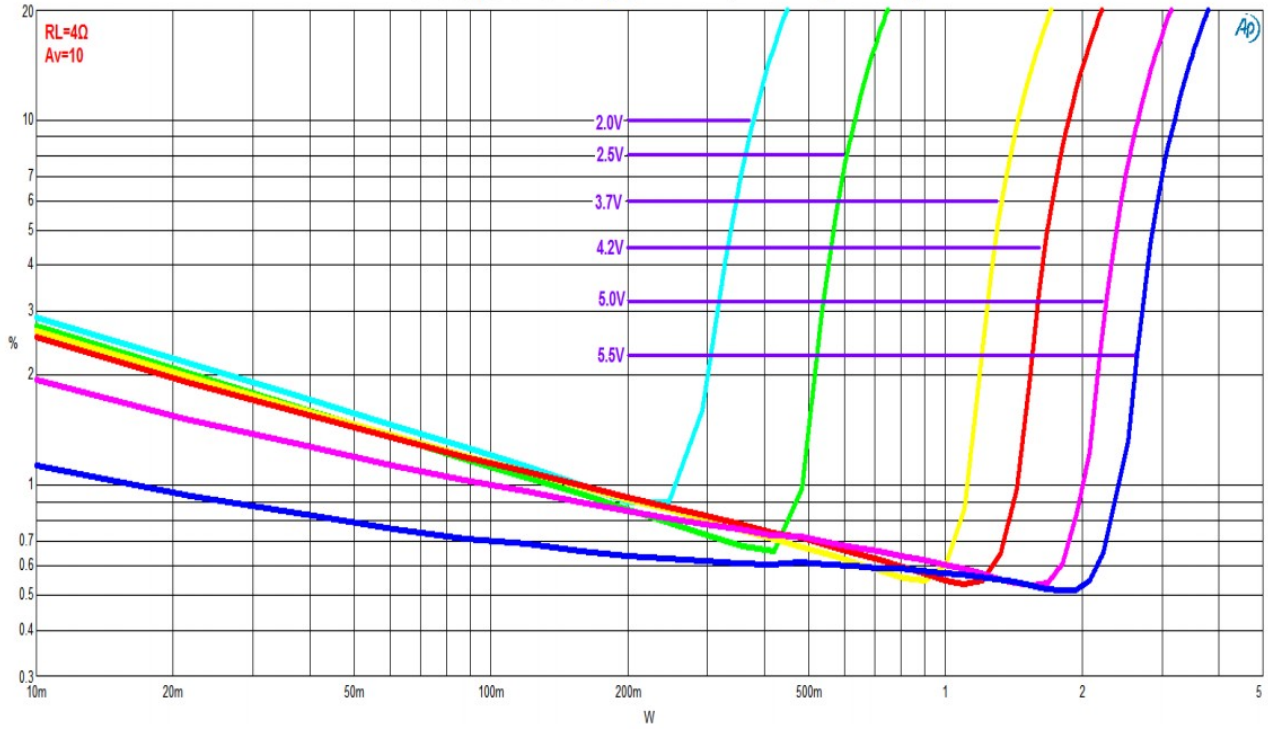
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UN
Output Power	Po	RL=4Ω THD=10%,f=1 kHz PS1	VDD=5.5V	-	3.3	-	
			VDD=5.0V	-	2.7	-	
			VDD=3.7V	-	1.5	-	
			VDD=2.5V	-	0.6	-	
			VDD=2.0V	-	0.37	-	
		RL=4Ω THD=1%,f=1 kHz PS2	VDD=5.5V	-	2.5	-	
			VDD=5.0V	-	2.0	-	
			VDD=3.7V	-	1.1	-	
			VDD=2.5V	-	0.5	-	
			VDD=2.0V	-	0.24	-	
		RL=8Ω THD=10%,f=1 kHz	VDD=5.5V	-	2.0	-	
			VDD=5.0V	-	1.7	-	
			VDD=3.7V	-	1.0	-	
			VDD=2.5V	-	0.4	-	
			VDD=2.0V	-	0.25	-	
		RL=8Ω THD=1%,f=1 kHz	VDD=5.5V	-	1.6	-	
			VDD=5.0V	-	1.3	-	
			VDD=3.7V	-	0.7	-	
			VDD=2.5V	-	0.3	-	
			VDD=2.0V	-	0.2	-	

PS1 : Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and TA = 25℃

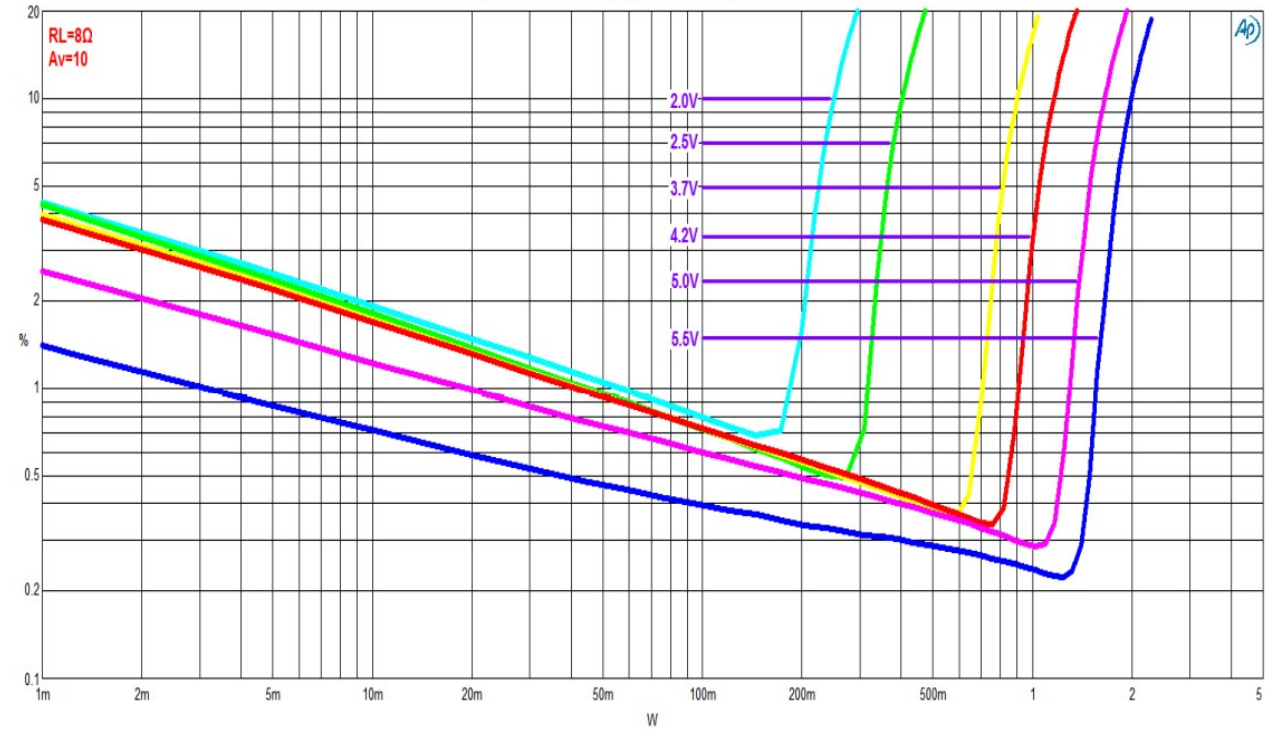
PS2 : When driving 4Ω loads from 4.2V~5V power supply, the device must be mounted to a circuit board.

- ***TYPICAL PERFORMANCE CHARACTERISTIC***

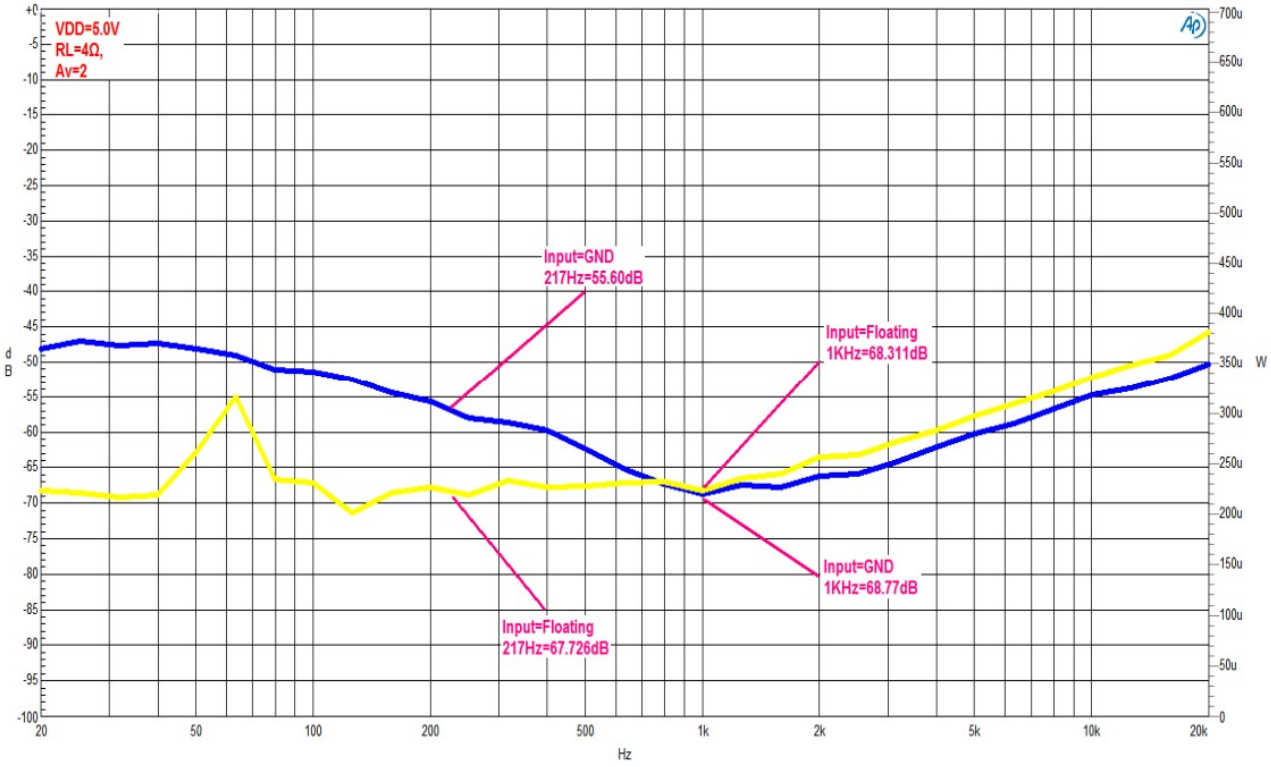
THD+N vs. Output Power (@ RL=4Ω, f=1kHz, AV=10)



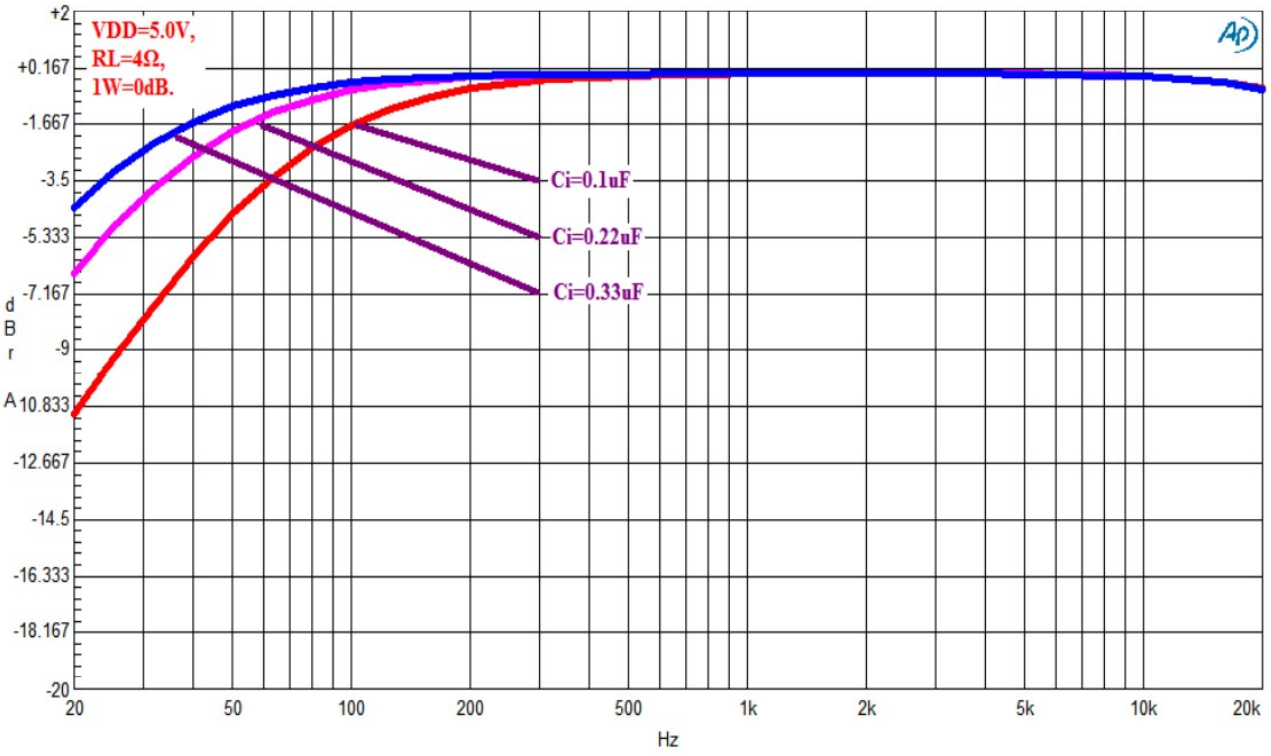
THD+N vs. Output Power (@ RL=8Ω, f=1kHz, AV=10)



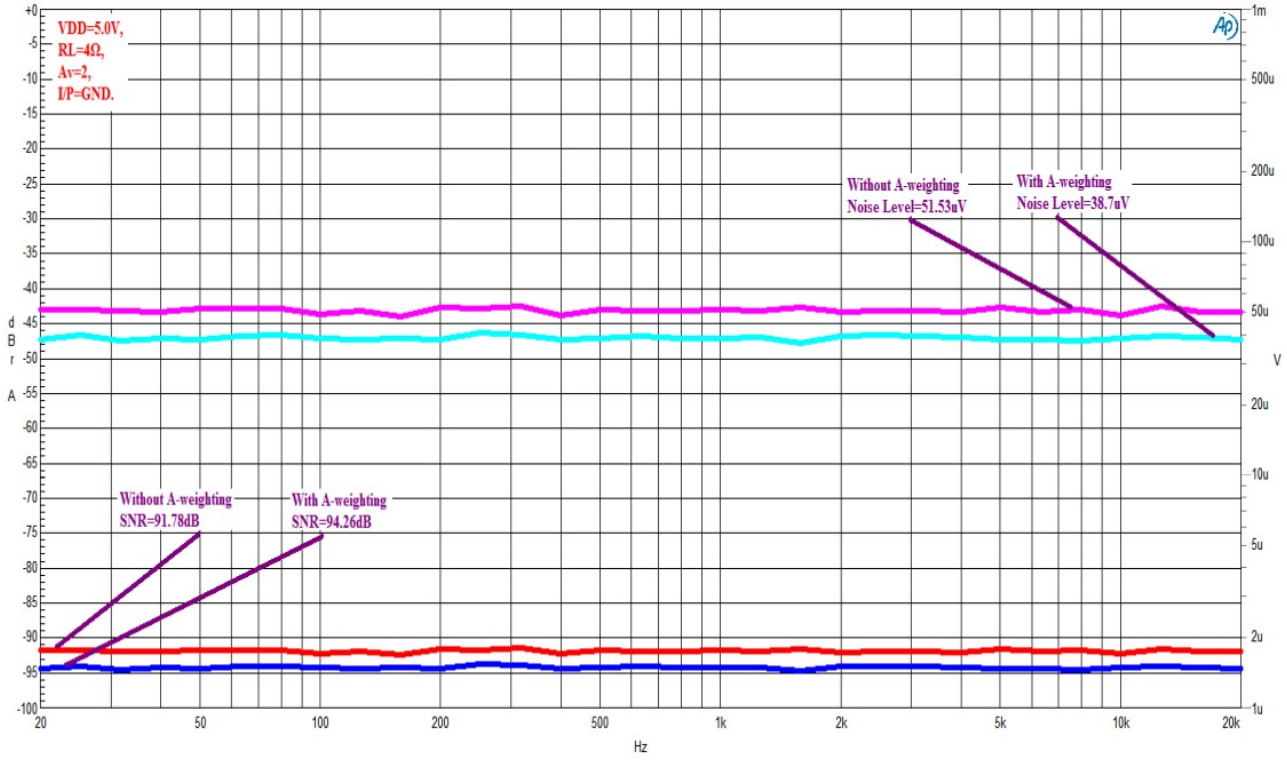
Power Supply Rejection Ratio (PSRR)



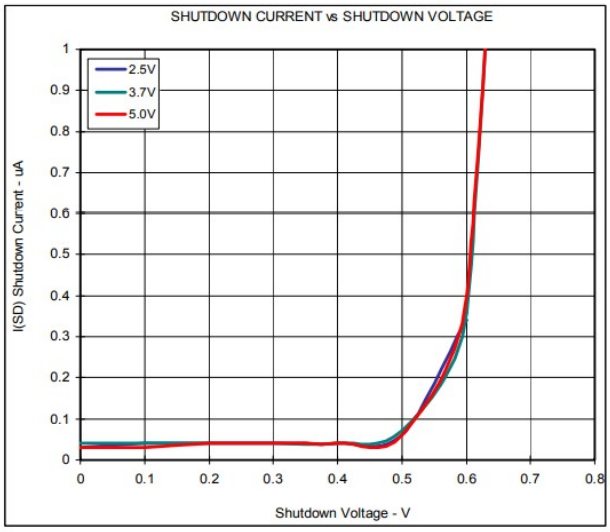
Frequency response



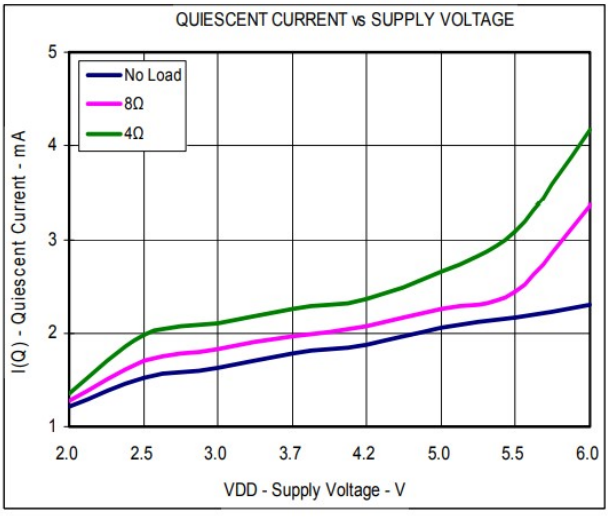
SNR vs. Noise Level



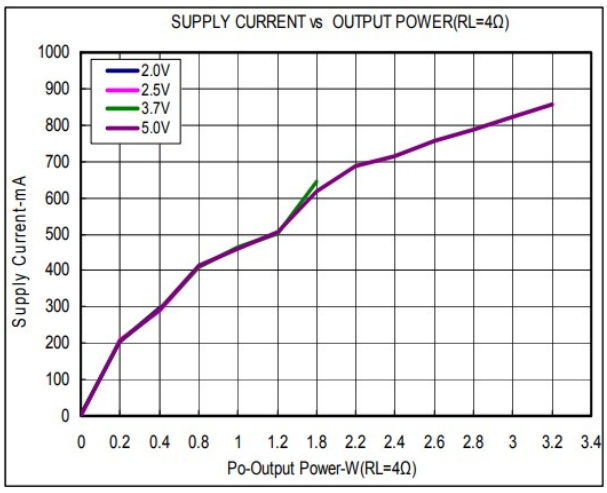
SD Current vs. SD Voltage



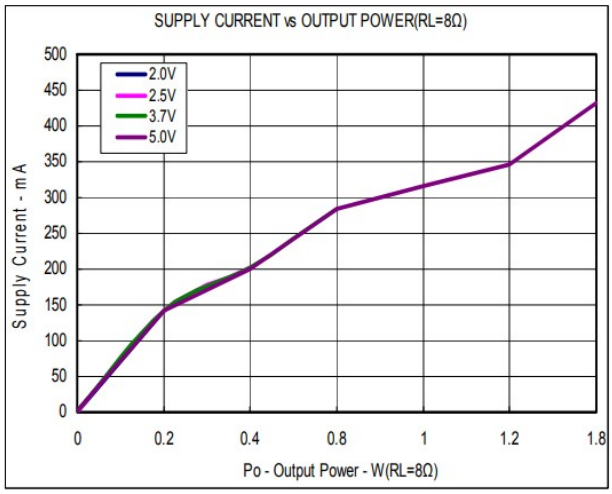
Quiescent Current vs. Supply voltage



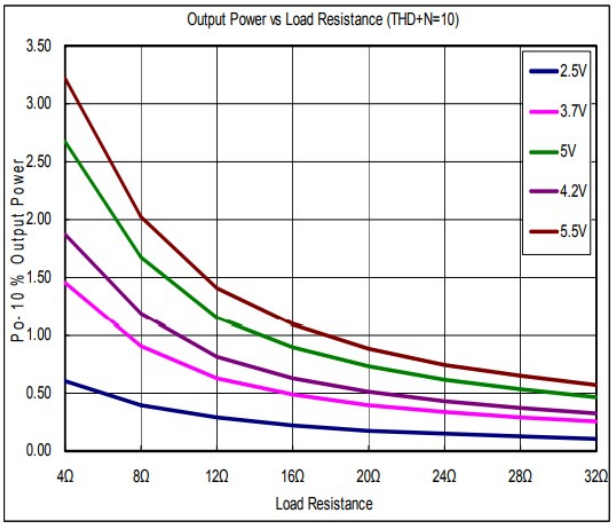
V_{DD} Current vs. Output Power (R_L=4Ω)



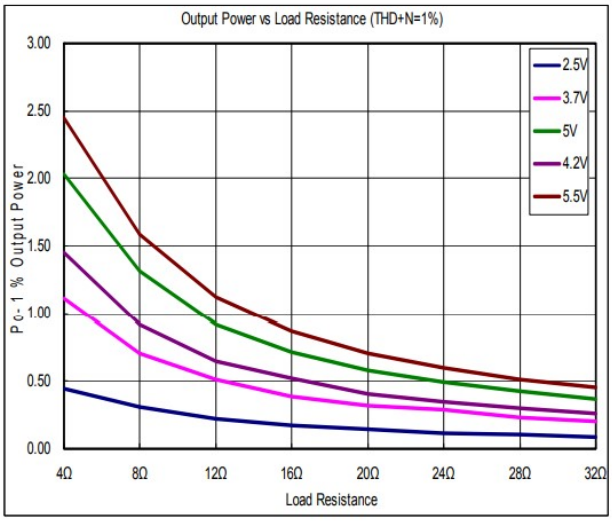
V_{DD} Current vs. Output Power (R_L=8Ω)



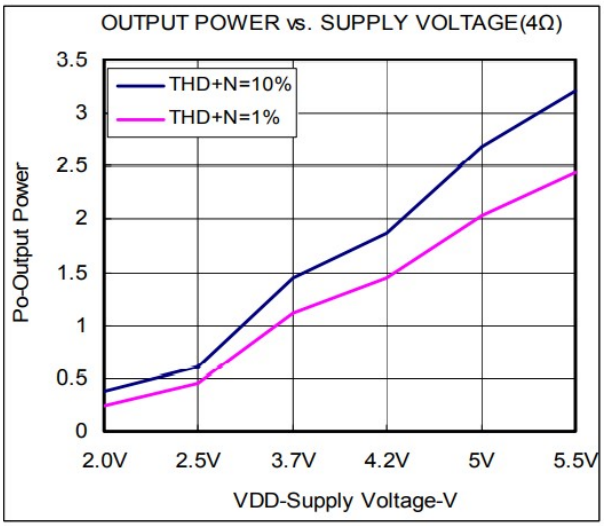
Load Resistance vs. Output Power (THD+N=10%)



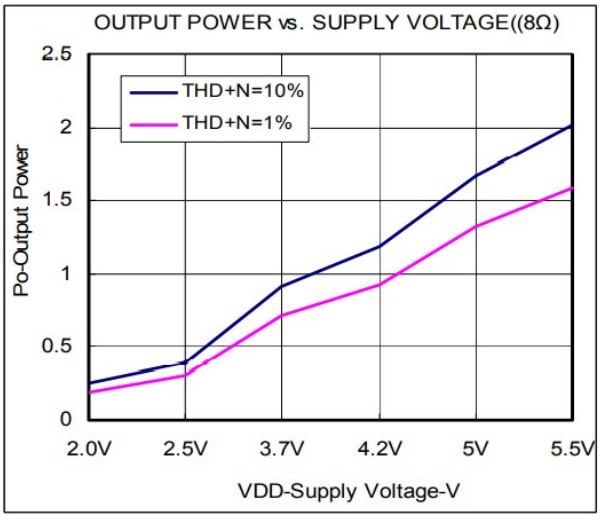
Load Resistance vs. Output Power (THD+N=1%)



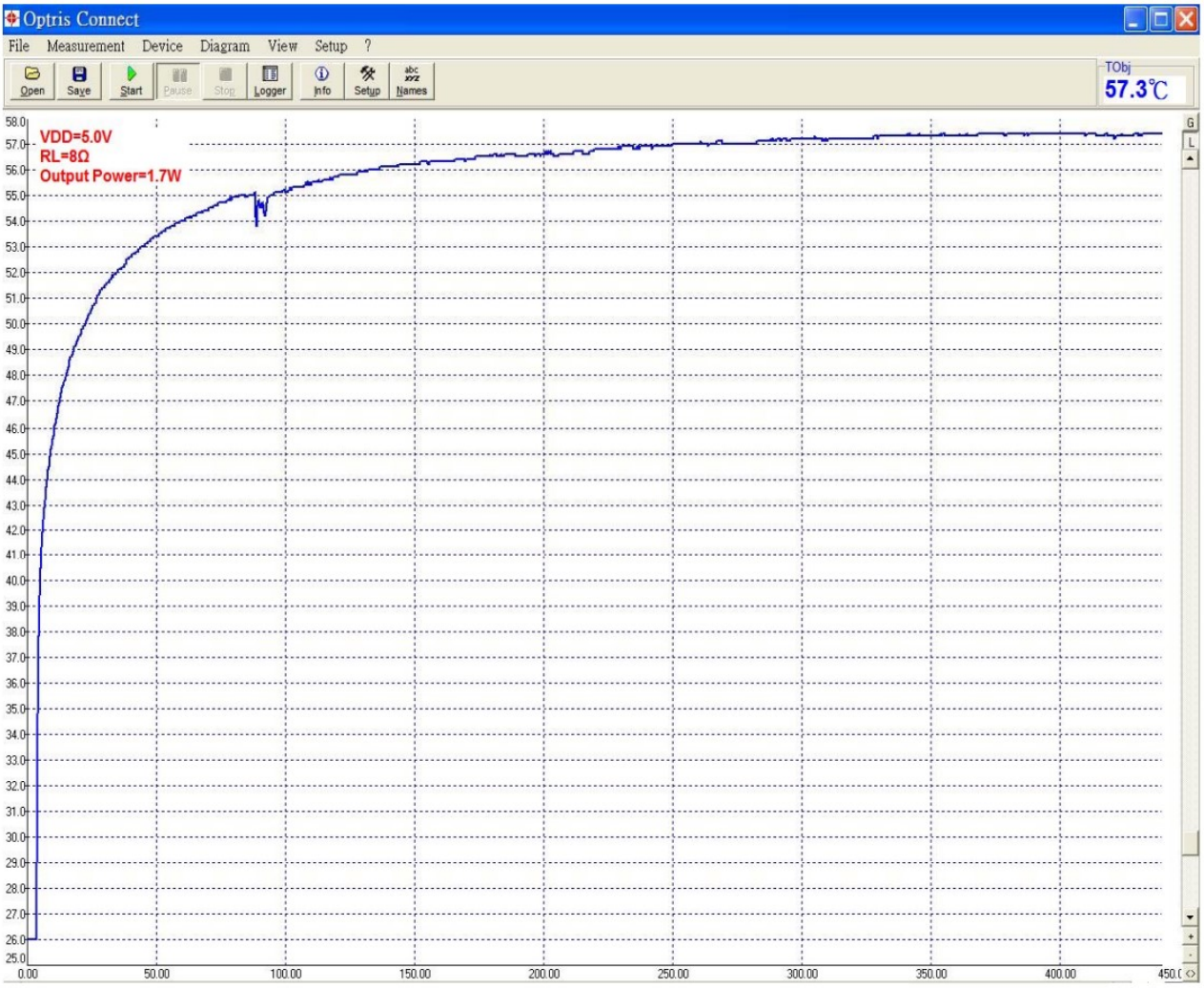
V_{DD} vs. Output Power (R_L=4Ω)



V_{DD} vs. Output Power (R_L=8Ω)



Output Power vs. Temperature



- ***APPLICATION INFORMATION***

- ***Bridged configuration explanation***

As shown in Figure 1 and 2, the AP4890U has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to RIN while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 and 2 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$AVD = 2 \times (Rf / RIN) \quad \text{.....(1)}$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.
A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a pecified supply voltage.
Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section. A bridge configuration, such as the one used in the AP4890U, also creates a second advantage over Single -ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load.
This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

- ***Input Capacitors (Ci)***

The AP4890U input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation Equation 2.

$$fc = 1 / 2\pi RiCi \quad \text{.....(2)}$$

Equation 3 is reconfigured to solve for the input coupling capacitance.

$$Ci = 1 / 2\pi Rifc \quad \text{.....(3)}$$

For example

In the table 1 shows the external components.
Rin in connect with Cin to create a high-pass filter.

Table 1. Typical Component Values

Reference	Description				Note
Ri	20KΩ				1% tolerance resi
Ci	0.1uF	0.22uF	0.33uF	0.47uF	80%/–20% non polarized
corner frequency	79.57Hz	36.17Hz	20.4Hz	16.93Hz	

$$Ci = 1 / (2\pi Rifc)$$

$$Ci = 1 / (2\pi \times 20K\Omega \times 20Hz)=0.1uF$$

One would likely choose a value of 0.1uF as this value is commonly used.
Note that it is important to Ci must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing Ci for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$Ci \leqq Cbypass / 10$$

- ***Bypass Capacitor Value Selection***

Besides minimizing the input capacitor size, careful consideration should be paid to value of Cbypass, the capacitor connected to the BYPASS pin. Since Cbypass determines how fast the AP4890U settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the AP4890U's outputs ramp to their quiescent DC voltage (nominally 1/2 VDD),
the smaller the turn-on pop. Choosing Cbypass value equal 1.0 to 10 uF along with a small value of Ci (in the range of 1 nF to 0.39 µF), produces a click-less and pop-less shutdown function. As discussed above, choosing Ci no larger than necessary for the desired bandwith helps minimize clicks and pops. Therefore, increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, Cbypass should be 10 times larger than Ci.

$$Cbypass \geqq Ci \times 10$$

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UN
Start-up time from shutdown	ZI	VDD=5.0V, Ci=0.1uF, Ri=20KΩ, Av=10	Cbypass = 10μf	-	940	-	ms
			Cbypass = 4.7μf	-	550	-	
			Cbypass = 2.2μf	-	190	-	
			Cbypass = 1.0μf	-	158	-	
		VDD=3.7V, Ci=0.1uF, Ri=20KΩ, Av=10	Cbypass = 10μf		780		
			Cbypass = 4.7μf		480		
			Cbypass = 2.2μf		180		
			Cbypass = 1.0μf		126		

■ Power Supply Bypassing Capacitor

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible.
The AP4890U is a mono class AB audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance ceramic capacitor or electrolytic capacitors, typically 10~220uF, placed as close as possible to the device VDD lead works best. Placing 0.1uF decoupling capacitor close to the AP4890U is very important for the efficiency of the class AB amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency and protect device damage.
For filtering lower-frequency noise signals, a 10.0uF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

■ *Shutdown Function*

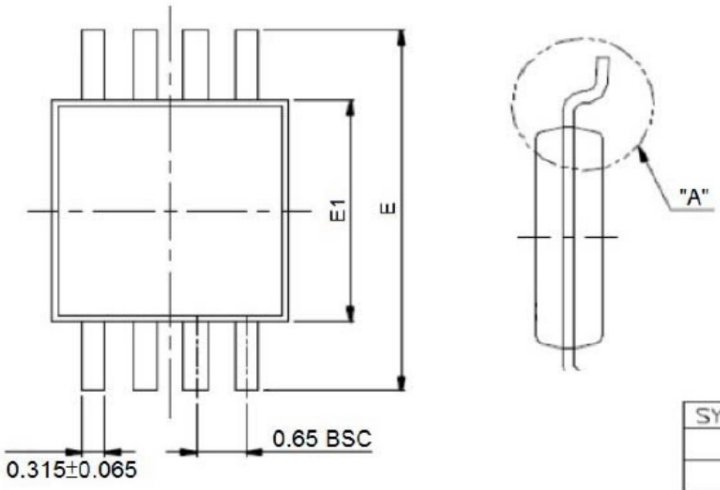
When the AP4890U not in use. The device will be to turn off the amplifier to reduce power consumption. When logic low is applied to the shutdown pin, this shutdown feature will turns the amplifier off. By switching the shutdown pin connected to GND, the device supply current draw will be minimized in idle mode. The pin cannot be left floating due to the internal did not pull-up. Over-Heat Protection
The AP4890U has a built-in over-heat protection circuit , it will turn off all power output when the Chip temperature over 160℃, the chip will return to normal operation automatically after the temperature cool down to 130℃.

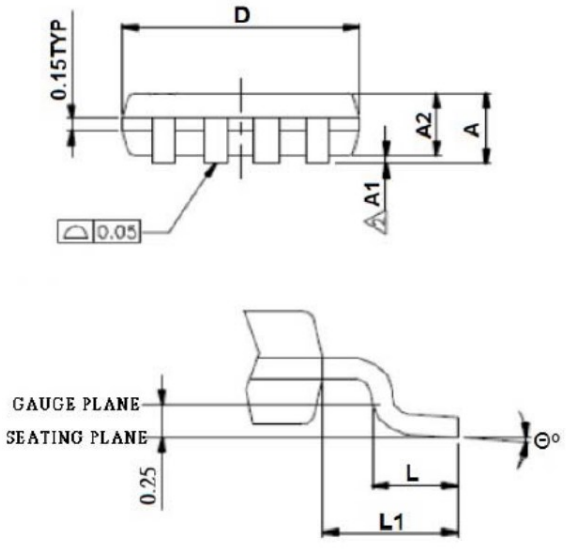
■ *PCB LAYOUT*

All the external components must place very close to the AP4890U. The input resistors need to be very close to the AP4890U input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the AP4890U. Then place the decoupling capacitor Cs, close to the AP4890U is important for the efficiency of the class AB amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. Making the high current traces going to VDD, GND, VO+ and VO- pins of the AP4890U should be as wide as possible to minimize trace resistance. If these traces are too thin, the AP4890U's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

■ PACKAGE OUTLINE DIMENSION

▪ MSOP8 (118mil) Package Outline Dimension



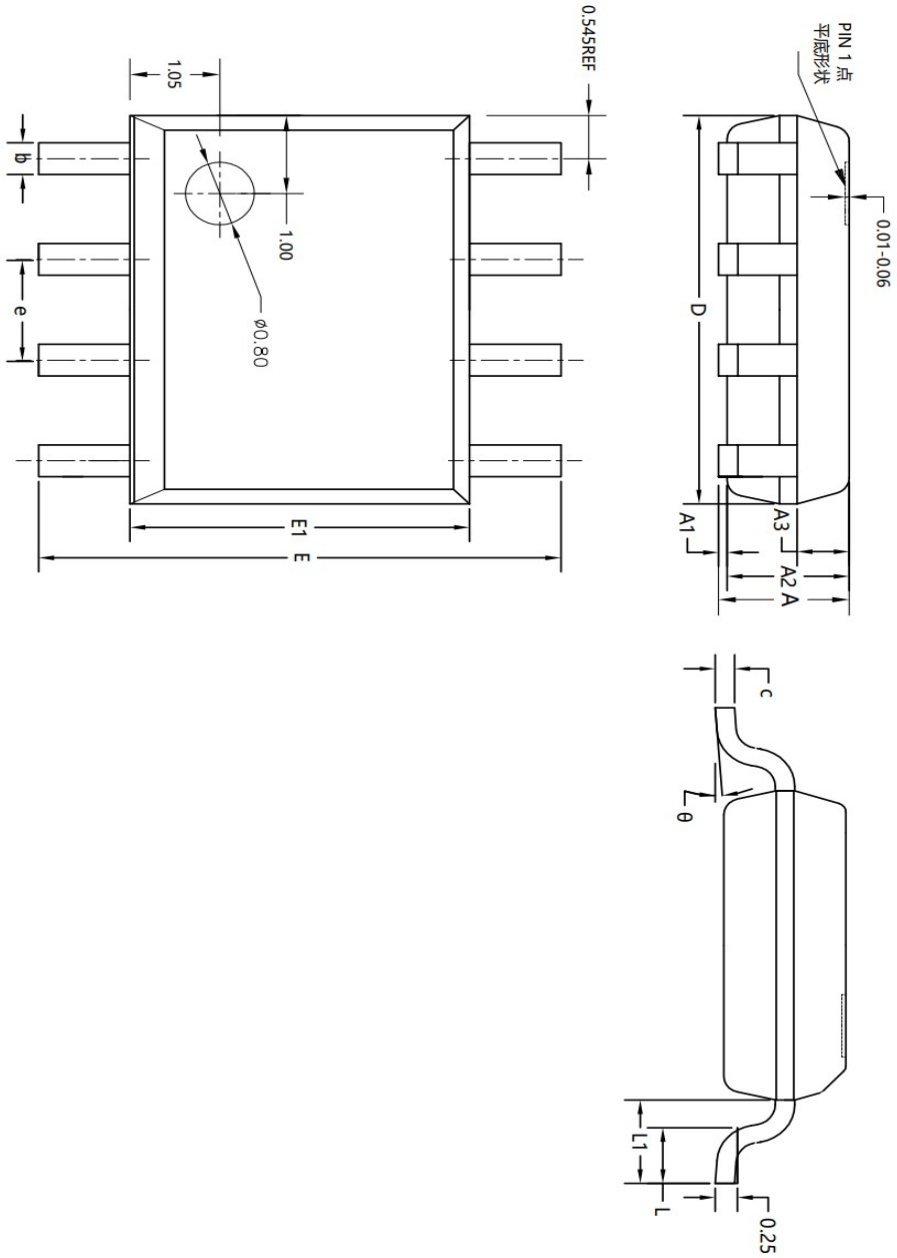


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

NOTES:
1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "0.22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "0.22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE ⊟ .

- ***SOP8 (150 mil)***



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.55	1.65	1.75
A1	0.10	0.20	0.25
A2	1.35	1.45	1.55
A3	0.60	0.70	0.80
b	0.30	0.40	0.50
c	0.17	0.20	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05REF		
θ	0°	4°	8°