Precision, 200-µA Supply Current, 2.7-V to 36-V Supply Instrumentation Amplifier with Rail-to-Rail Output

Check for Samples: INA826

FEATURES

- **Input Common-Mode Range: Includes V–**
- **Common-Mode Rejection:**
  - **104 dB, min (G = 10)**
  - **100 dB, min at 5 kHz (G = 10)**
- **Power-Supply Rejection: 100 dB, min (G = 1)**
- **Low Offset Voltage: 150 µV, max**
- **Gain Drift: 1 ppm/°C (G = 1), 35 ppm/°C (G > 1)**
- **Noise: 18 nV/√Hz, G ≥ 100**
- **Bandwidth: 1 MHz (G = 1), 60 kHz (G = 100)**
- **Inputs Protected up to ±40 V**
- **Rail-to-Rail Output**
- **Supply Current: 200 µA**
- **Supply Range:**
  - **Single Supply: +2.7 V to +36 V**
  - **Dual Supply: ±1.35 V to ±18 V**
- **Specified Temperature Range: –40°C to +125°C**
- **Packages: MSOP-8, SO-8 and DFN-8**

APPLICATIONS

- **Industrial Process Controls**
- **Circuit Breakers**
- **Battery Testers**
- **ECG Amplifiers**
- **Power Automation**
- **Medical Instrumentation**
- **Portable Instrumentation**

DESCRIPTION

The INA826 is a low-cost instrumentation amplifier that offers extremely low power consumption and operates over a very wide single or dual supply range. A single external resistor sets any gain from 1 to 1000. It offers excellent stability over temperature, even at G > 1, as a result of the low gain drift of only 35 ppm/°C (max).

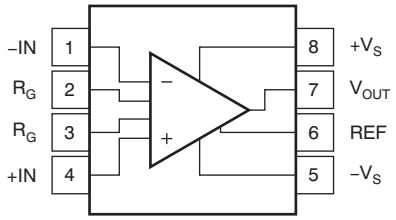
The INA826 is optimized to provide excellent common-mode rejection ratio of over 100 dB (G = 10) over frequencies up to 5 kHz. In G = 1, the common-mode rejection ratio exceeds 84 dB across the full input common-mode range from the negative supply all the way up to 1 V of the positive supply. Using a rail-to-rail output, the INA826 is well-suited for low voltage operation from a 2.7 V single supply as well as dual supplies up to ±18 V.

Additional circuitry protects the inputs against overvoltage of up to ±40 V beyond the power supplies by limiting the input currents to less than 8 mA.

The INA826 is available in SO-8, MSOP-8, and tiny 3-mm × 3-mm DFN-8 surface-mount packages. All versions are specified for the –40°C to +125°C temperature range.

RELATED PRODUCTS

DEVICE	DESCRIPTION
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion
PGA112	Precision programmable gain op amp with SPI™ interface



MSOP-8, SO-8

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR
INA826	MSOP-8	DGK
	SO-8	D
	DFN-8	DRG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		INA826	UNIT
Supply voltage		±20	V
Input voltage range		$(-V_S) - 40$ to $(+V_S) + 40$	V
REF input		±20	V
Output short-circuit(2)		Continuous	
Operating temperature range, T_A		–50 to +150	°C
Storage temperature range, T_A		–65 to +150	°C
Junction temperature, T_J		+175	°C
ESD rating	Human body model (HBM)	2500	V
	Charged device model (CDM)	1500	V
	Machine model (MM)	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to $V_S/2$.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS		INA826 MIN	INA826 TYP	INA826 MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1)	RTI			40	150	µV
		vs temperature, T_A = –40°C to +125°C			0.4	2	µV/°C
V_{OSO}	Output stage offset voltage(1)	RTI			200	700	µV
		vs temperature, T_A = –40°C to +125°C			2	10	µV/°C
PSRR	Power supply rejection	G = 1, RTI		100	124		dB
		G = 10, RTI		115	130		dB
		G = 100, RTI		120	140		dB
		G = 1000, RTI		120	140		dB
Z_{IN}	Differential impedance				20 || 1		GΩ || pF
Z_{IN}	Common-mode impedance				10 || 5		GΩ || pF
	RFI filter, –3-dB frequency				20		MHz
V_{CM}	Operating input range(2)			V–		(V+) – 1	V
		V_S = ±1.35 V to ±18 V, T_A = –40°C to +125°C		See Figure 41 to Figure 44			V
	Input overvoltage range	T_A = –40°C to +125°C				±40	V
CMRR	Common-mode rejection	DC to 60 Hz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84	95		dB
			G = 10, V_{CM} = (V–) to (V+) – 1 V	104	115		dB
			G = 100, V_{CM} = (V–) to (V+) – 1 V	120	130		dB
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	120	130		dB
			G = 1, V_{CM} = (V–) to (V+) – 1 V, T_A = –40°C to +125°C	80			dB
		At 5 kHz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84			dB
			G = 10, V_{CM} = (V–) to (V+) – 1 V	100			dB
			G = 100, V_{CM} = (V–) to (V+) – 1 V	105			dB
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	105			dB
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S/2			35	65	nA
		T_A = –40°C to +125°C				95	nA
I_{OS}	Input offset current	V_{CM} = V_S/2			0.7	5	nA
		T_A = –40°C to +125°C				10	nA
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise(3)	f = 1 kHz, G = 100, R_S = 0 Ω			18	20	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.52		$µV_{PP}$
e_{NO}	Output stage voltage noise(3)	f = 1 kHz, G = 1, R_S = 0 Ω			110	115	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 1, R_S = 0 Ω			3.3		$µV_{PP}$
i_N	Noise current	f = 1 kHz			100		fA/√Hz
		f_B = 0.1 Hz to 10 Hz			5		pA_{PP}

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.

(2) Input voltage range of the INA826 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See Typical Characteristic curves Figure 9 through Figure 16 and Figure 41 through Figure 44 for more information.

(3) Total RTI voltage noise = $\sqrt{(e_{NI})^2 + \left(\frac{e_{NO}}{G}\right)^2}$.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA826 MIN	INA826 TYP	INA826 MAX	UNIT
GAIN						
G	Gain equation			$1 + \left(\frac{49.4\ k\Omega}{R_G}\right)$		V/V
G	Range of gain		1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V		±0.003	±0.015	%
		G = 10, V_O = ±10 V		±0.03	±0.15	%
		G = 100, V_O = ±10 V		±0.04	±0.15	%
		G = 1000, V_O = ±10 V		±0.04	±0.15	%
	Gain vs temperature(4)	G = 1, T_A = –40°C to +125°C		±0.1	±1	ppm/°C
		G > 1, T_A = –40°C to +125°C		±10	±35	ppm/°C
	Gain nonlinearity	G = 1 to 100, V_O = –10 V to +10 V		1	5	ppm
		G = 1000, V_O = –10 V to +10 V		5	20	ppm
OUTPUT						
	Voltage swing	R_L = 10 kΩ	(V–) + 0.1		(V+) – 0.15	V
	Load capacitance stability			1000		pF
	Open loop output impedance			See Figure 56		
	Short-circuit current	Continuous to V_S/2		±16		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		1		MHz
		G = 10		500		kHz
		G = 100		60		kHz
		G = 1000		6		kHz
SR	Slew rate	G = 1, V_O = ±14.5 V		1		V/µs
		G = 100, V_O = ±14.5 V		1		V/µs
t_S	Settling time to 0.01%	G = 1, V_{STEP} = 10 V		12		µs
		G = 10, V_{STEP} = 10 V		12		µs
		G = 100, V_{STEP} = 10 V		24		µs
		G = 1000, V_{STEP} = 10 V		224		µs
t_S	Settling time to 0.001%	G = 1, V_{STEP} = 10 V		14		µs
		G = 10, V_{STEP} = 10 V		14		µs
		G = 100, V_{STEP} = 10 V		31		µs
		G = 1000, V_{STEP} = 10 V		278		µs

(4) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA826 MIN	INA826 TYP	INA826 MAX	UNIT
REFERENCE INPUT						
R_{IN}	Input impedance			100		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01		%
POWER SUPPLY						
V_S	Power-supply voltage	Single	+2.7		+36	V
		Dual	±1.35		±18	V
I_Q	Quiescent current	V_{IN} = 0 V		200	250	µA
		vs temperature, T_A = –40°C to +125°C		250	300	µA
TEMPERATURE RANGE						
	Specified		–40		+125	°C
	Operating		–50		+150	°C

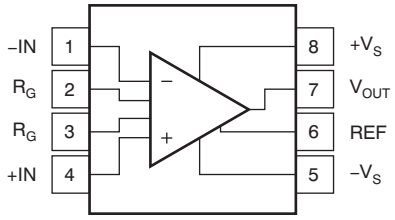
THERMAL INFORMATION

THERMAL METRIC(1)		INA826 D (SOIC) 8 PINS	INA826 DGK (MSOP) 8 PINS	INA826 DRG (DFN) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	141.4	215.4	50.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	75.4	66.3	60.0	
θ_{JB}	Junction-to-board thermal resistance	59.6	97.8	25.4	
ψ_{JT}	Junction-to-top characterization parameter	27.4	10.5	1.2	
ψ_{JB}	Junction-to-board characterization parameter	59.1	96.1	25.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.2	

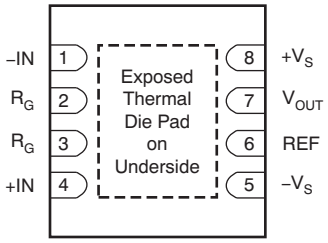
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

DGK PACKAGE
MSOP-8, SO-8
(TOP VIEW)



DRG PACKAGE
3-mm × 3-mm DFN-8
(TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
–IN	1	Negative input
R_G	2	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
R_G	3	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
+IN	4	Positive input
$–V_S$	5	Negative supply
REF	6	Reference input. This pin must be driven by low impedance.
V_{OUT}	7	Output
$+V_S$	8	Positive supply

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

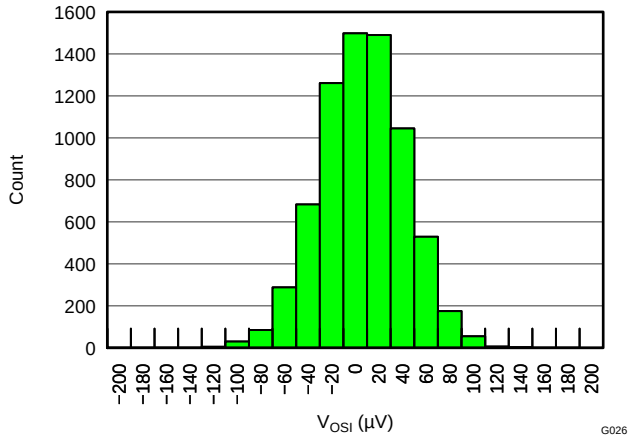


Figure 1.

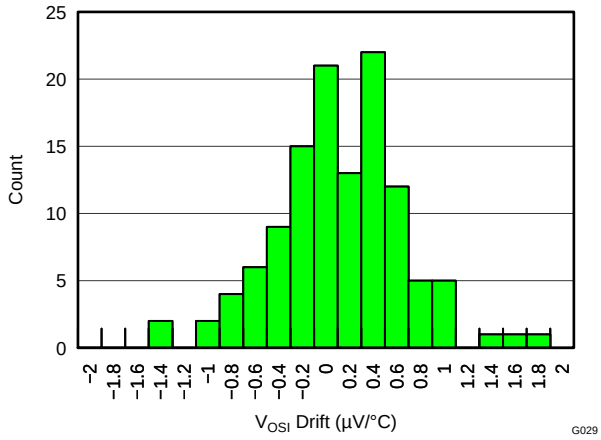


Figure 2.

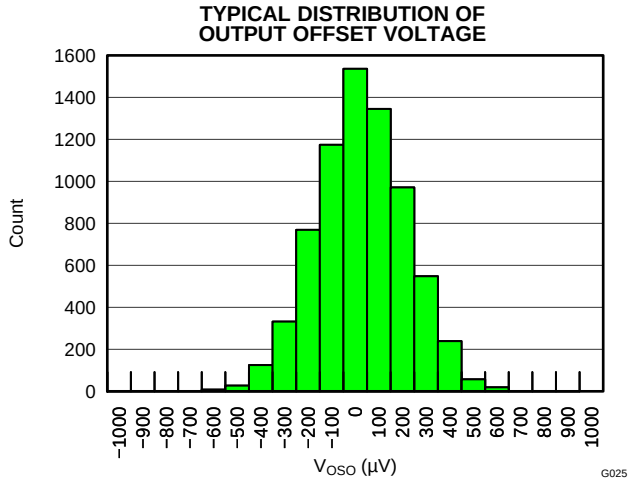


Figure 3.

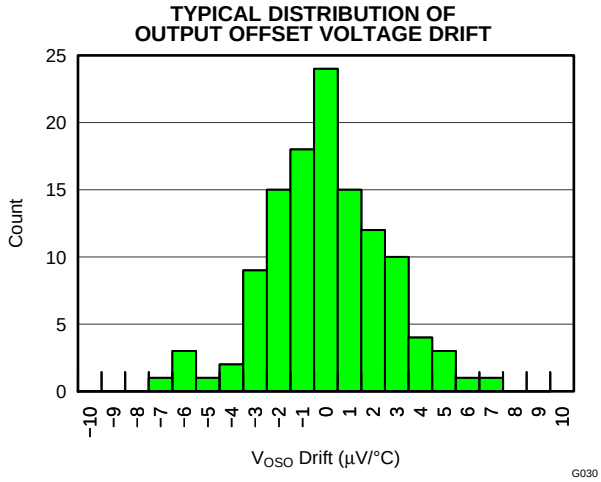


Figure 4.

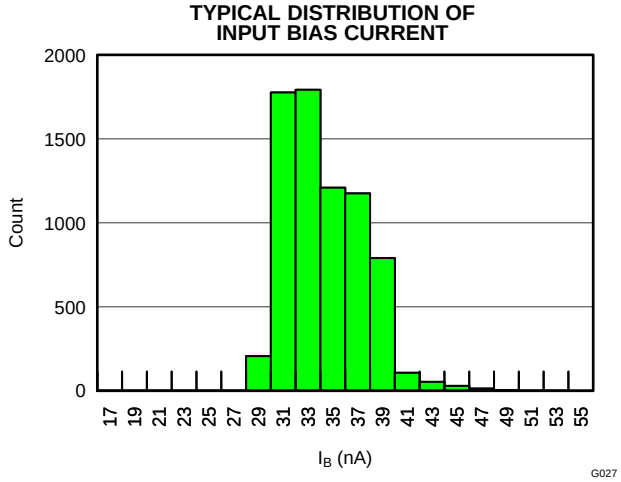


Figure 5.

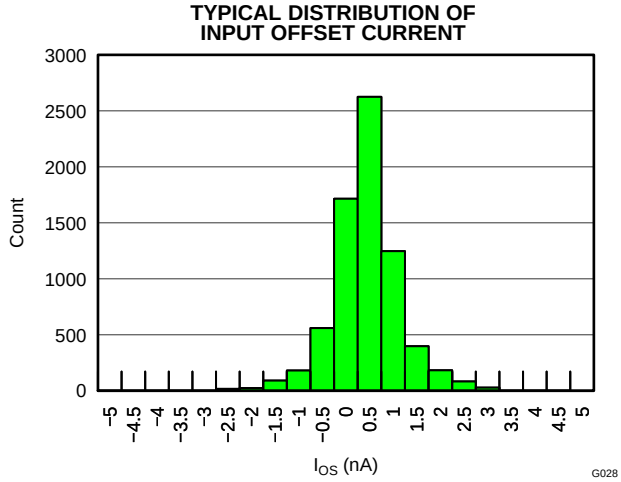


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

TYPICAL GAIN ERROR DRIFT DISTRIBUTION (G = 1)

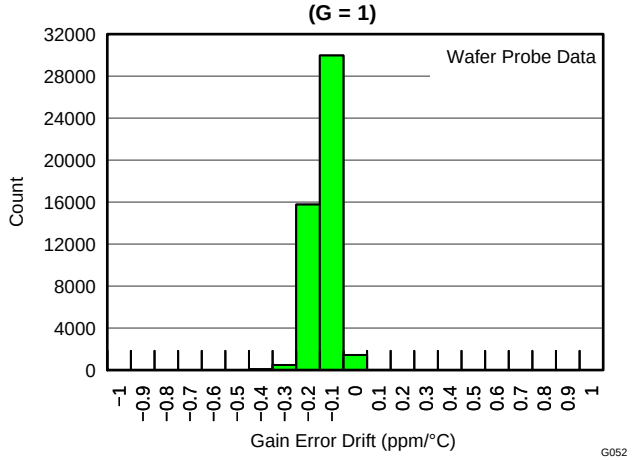


Figure 7.

TYPICAL GAIN ERROR DRIFT DISTRIBUTION (G > 1)

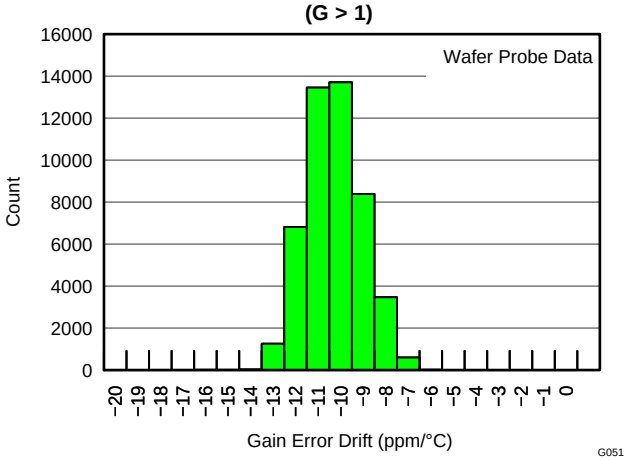


Figure 8.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Single Supply, V_S = +2.7 V, G = 1)

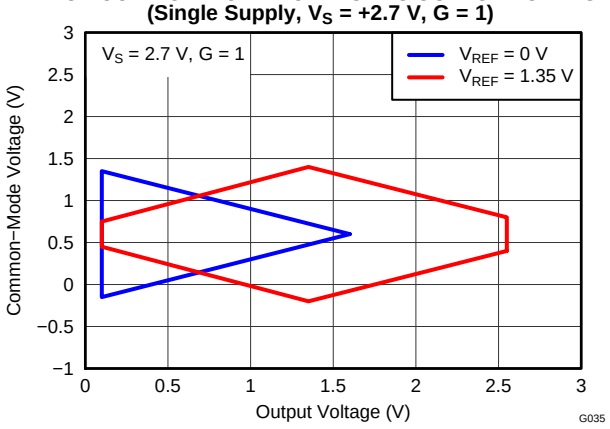


Figure 9.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Single Supply, V_S = +2.7 V, G = 100)

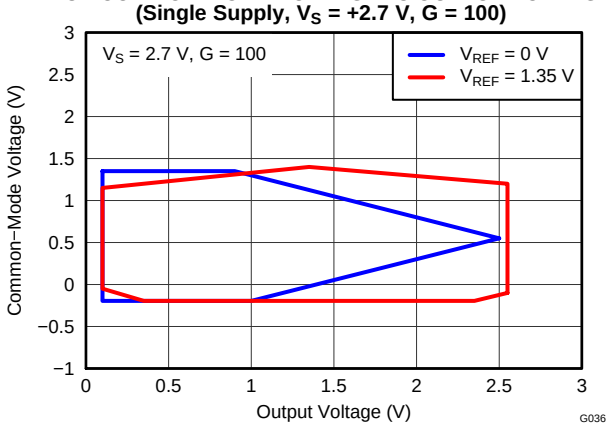


Figure 10.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Single Supply, V_S = +5 V, G = 1)

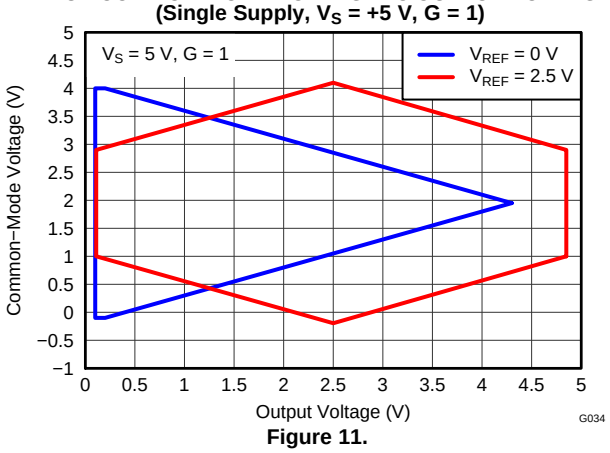


Figure 11.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Single Supply, V_S = +5 V, G = 100)

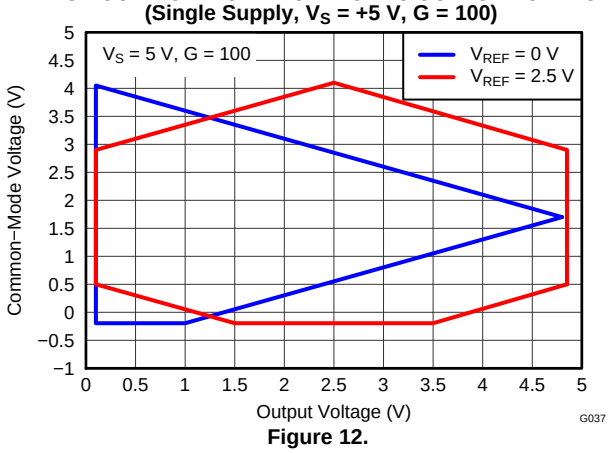


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Dual Supply, V_S = ±3.3 V)

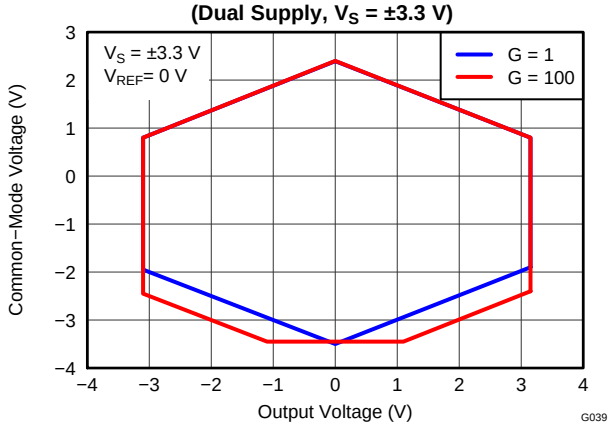


Figure 13.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Dual Supply, V_S = ±5 V)

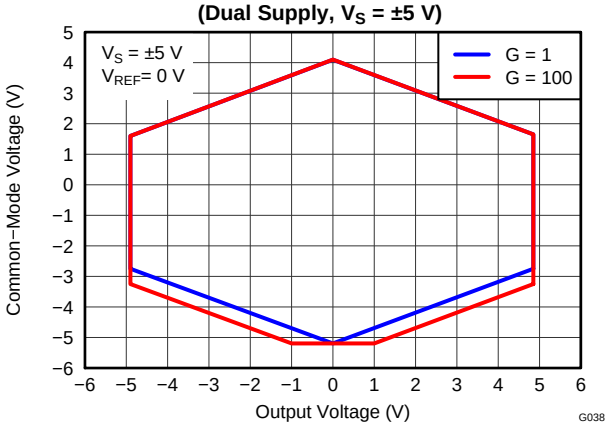


Figure 14.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Dual Supply, V_S = ±15 V, ±12 V, G = 1)

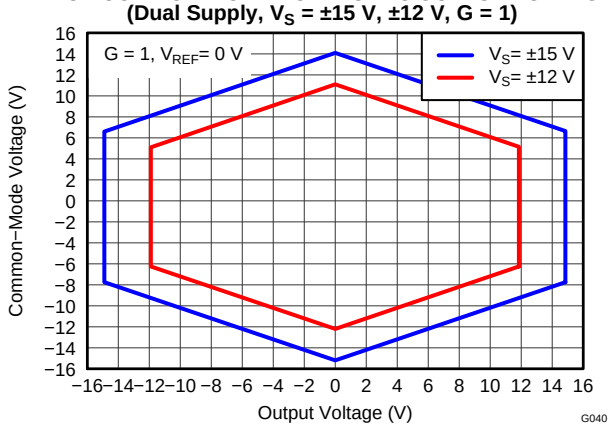


Figure 15.

INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE (Dual Supply, V_S = ±15 V, ±12 V, G = 100)

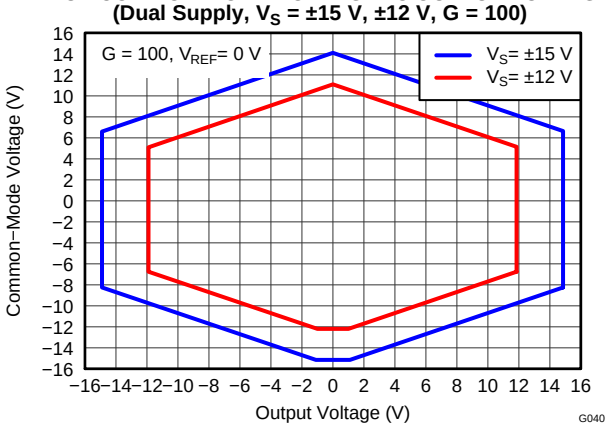


Figure 16.

INPUT OVERVOLTAGE vs INPUT CURRENT (G = 1, V_S = ±15 V)

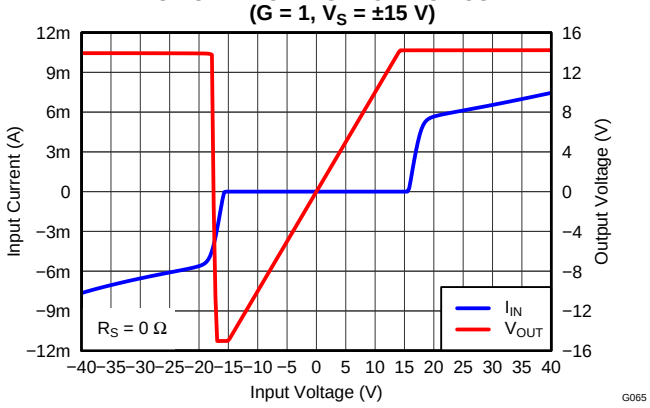


Figure 17.

INPUT OVERVOLTAGE vs INPUT CURRENT WITH 10-kΩ RESISTANCE (G = 1, V_S = ±15 V)

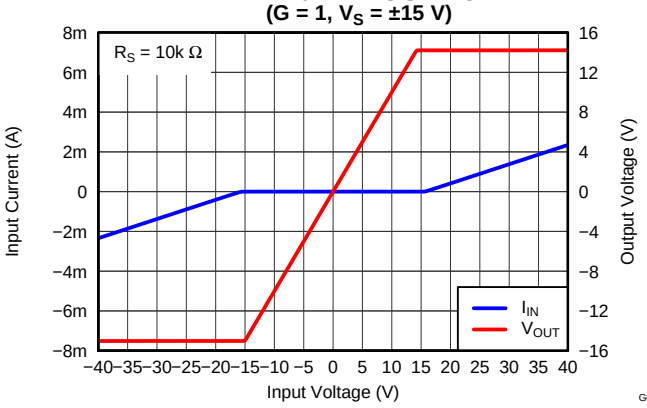


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

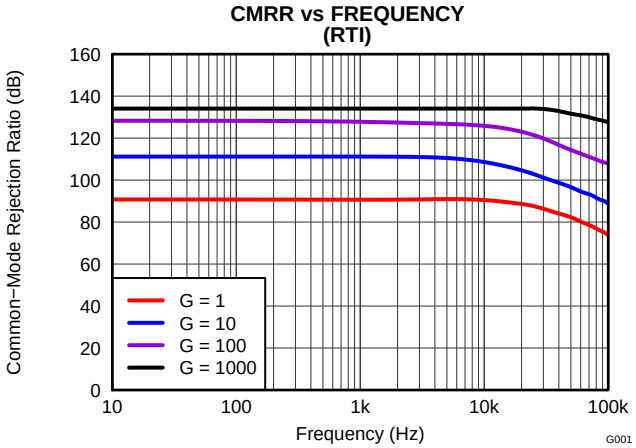


Figure 19.

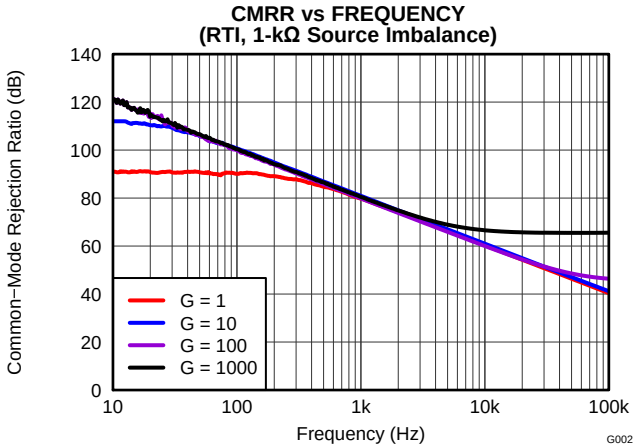


Figure 20.

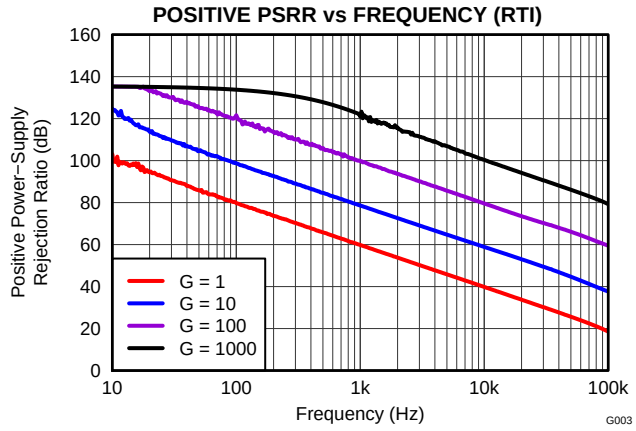


Figure 21.

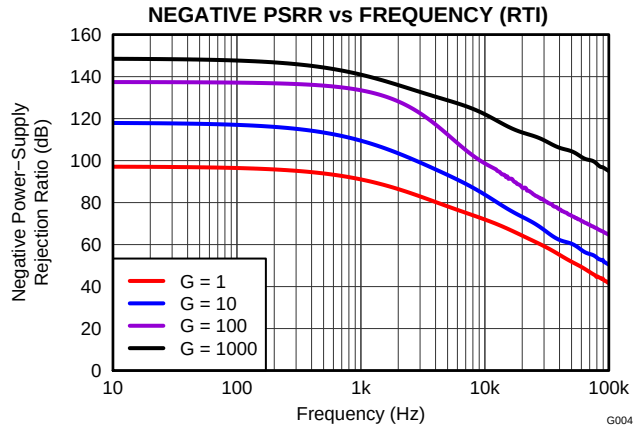


Figure 22.

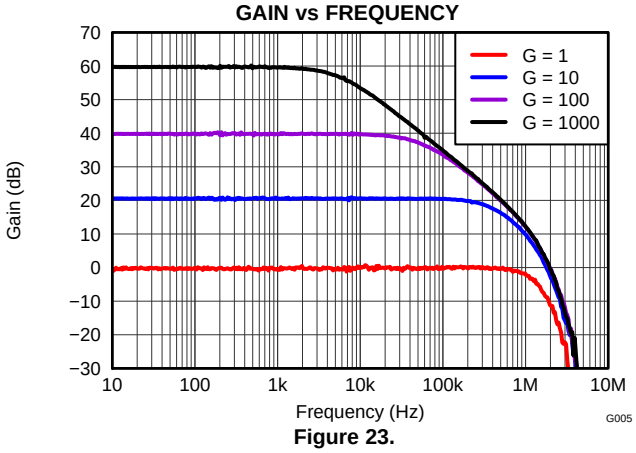


Figure 23.

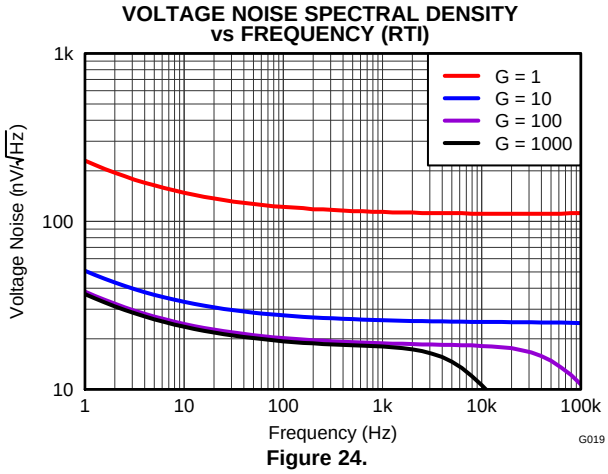


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY (RTI)

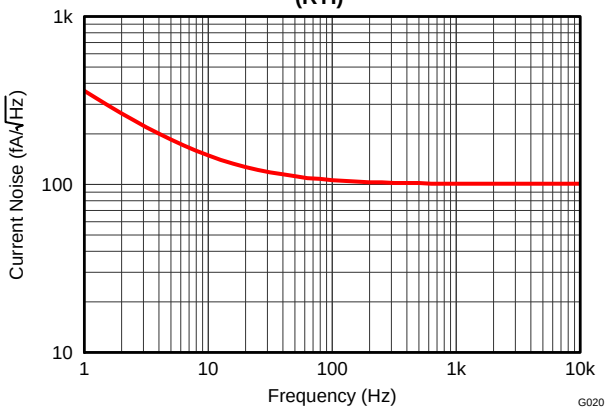


Figure 25.

0.1-Hz TO 10-Hz RTI VOLTAGE NOISE (G = 1)

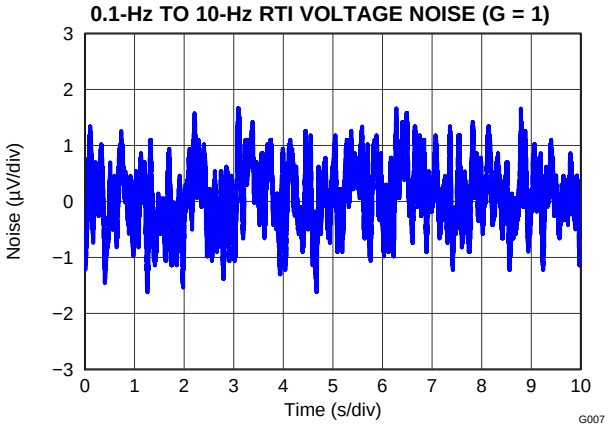


Figure 26.

0.1-Hz TO 10-Hz RTI VOLTAGE NOISE (G = 1000)

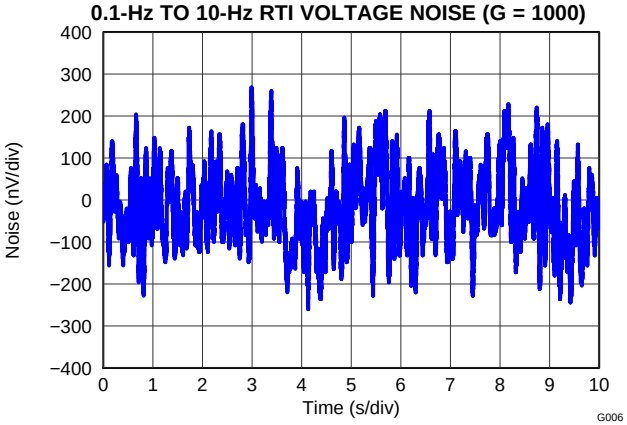


Figure 27.

0.1-Hz TO 10-Hz RTI CURRENT NOISE

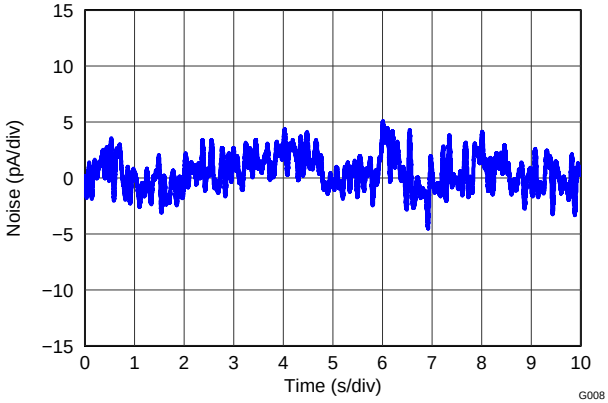


Figure 28.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE (V_S = +2.7 V)

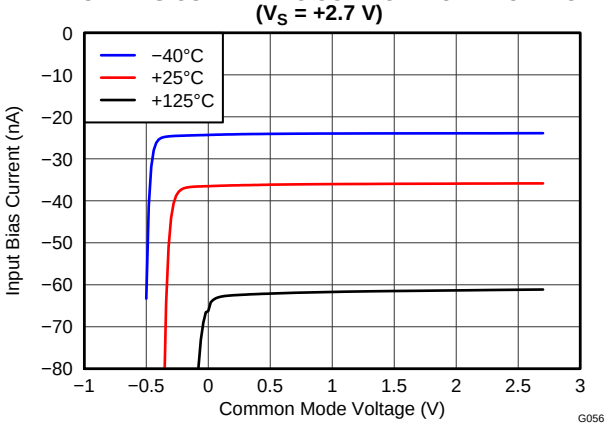


Figure 29.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE (V_S = ±15 V)

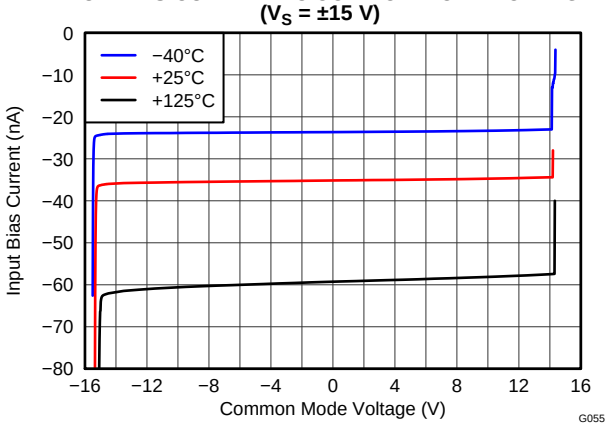


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

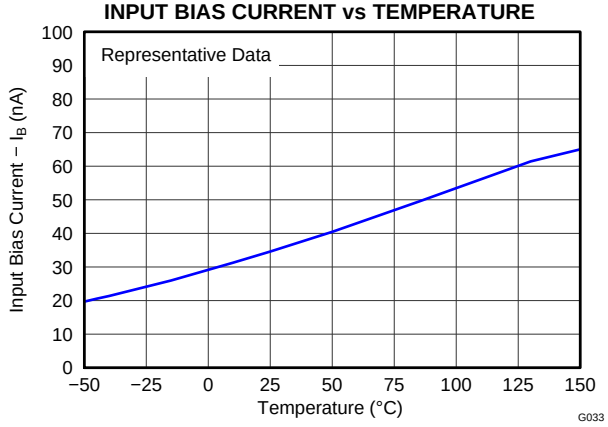


Figure 31.

INPUT OFFSET CURRENT vs TEMPERATURE

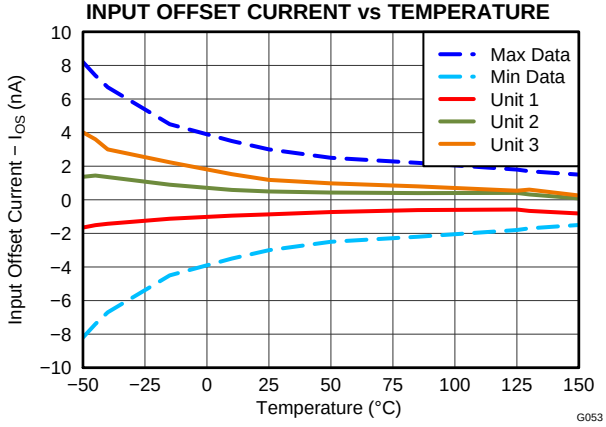


Figure 32.

GAIN ERROR vs TEMPERATURE (G = 1)

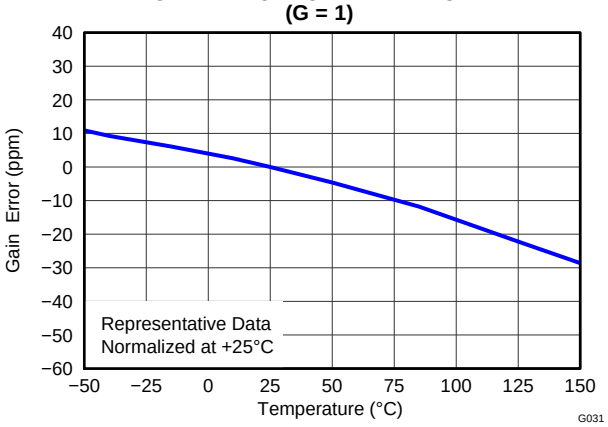


Figure 33.

GAIN ERROR vs TEMPERATURE (G > 1)

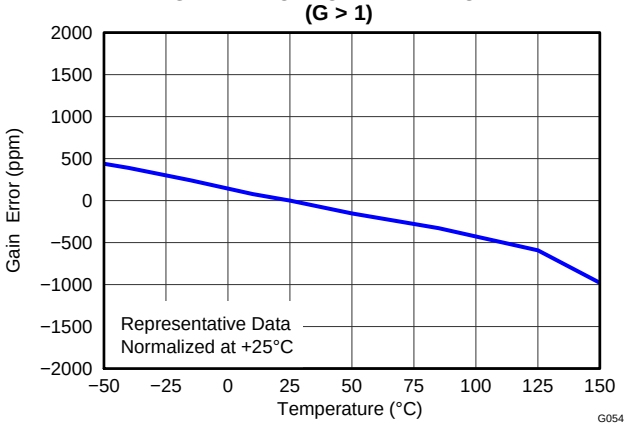


Figure 34.

CMRR vs TEMPERATURE (G = 1)

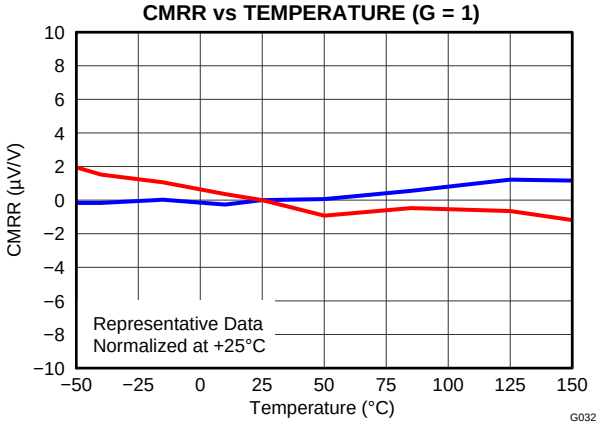


Figure 35.

SUPPLY CURRENT vs TEMPERATURE

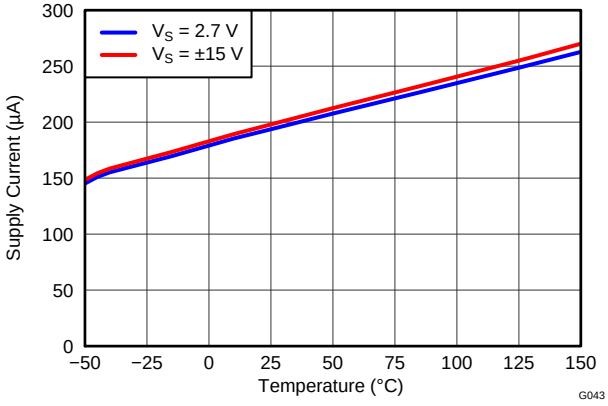


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

GAIN NONLINEARITY (G = 1)

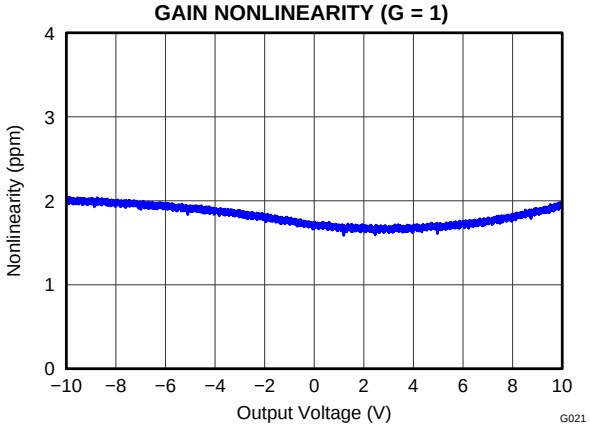


Figure 37.

GAIN NONLINEARITY (G = 10)

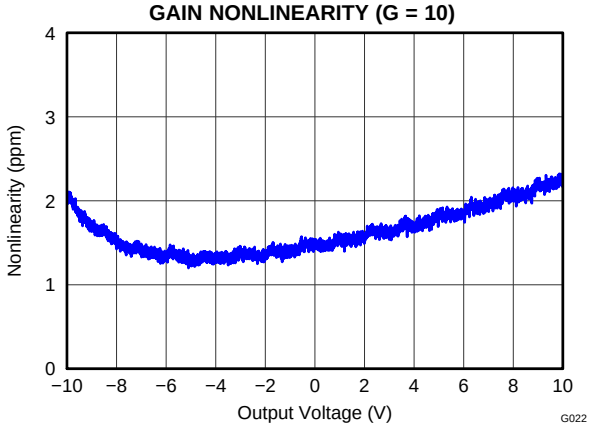


Figure 38.

GAIN NONLINEARITY (G = 100)

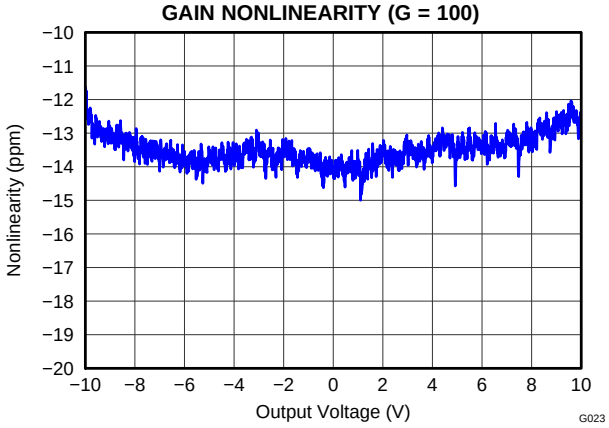


Figure 39.

GAIN NONLINEARITY (G = 1000)

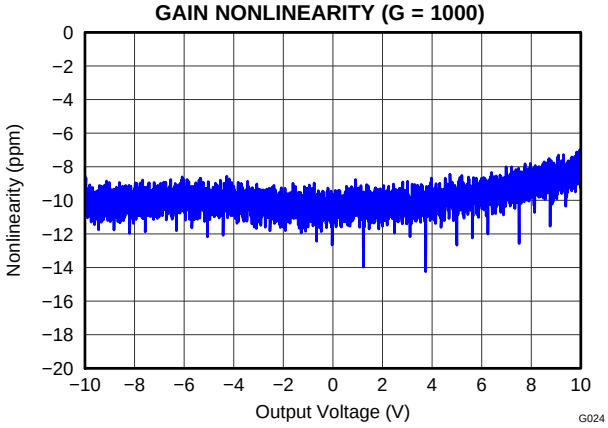


Figure 40.

OFFSET VOLTAGE vs NEGATIVE COMMON-MODE VOLTAGE (V_S = ±15 V)

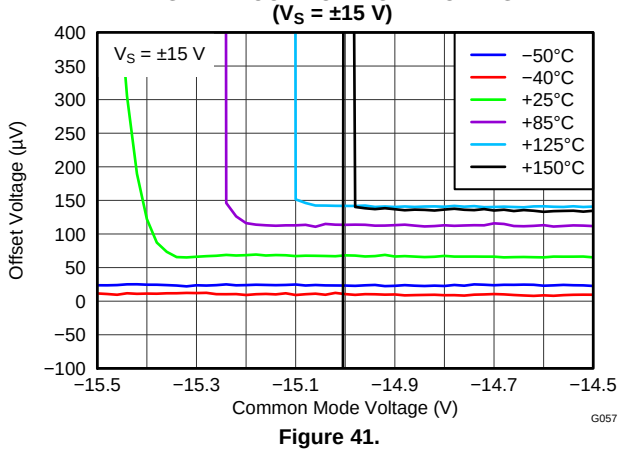


Figure 41.

OFFSET VOLTAGE vs POSITIVE COMMON-MODE VOLTAGE (V_S = ±15 V)

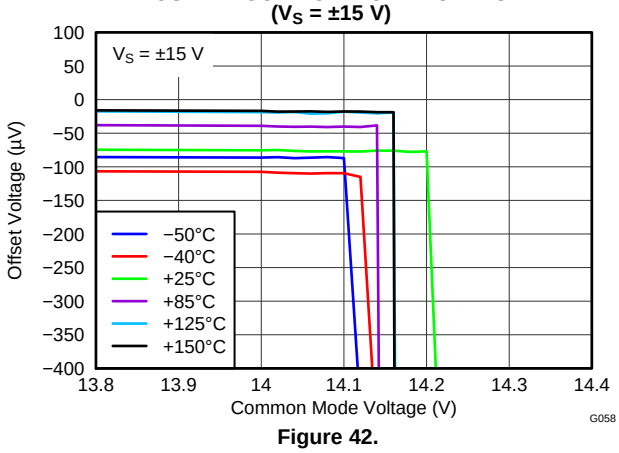


Figure 42.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

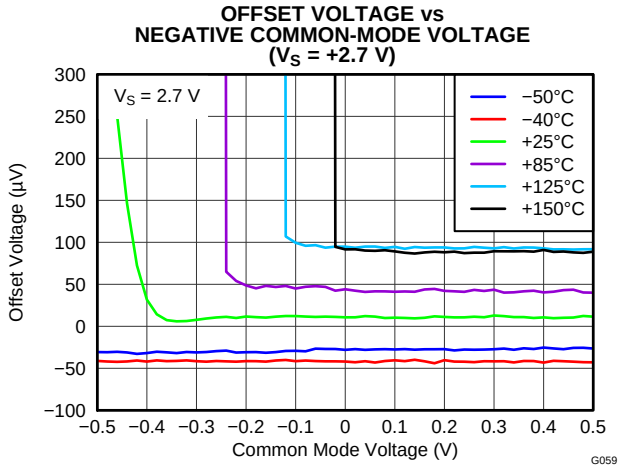


Figure 43.

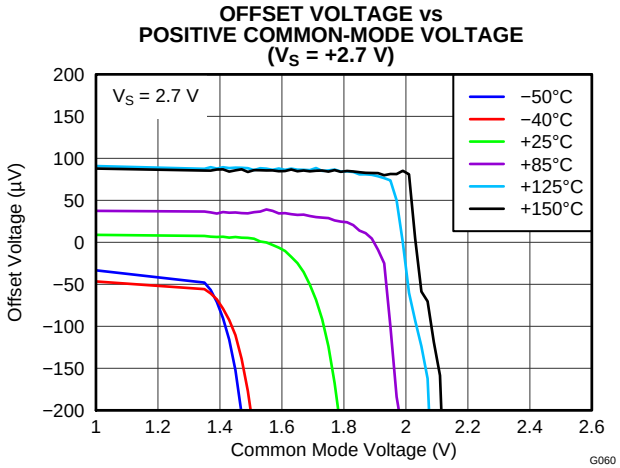


Figure 44.

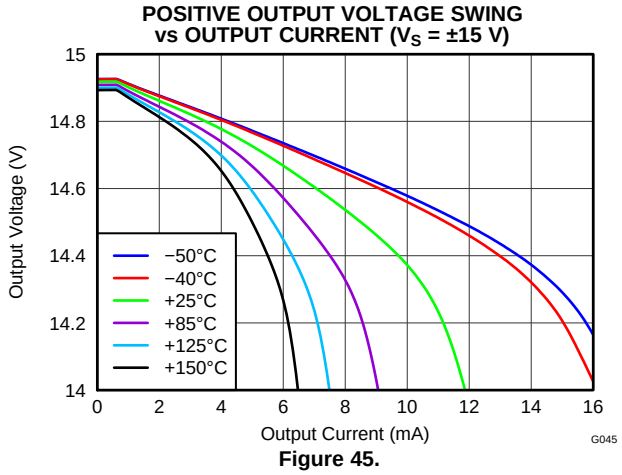


Figure 45.

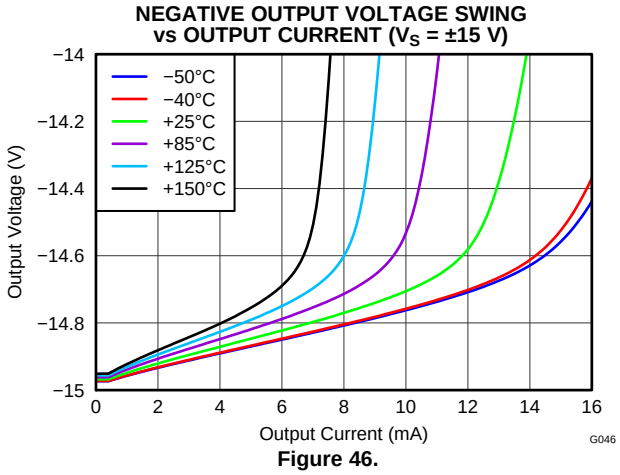


Figure 46.

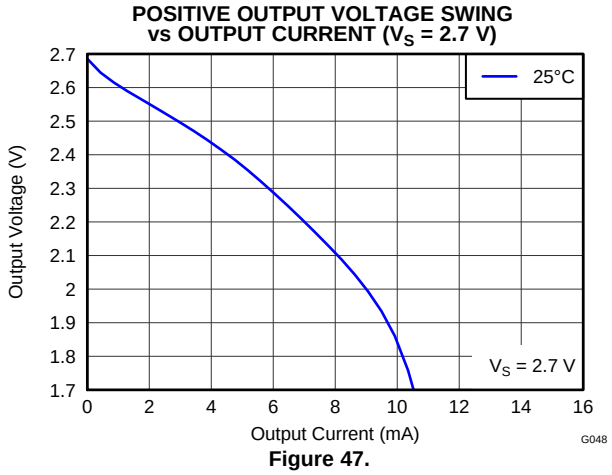


Figure 47.

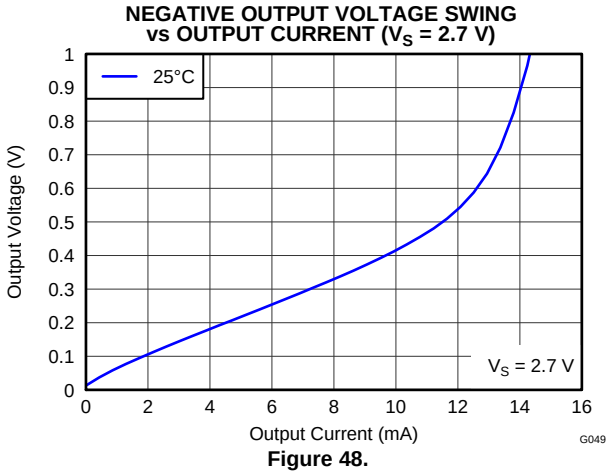


Figure 48.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

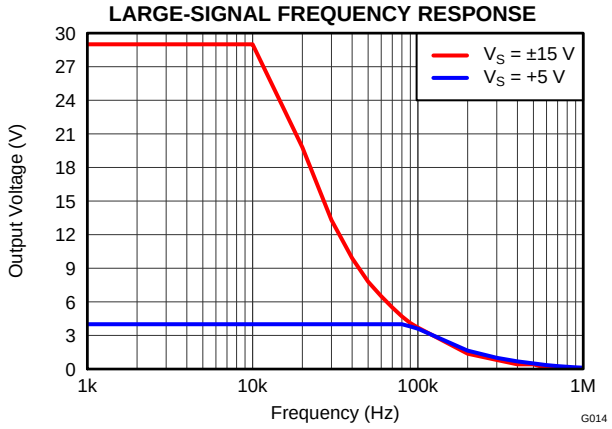


Figure 49.

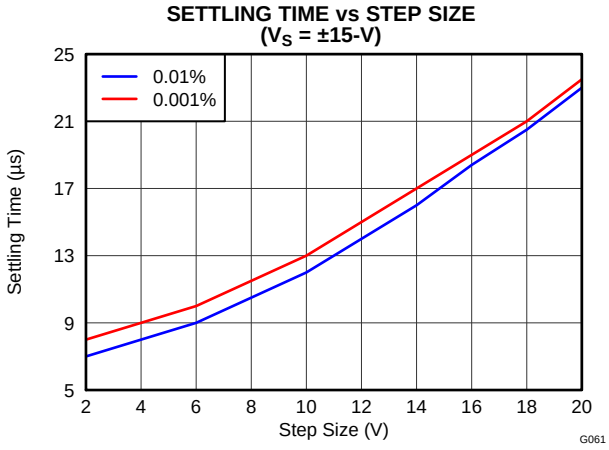


Figure 50.

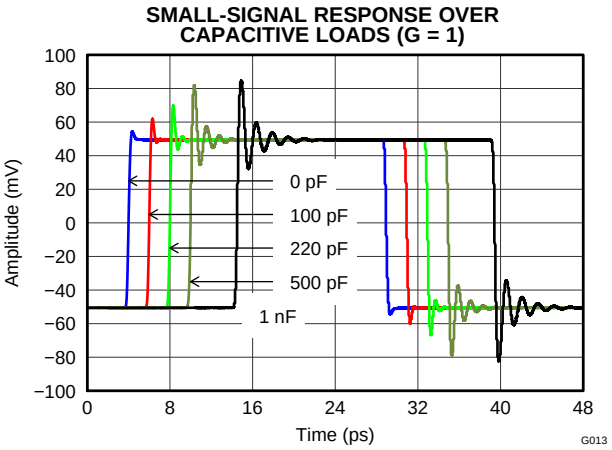


Figure 51.

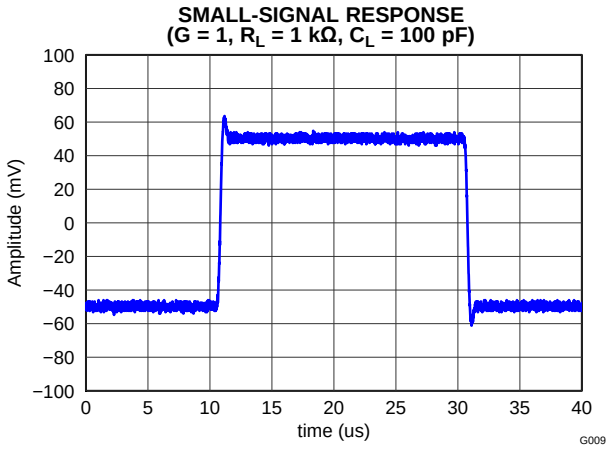


Figure 52.

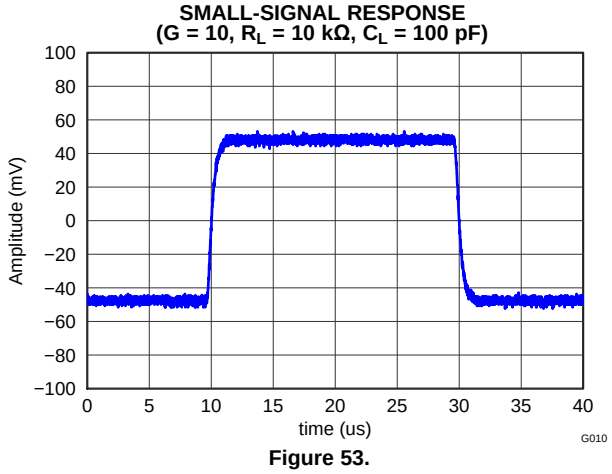


Figure 53.

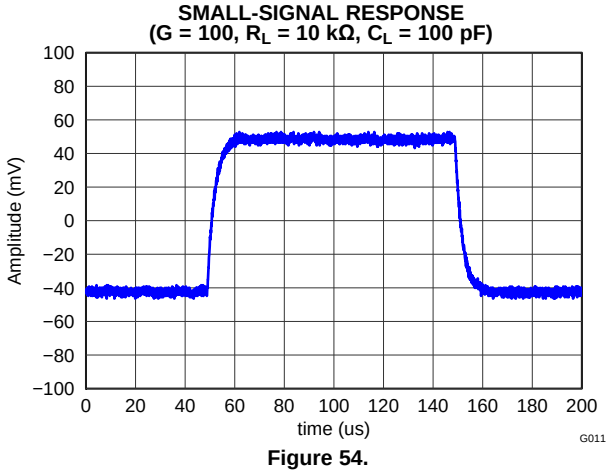


Figure 54.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1, unless otherwise noted.

SMALL-SIGNAL RESPONSE
(G = 1000, R_L = 10 kΩ, C_L = 100 pF)

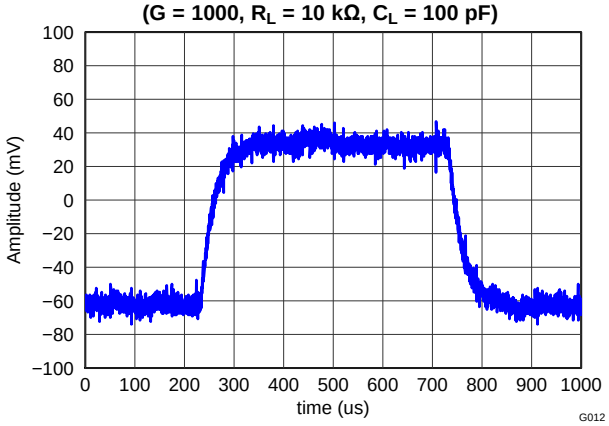


Figure 55.

OPEN-LOOP OUTPUT IMPEDANCE

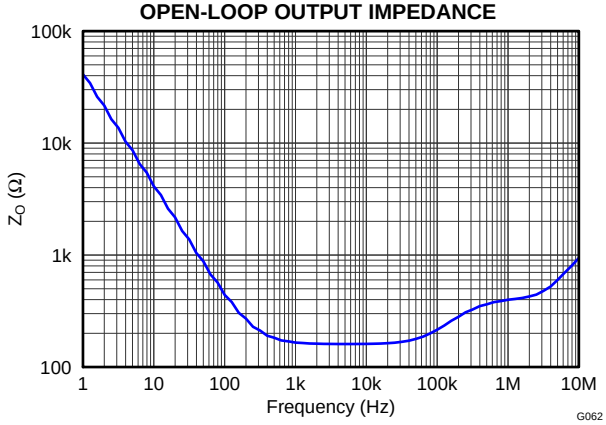


Figure 56.

CHANGE IN INPUT OFFSET VOLTAGE vs WARM-UP TIME

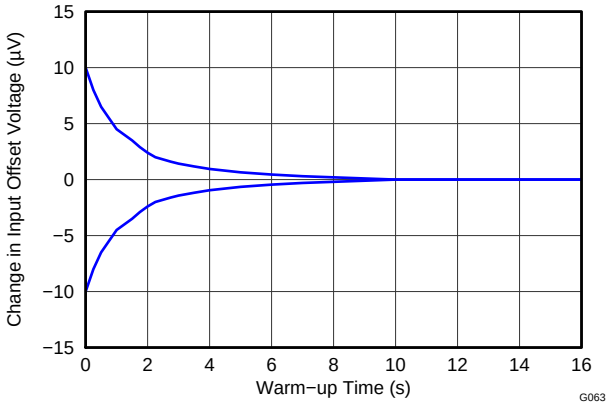
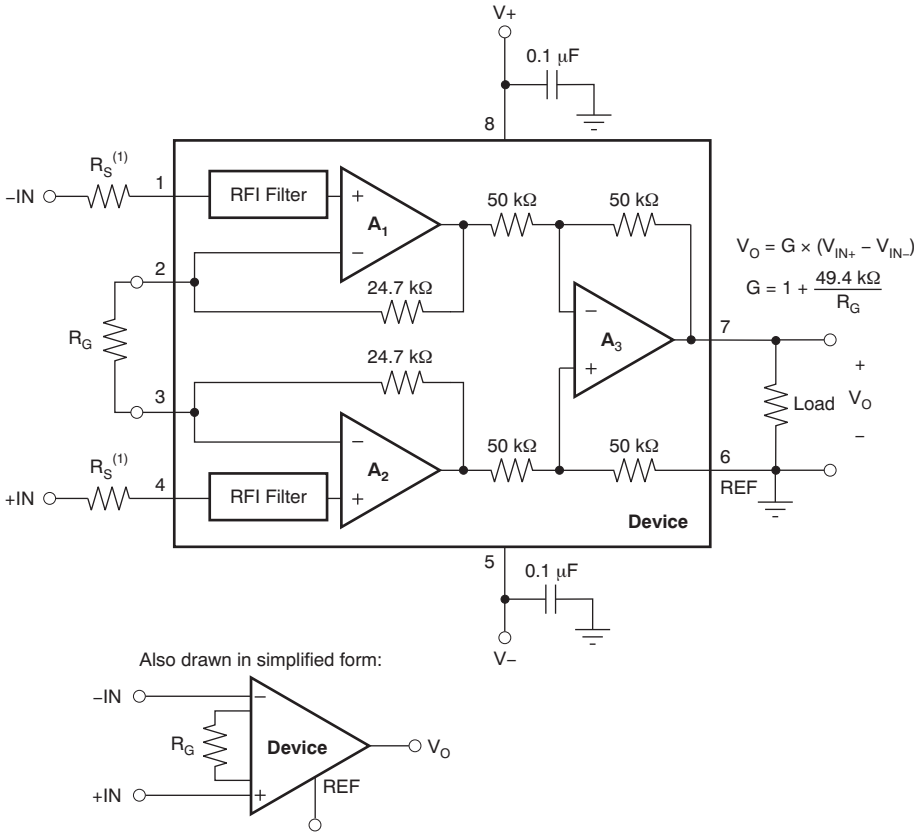


Figure 57.

APPLICATION INFORMATION

Figure 58 shows the basic connections required for operation of the INA826. Good layout practice mandates the use of bypass capacitors placed as close to the device pins as possible.

The output of the INA826 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 5 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.



(1) This resistor is optional if the input voltage stays above [(V–) – 2 V] or the signal source current drive capability is limited to less than 3.5 mA. See the *Input Protection* section for more details.

Figure 58. Basic Connections

SETTING THE GAIN

Gain of the INA826 is set by a single external resistor, R_G, connected between pins 2 and 3. The value of R_G is selected according to Equation 1:

$$G = 1 + \left(\frac{49.4\ k\Omega}{R_G} \right) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 49.4-kΩ term in Equation 1 comes from the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA826.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
1	—	—
2	49.4k	49.9k
5	12.35k	12.4k
10	5.489k	5.49k
20	2.600k	2.61k
50	1.008k	1k
100	499	499
200	248	249
500	99	100
1000	49.5	49.9

Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain of Equation 1.

The best gain drift of 1 ppm/°C can be achieved when the INA826 uses G = 1 without R_G connected. In this case, the gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 50-kΩ resistors in the differential amplifier (A_3). At G greater than 1, the gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. Process improvements of the temperature coefficient of the feedback resistors now make it possible to specify a maximum gain drift of the feedback resistors of 35 ppm/°C, thus significantly improving the overall temperature stability of applications using gains greater than 1.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see Typical Characteristics curves (Figure 19 and Figure 20).

OFFSET TRIMMING

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 59 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.

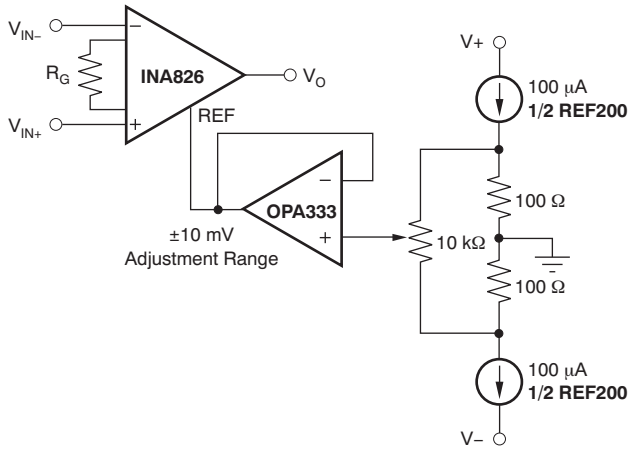


Figure 59. Optional Trimming of Output Offset Voltage

INPUT COMMON-MODE RANGE

The linear input voltage range of the INA826 input circuitry extends from the negative supply voltage to 1 V below the positive supply, while maintaining 84-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is described in the typical characteristic curves (*Input Common-Mode Voltage vs Output Voltage*, Figure 9 through Figure 16) and *Offset Voltage vs Common-Mode Voltage* (Figure 41 through Figure 44). The INA826 can operate over a wide range of power supplies and V_{REF} configurations, making it impractical to provide a comprehensive guide to common-mode range limits for all possible conditions.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2, which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see Figure 60) provides a check for the most common overload conditions. The designs of A_1 and A_2 are identical and the outputs can swing to within approximately 100 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 may continue to be in linear operation, responding to changes in the noninverting input voltage. This difference may give the appearance of linear operation but the output voltage is invalid.

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA826 employs a current-feedback topology with PNP input transistors; see Figure 60. The matched PNP transistors Q_1 and Q_2 shift the input voltages of both inputs up by a diode drop, and through the feedback network, shift the output of A_1 and A_2 by approximately +0.8 V. With both inputs and V_{REF} at single-supply ground (negative power supply), the output of A_1 and A_2 is well within the linear range, allowing users to make differential measurements at the GND level. As a result of this input level-shifting, the voltages at pin 2 and pin 3 are not equal to the respective input terminal voltages (pin 1 and pin 4). For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

INSIDE THE INA826

See Figure 58 for a simplified representation of the INA826. A more detailed diagram (shown in Figure 60) provides additional insight into the INA826 operation.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

The differential input voltage is buffered by Q_1 and Q_2 and is impressed across R_G, causing a signal current to flow through R_G, R_1, and R_2. The output difference amp, A_3, removes the common-mode component of the input signal and refers the output signal to the REF terminal.

The equations shown in Figure 60 describe the output voltages of A_1 and A_2. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V higher than the input voltages.

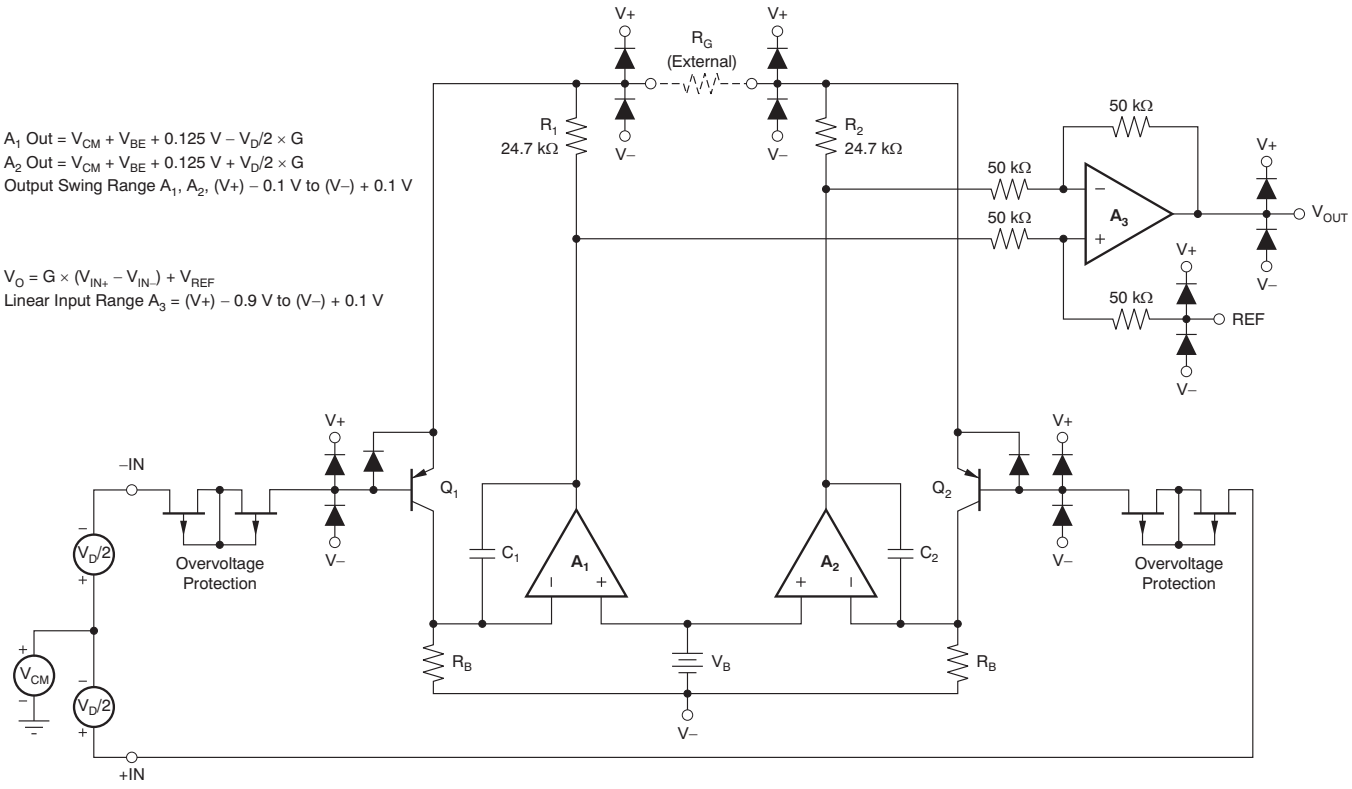


Figure 60. INA826 Simplified Circuit Diagram

INPUT PROTECTION

The inputs of the INA826 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. However, if the input voltage exceeds (V–) – 2 V and the signal source current drive capability exceeds 3.5 mA, the output voltage switches to the opposite polarity; see typical characteristic curve *Input Overvoltage vs Input Current* (Figure 17). This polarity reversal can easily be avoided by adding resistance of 10 kΩ in series with both inputs.

Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 8 mA. The typical characteristic curves *Input Current vs Input Overvoltage* (Figure 17 and Figure 18) illustrate this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA826 is extremely high—approximately 20 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 35 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 61 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA826, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in Figure 61). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

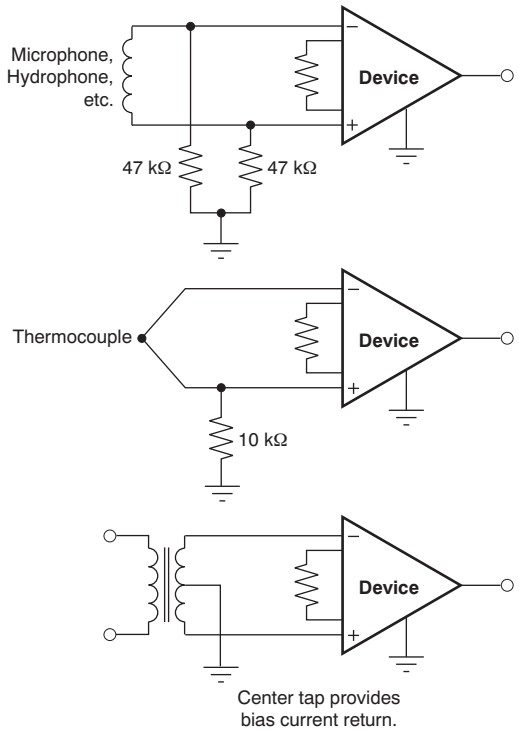


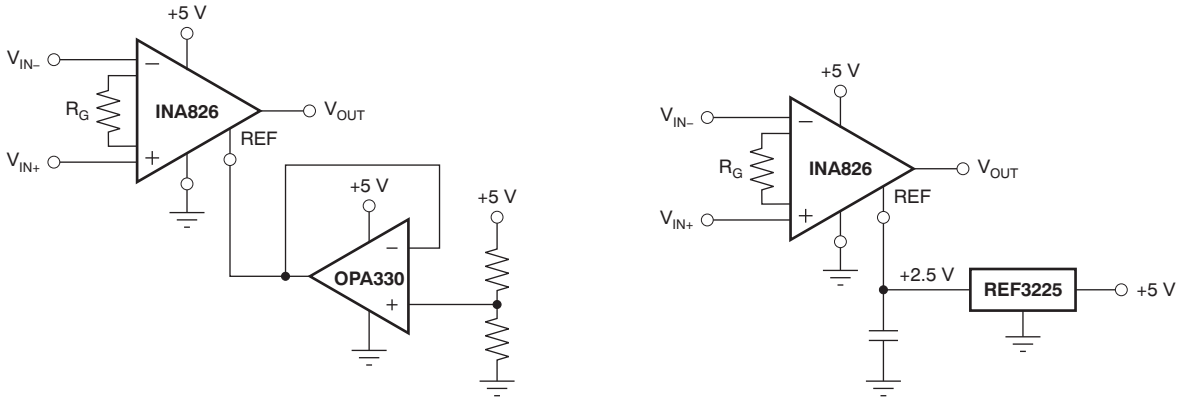
Figure 61. Providing an Input Common-Mode Current Path

REFERENCE TERMINAL

The output voltage of the INA826 is developed with respect to the voltage on the reference terminal. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, it can be useful to offset the output signal to a precise mid-supply level (for example, 2.5 V in a 5-V supply environment). To accomplish this, a voltage source can be tied to the REF pin to level-shift the output so that the INA826 can drive a single-supply ADC, for example.

For the best performance, source impedance to the REF terminal should be kept below 5 Ω. As can be seen in Figure 58, the reference resistor is at one end of a 50-kΩ resistor. Additional impedance at the REF pin adds to this 50-kΩ resistor. The imbalance in the resistor ratios results in degraded common-mode rejection ratio (CMRR).

Figure 62 shows two different methods of driving the reference pin with low impedance. The OPA330 is a low-power, chopper-stabilized amplifier, and therefore offers excellent stability over temperature. It is available in the space-saving SC70 and even smaller chip-scale package. The REF3225 is a precision reference in the small SOT23-6 package.



a) Level shifting using the OPA330 as a low-impedance buffer

b) Level shifting using the low-impedance output of the REF3225

Figure 62. Options for Low-Impedance Level Shifting

DYNAMIC PERFORMANCE

The typical characteristic curve *Gain vs Frequency* (Figure 23) illustrates that, despite its low quiescent current of only 200 µA, the INA826 achieves much wider bandwidth than other INAs in its class. This achievement is a result of using TI's proprietary high-speed precision bipolar process technology. The current-feedback topology provides the INA826 with wide bandwidth even at high gains. Settling time also remains excellent at high gain because of a high slew rate of 1 V/µs.

OPERATING VOLTAGE

The INA826 operates over a power-supply range of +2.7 V to +36 V (±1.35 V to ±18 V). Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Low-Voltage Operation

The INA826 can operate on power supplies as low as ±1.35 V. Most parameters vary only slightly throughout this supply voltage range; see the Typical Characteristics section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The typical characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 9 to Figure 16) and *Offset Voltage vs Common-Mode Voltage* (Figure 41 to Figure 44) describe the range of linear operation for various supply voltages, reference connections, and gains.

ERROR SOURCES

Most modern signal conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, it is important to minimize these errors by choosing high-precision components such as the INA826 that have improved specifications in critical areas that impact the precision of the overall system. Figure 63 shows an example application.

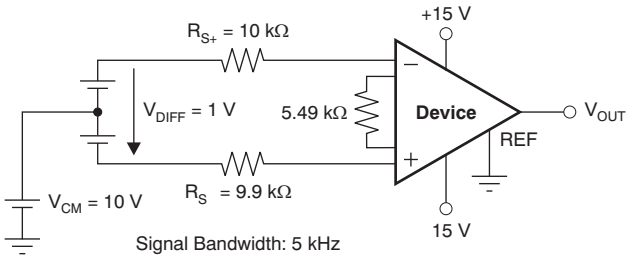


Figure 63. Example Application with G = 10 V/V and 1-V Differential Voltage

Resistor-adjustable INAs such as the INA826 show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V) the gain error becomes a significant error source because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift. The INA826 offers the lowest gain error over temperature in the marketplace for both G > 1 and G = 1 (no external gain resistor). Table 2 summarizes the major error sources in common INA applications and compares the two cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor). As can be seen in Table 2, while the static errors (absolute accuracy errors) in G = 1 are almost twice as great as compared to G = 10, there are much fewer drift errors because of the much lower gain error drift. In most applications, these static errors can readily be removed during calibration in production. All calculations refer the error to the input for easy comparison and system evaluation.

Table 2. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA826		
		SPEC	G = 10 ERROR (ppm)	G = 1 ERROR (ppm)
ABSOLUTE ACCURACY AT +25°C				
Input offset voltage (µV)	V_{OSI}/V_{DIFF}	150	150	150
Output offset voltage (µV)	$V_{OSO}/(G \times V_{DIFF})$	700	70	700
Input offset current (nA)	$I_{OS} \times$ maximum $(R_{S+}, R_{S-})/V_{DIFF}$	5	50	50
CMRR (dB)	$V_{CM}/(10^{CMRR/20} \times V_{DIFF})$	104 (G = 10), 84 (G = 1)	63	631
Total absolute accuracy error (ppm)			333	1531
DRIFT TO +105°C				
Gain drift (ppm/°C)	$GTC \times (T_A - 25)$	35 (G = 10), 1 (G = 1)	2800	80
Input offset voltage drift (µV/°C)	$(V_{OSI\_TC}/V_{DIFF}) \times (T_A - 25)$	2	160	160
Output offset voltage drift (µV/°C)	$[V_{OSO\_TC}/(G \times V_{DIFF})] \times (T_A - 25)$	10	80	800
Offset current drift (pA/°C)	$I_{OS\_TC} \times$ maximum $(R_{S+}, R_{S-}) \times (T_A - 25)/V_{DIFF}$	60	48	48
Total drift error (ppm)			3088	1088
RESOLUTION				
Gain nonlinearity (ppm of FS)		5	5	5
Voltage noise (1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2} \times \frac{6}{V_{DIFF}}$	e_{NI} = 18, e_{NO} = 110	10	10
Total resolution error (ppm)			15	15
TOTAL ERROR				
Total error	Total error = sum of all error sources		3436	2634

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place 0.1-µF bypass capacitors close to the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

CMRR vs Frequency

The INA826 pinout has been optimized for achieving maximum CMRR performance over a wide range of frequencies. However, care must be taken to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, the component should be chosen so that the switch capacitance is as small as possible.

APPLICATION IDEAS

Circuit Breaker

Figure 64 shows the INA826 used in a circuit breaker application.

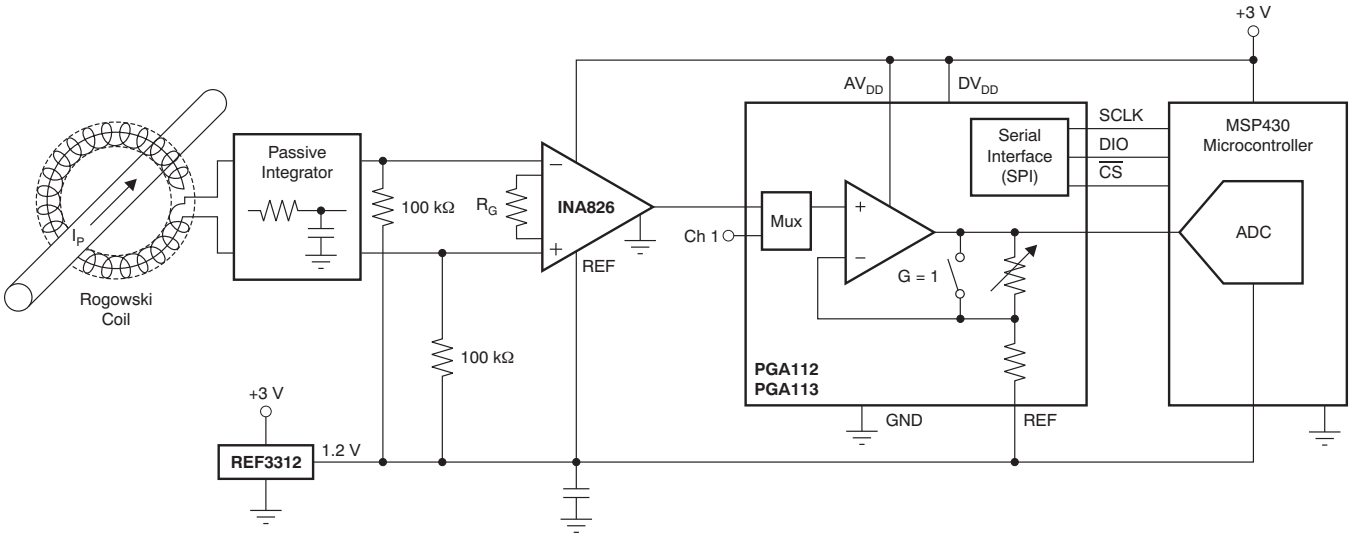


Figure 64. Circuit Breaker Example

Programmable Logic Controller (PLC) Input

The INA826 used in an example programmable logic controller (PLC) input application is shown in Figure 65.

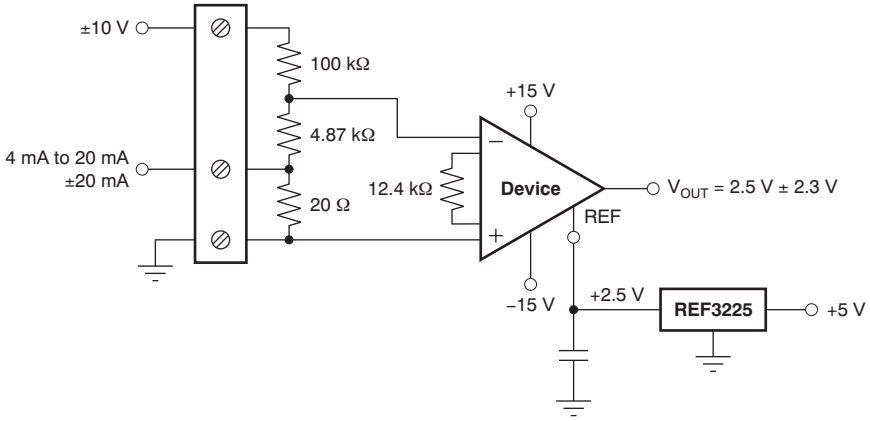


Figure 65. ±10-V, 4-mA to 20-mA PLC Input

Additional application ideas are shown in Figure 66 to Figure 70.

TINA-TI (FREE DOWNLOAD SOFTWARE)

Using TINA-TI SPICE-Based Analog Simulation Program with the INA826

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 66 and Figure 68 show example TINA-TI circuits for the INA826 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

NOTE: These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

The circuit in Figure 66 is used to convert inputs of ±10 V, ±5 V, or ±20 mA to an output voltage range from 0.5 V to 4.5 V. The input selection depends on the settings of SW_1 and SW_2. Further explanation as well as the TINA-TI simulation circuit is provided in the compressed file that can be downloaded at the following link: *PLC Circuit*.

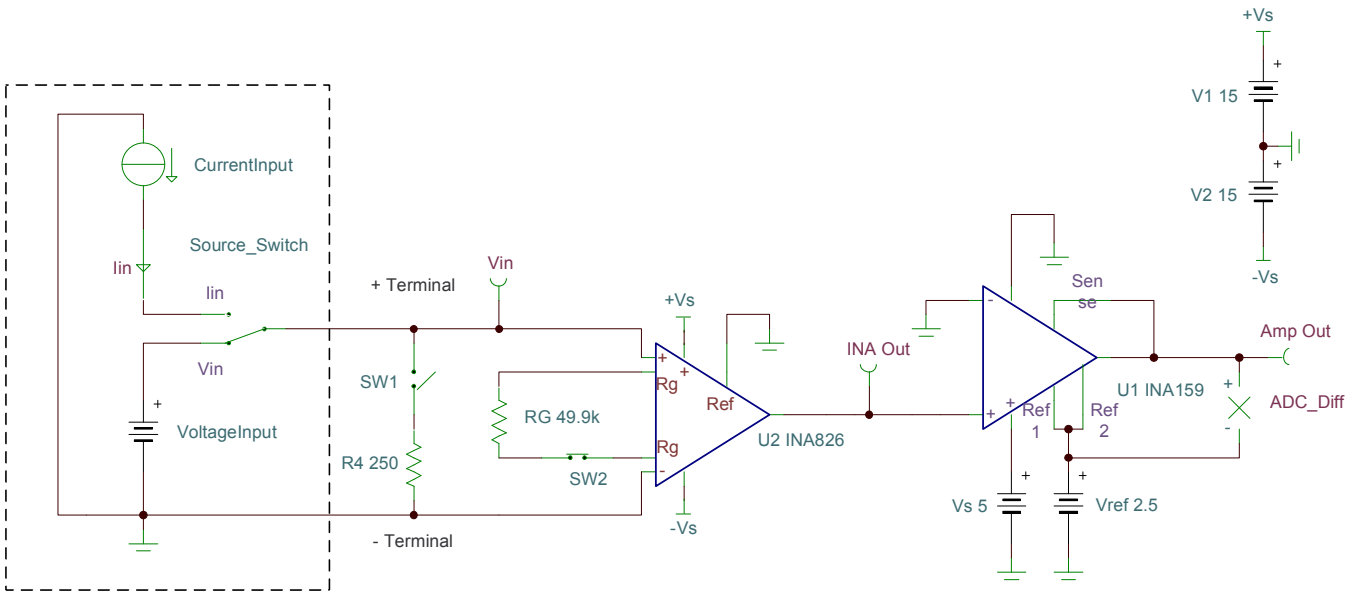


Figure 66. Two Terminal Programmable Logic Controller (PLC) Input

Figure 67 is an example of a LEAD I ECG circuit. The input signals come from leads attached to the right arm (RA) and left arm (LA). These signals are simulated with the circuitry in the corresponding boxes. Protection resistors (R_{PROT1} and R_{PROT2}) and filtering are also provided. The OPA333 is used as an integrator to remove the gained-up dc offsets and servo the INA826 outputs to V_{REF}. Finally, the right leg drive is biased to a potential ($+V_S/2$) and it inverts and amplifies the average common-mode signal back into the patient's right leg. This architecture reduces the 50-/60-Hz noise pickup. Click the following link to download the TINA-TI file: *ECG Circuit*.

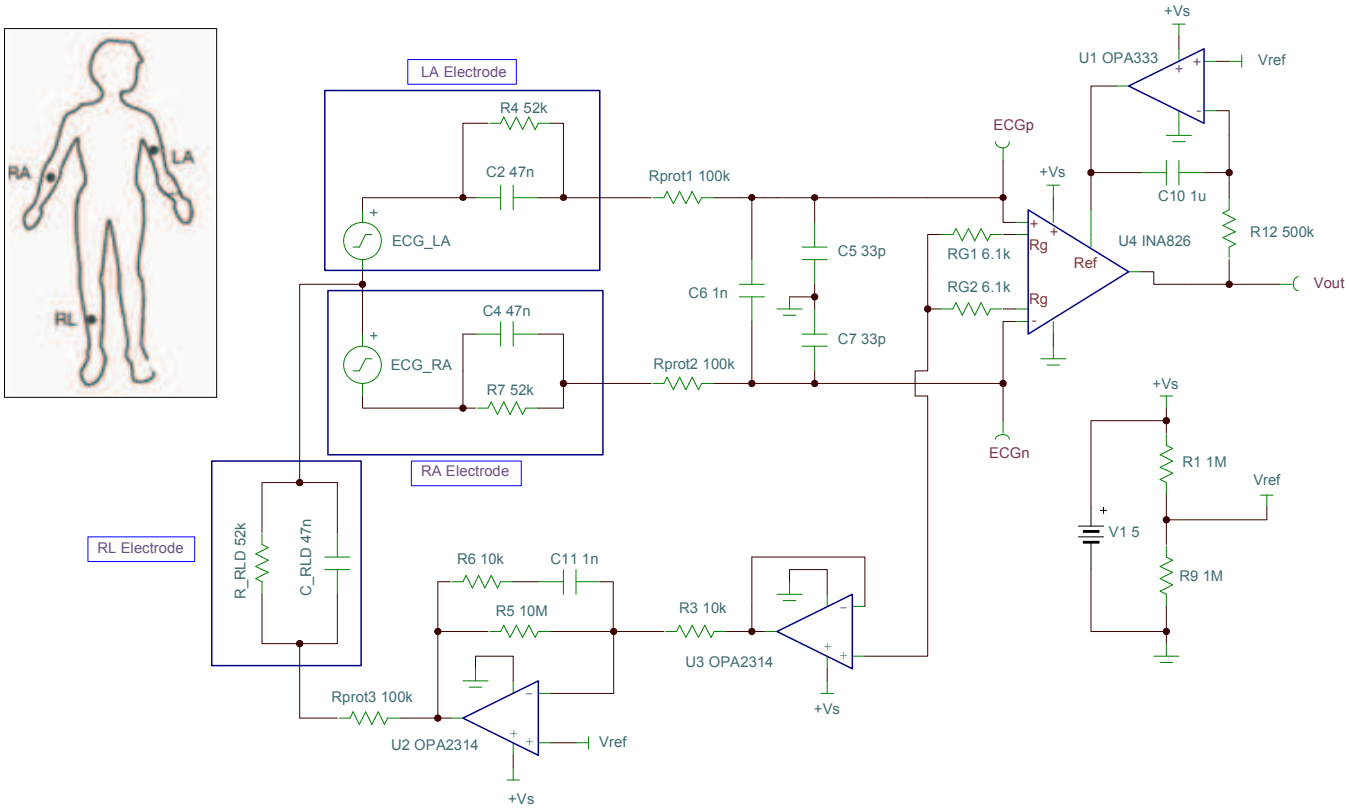


Figure 67. ECG Circuit

Figure 68 shows an example of how the INA826 can be used for low-side current sensing. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the INA826, with gain set to 100. The output swing of the INA826 is set by the common-mode voltage (which is 0 V in low-side current sensing) and power supplies. Therefore, a dual-supply circuit is implemented. The load current was set from 1 A to 10 A, which corresponds to an output voltage range from 350 mV to 3.5 V. The output range can be adjusted by changing the shunt resistor and/or the gain of the INA826. Click the following link to download the TINA-TI file: *Current Sensing Circuit*.

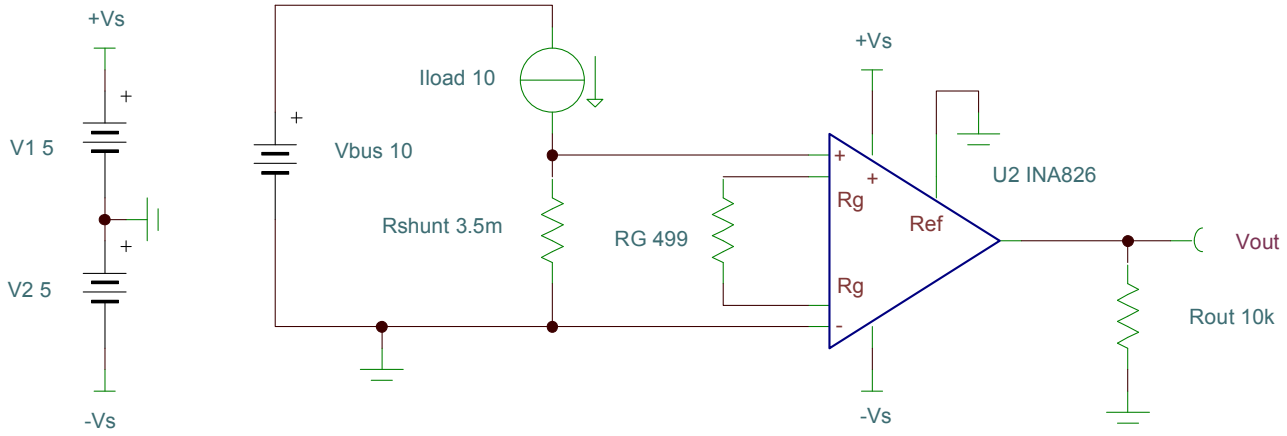


Figure 68. Low-Side Current Sensing

Figure 69 shows an example of how the INA826 can be used for RTD signal conditioning. This circuit creates an excitation current (I_{SET}) by forcing +2.5 V from the REF5025 across R_{SET}. The zero-drift, low-noise OPA188 creates the virtual ground that maintains a constant differential voltage across R_{SET} with changing common-mode voltage. This voltage is necessary because the voltage on the positive input of the INA826 fluctuates over temperature as a result of the changing RTD resistance. Click the following link to download the TINA-TI file: *RTD Circuit*.

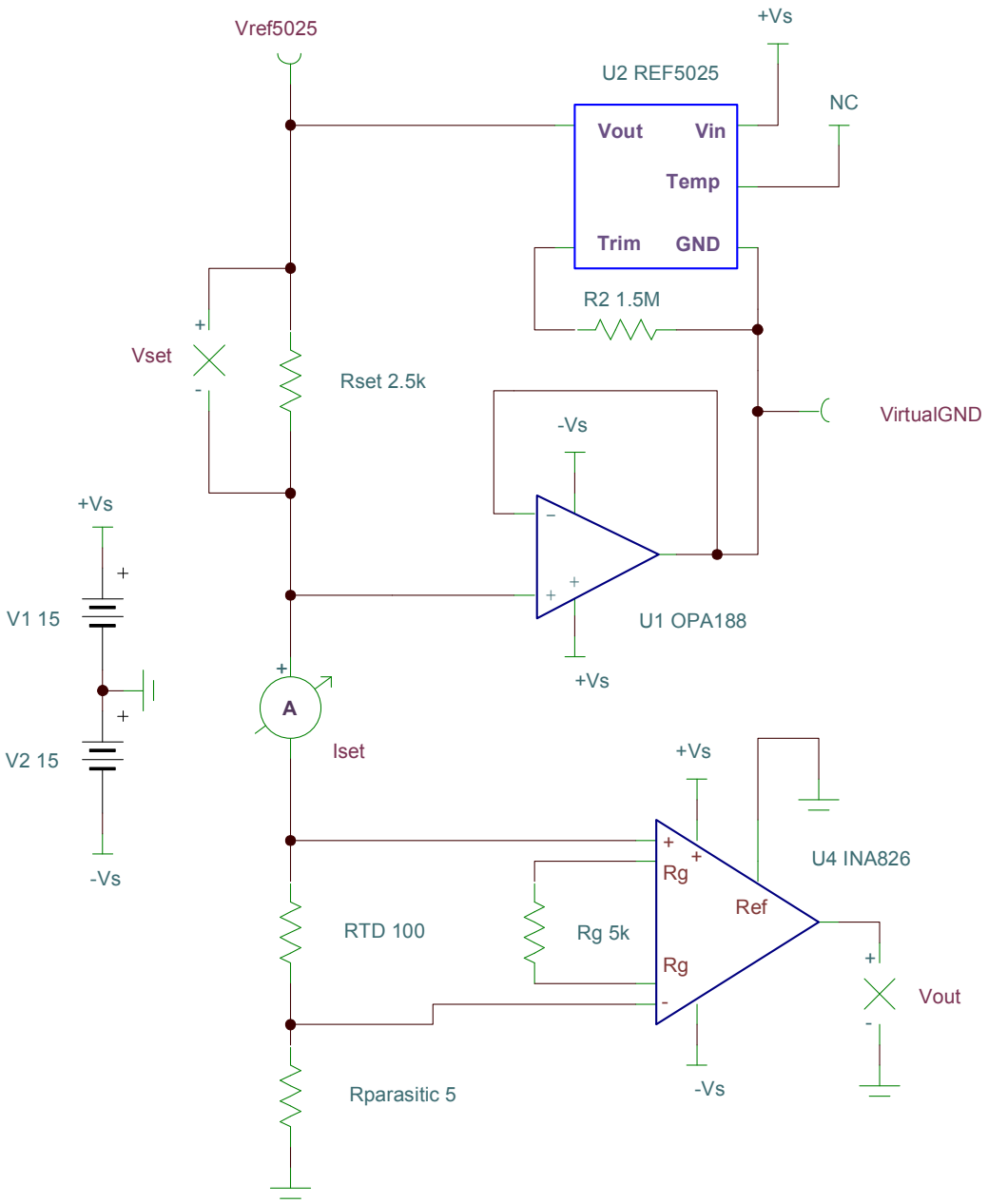


Figure 69. RTD Signal Conditioning

The circuit in Figure 70 creates a precision current I_{SET} by forcing the INA826 V_{DIFF} across R_{SET}. The input voltage V_{IN} is amplified to the output of the INA826 and then divided down by the gain of the INA826 to create V_{DIFF}. I_{SET} can be controlled either by changing the value of the gain-set resistor R_G, the set resistor R_{SET}, or by changing V_{OUT} through the gain of the composite loop. Care must be taken to ensure that the changing load resistance R_L does not create a voltage on the negative input of the INA826 that violates the compliance of the common-mode input range. Likewise, the voltage on the output of the OPA170 must remain compliant throughout the changing load resistance for this circuit to work properly. Click the following link to download the TINA-TI file: *Current Source*.

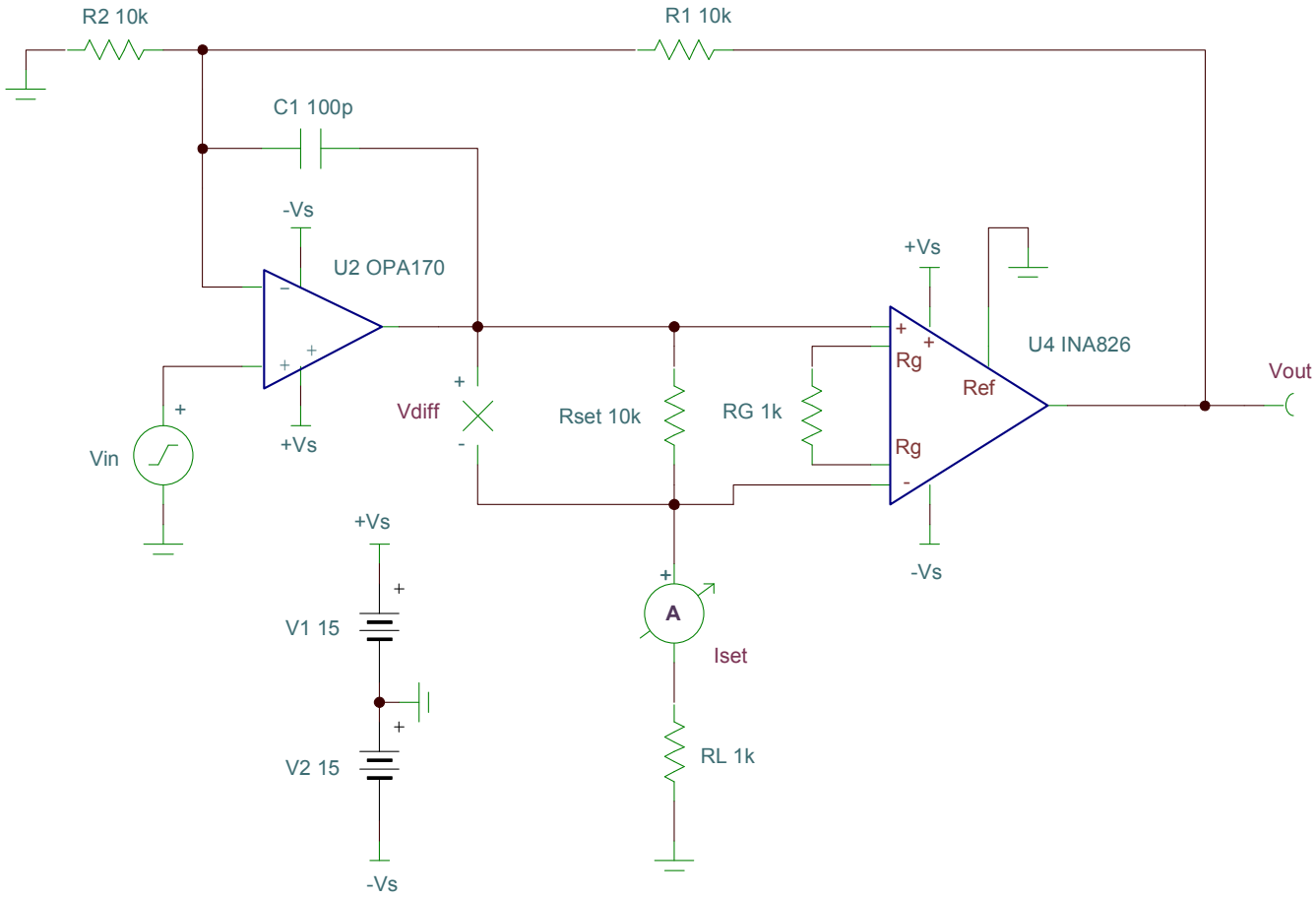


Figure 70. Precision Current Source

EVALUATION MODULE (EVM)

The INA826EVM is intended to provide basic functional evaluation of the INA826. A diagram of the INA826EVM is provided in Figure 71.

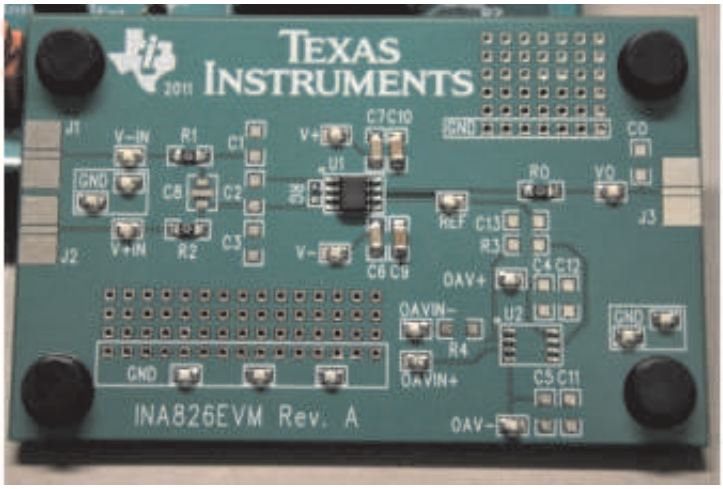


Figure 71. INA826 Evaluation Module

The INA826 provides the following features:

- Intuitive evaluation with silkscreen schematic
- Easy access to nodes with surface-mount test points
- Advanced evaluation with two prototype areas
- Reference voltage source flexibility
- Convenient input and output filtering

The *INA826EVM User Guide* (SBOU115) available for download at www.ti.com provides instructions on how to set up the device for dual- and single-supply operation. The user guide also includes schematics, layout, and a bill of material (BOM).

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E **Page**

- Deleted package marking column from Package/Ordering Information table 2

Changes from Revision C (March 2012) to Revision D **Page**

- Changed Input voltage range parameter specification value in *Absolute Maximum Ratings* table 2

Changes from Revision B (December 2011) to Revision C **Page**

- Changed product status from Mixed Status to Production Data 1
- Changed DFN-8 package to production data 2
- Deleted gray shading and footnote 2 from Package/Ordering Information table 2

Changes from Revision A (September 2011) to Revision B **Page**

- Deleted gray from SO-8 row in Package/Ordering Information 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA826AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826	Samples
INA826AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI	Samples
INA826AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI	Samples
INA826AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826	Samples
INA826AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI	Samples
INA826AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

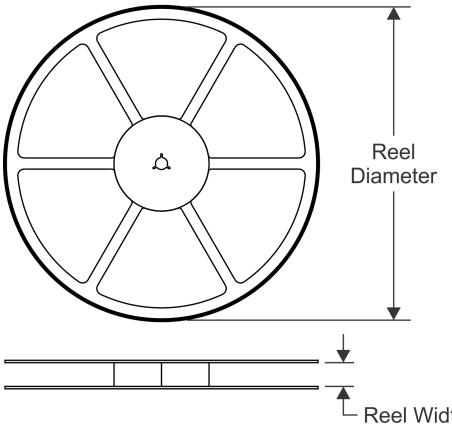
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

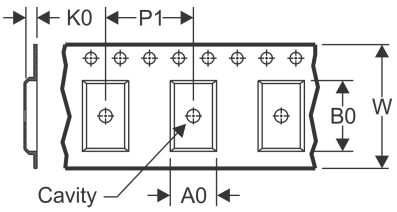
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

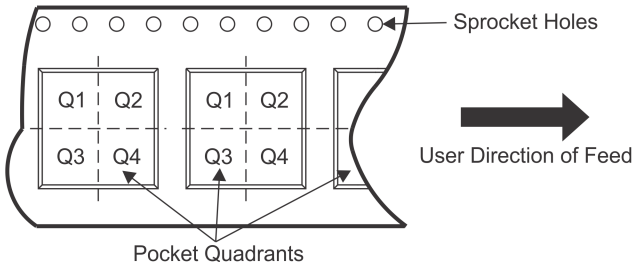


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

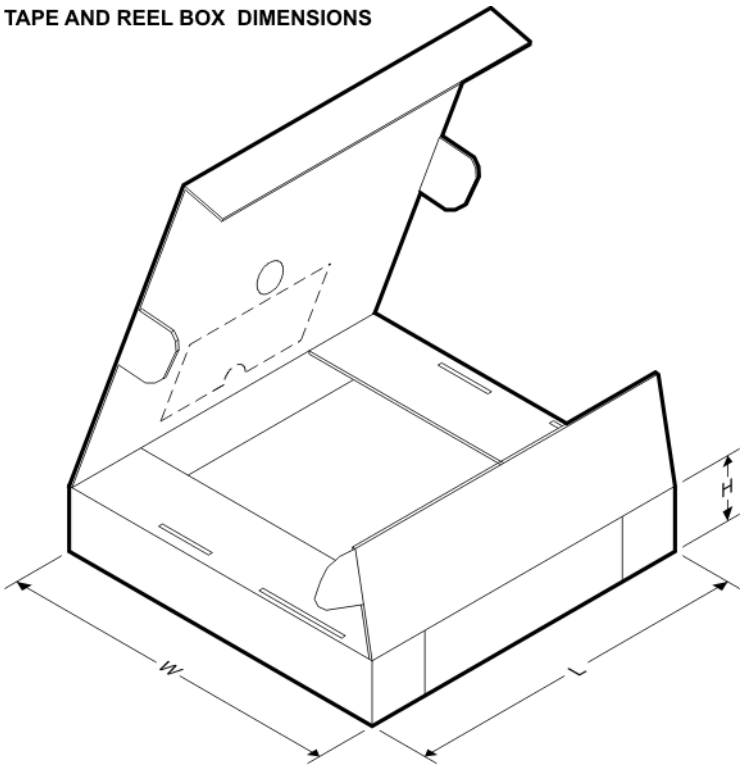
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA826AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA826AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA826AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA826AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

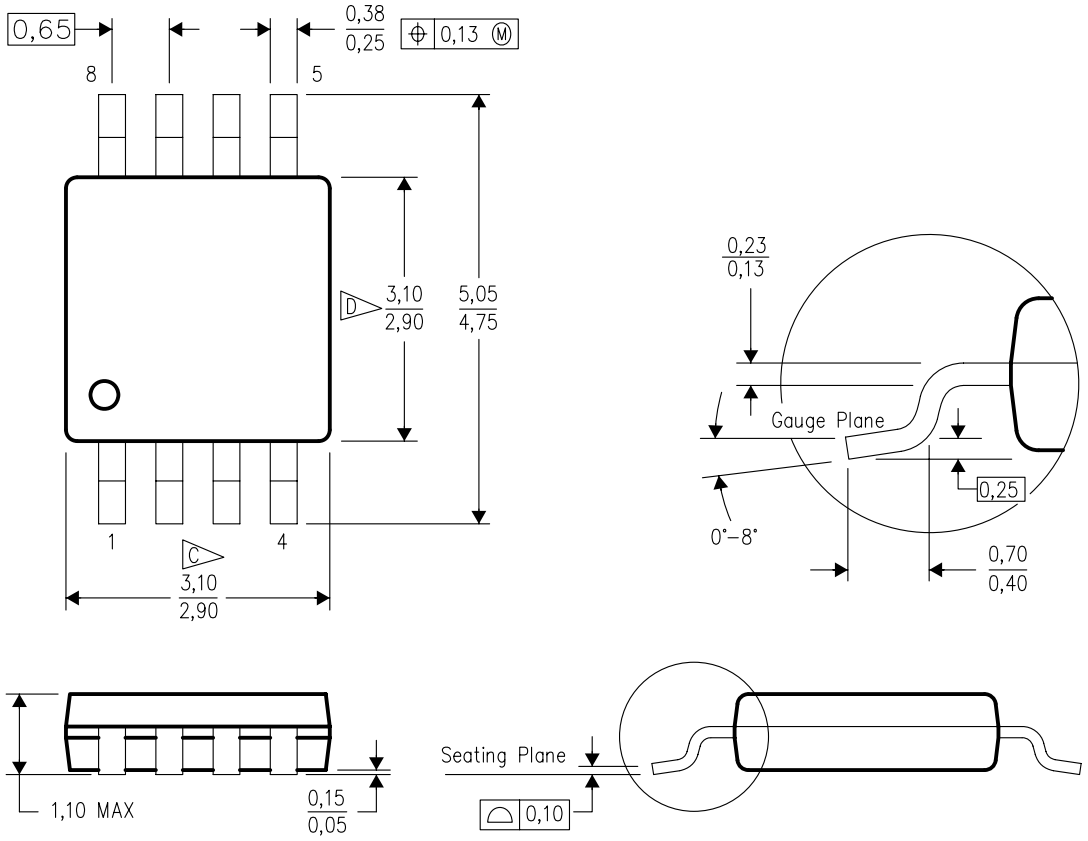
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA826AIDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
INA826AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA826AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
INA826AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

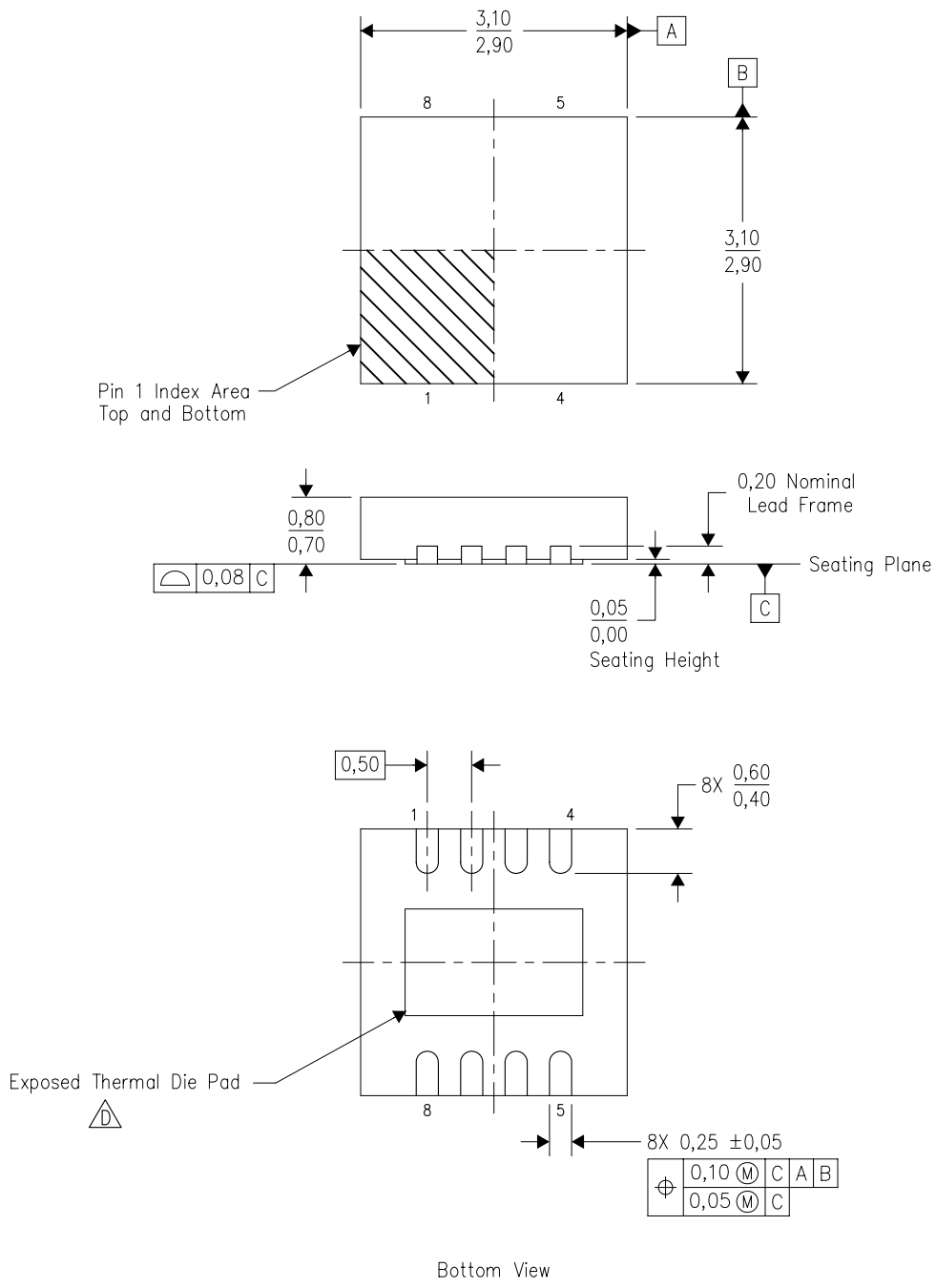
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

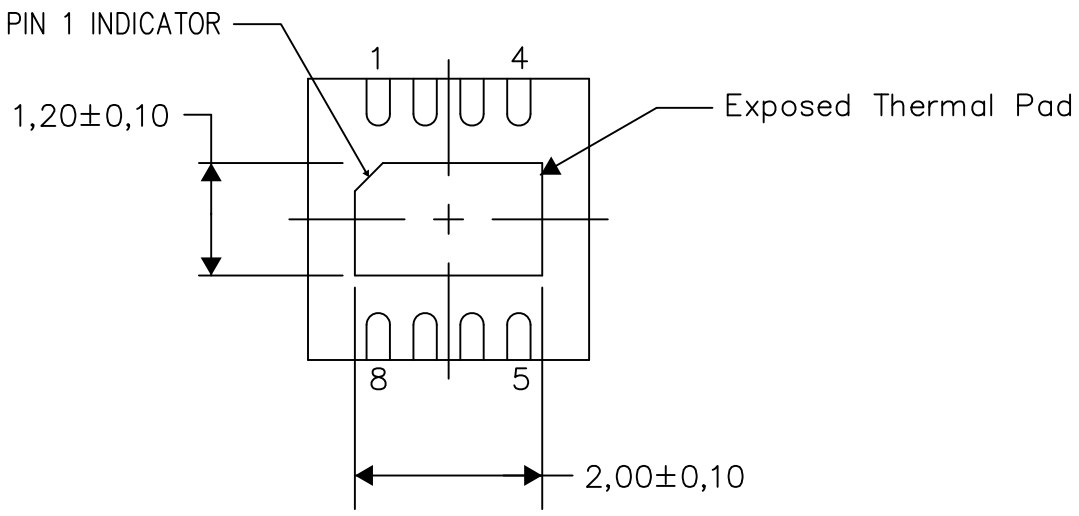
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



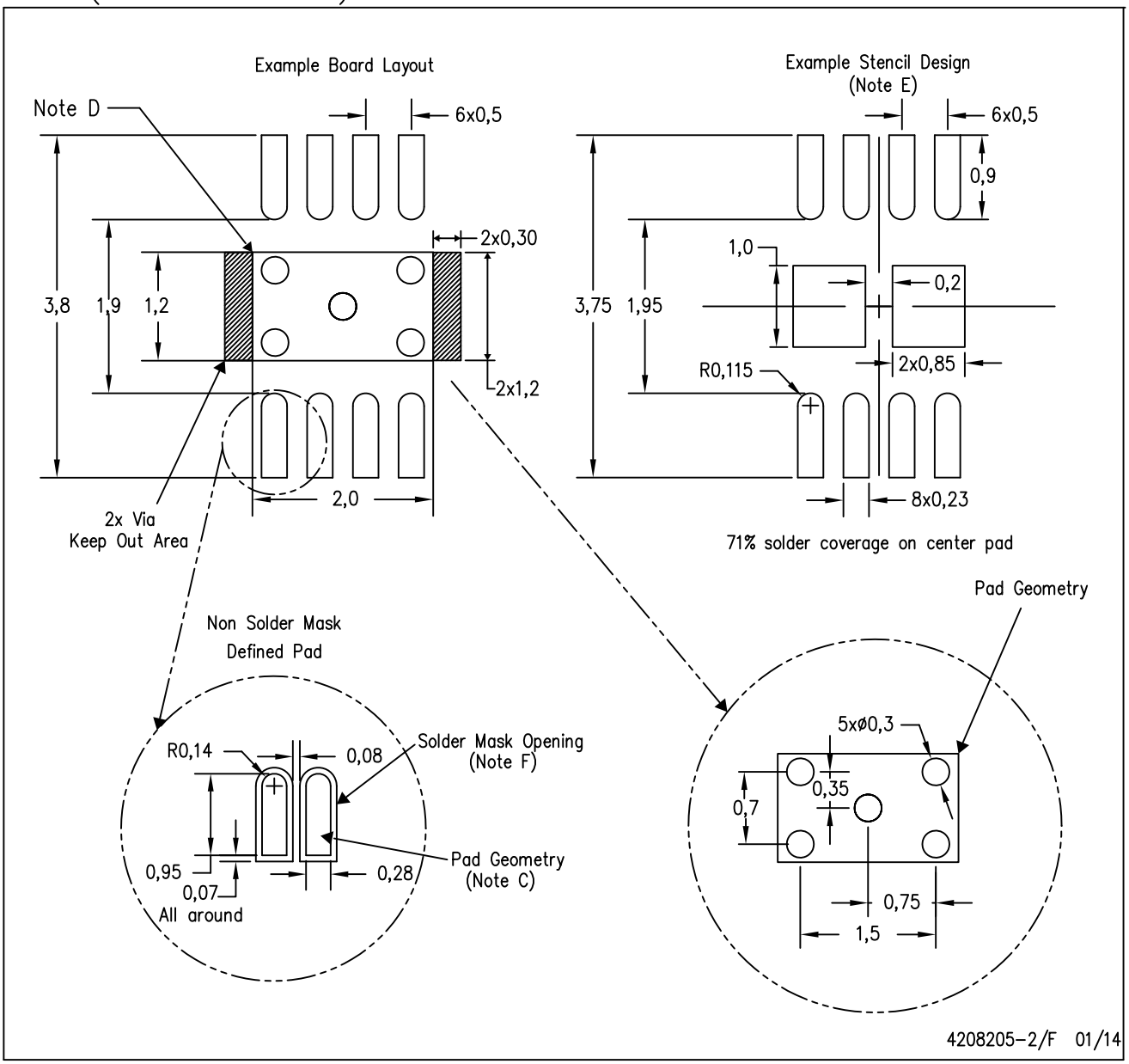
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/H 12/13

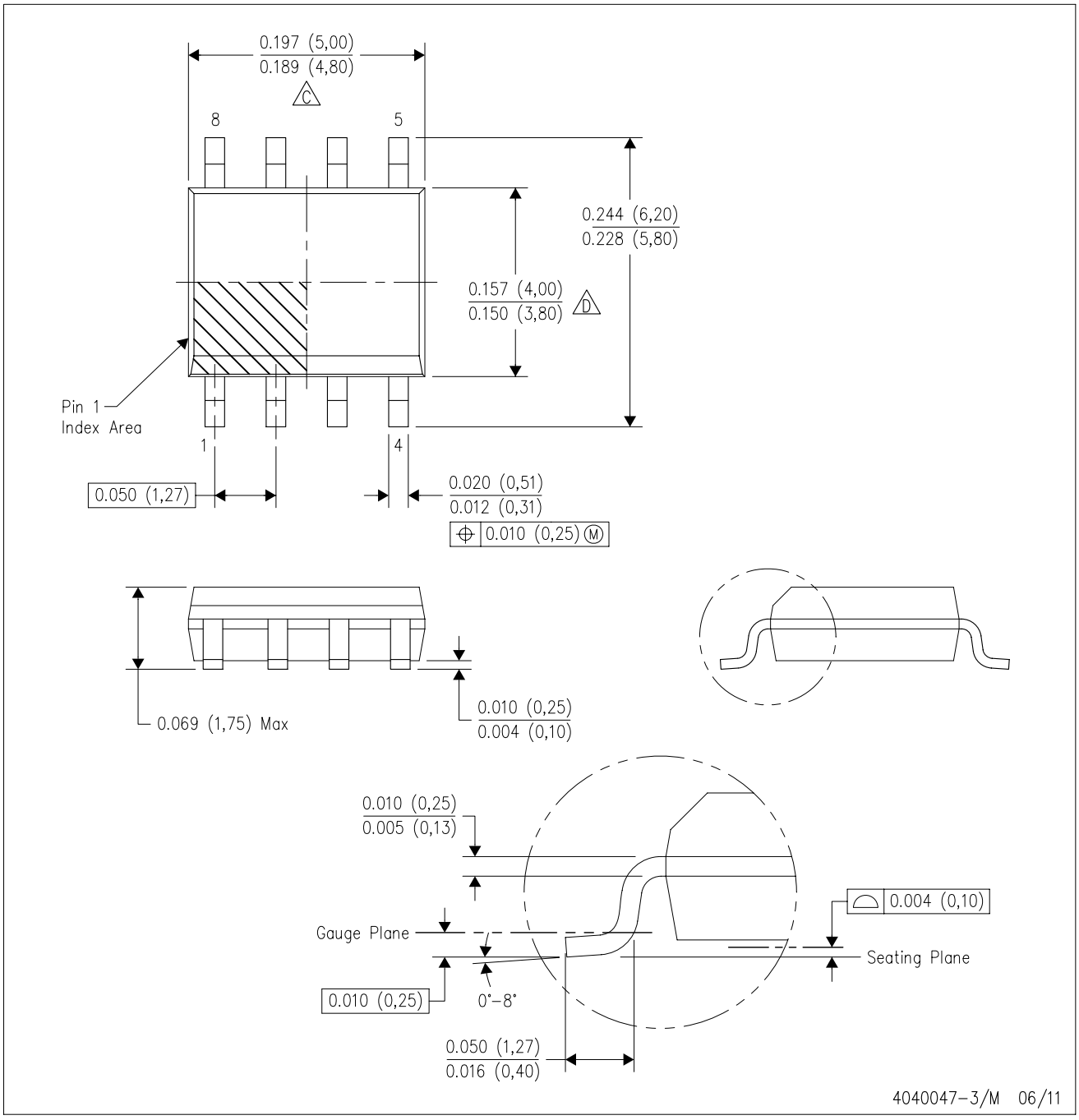
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



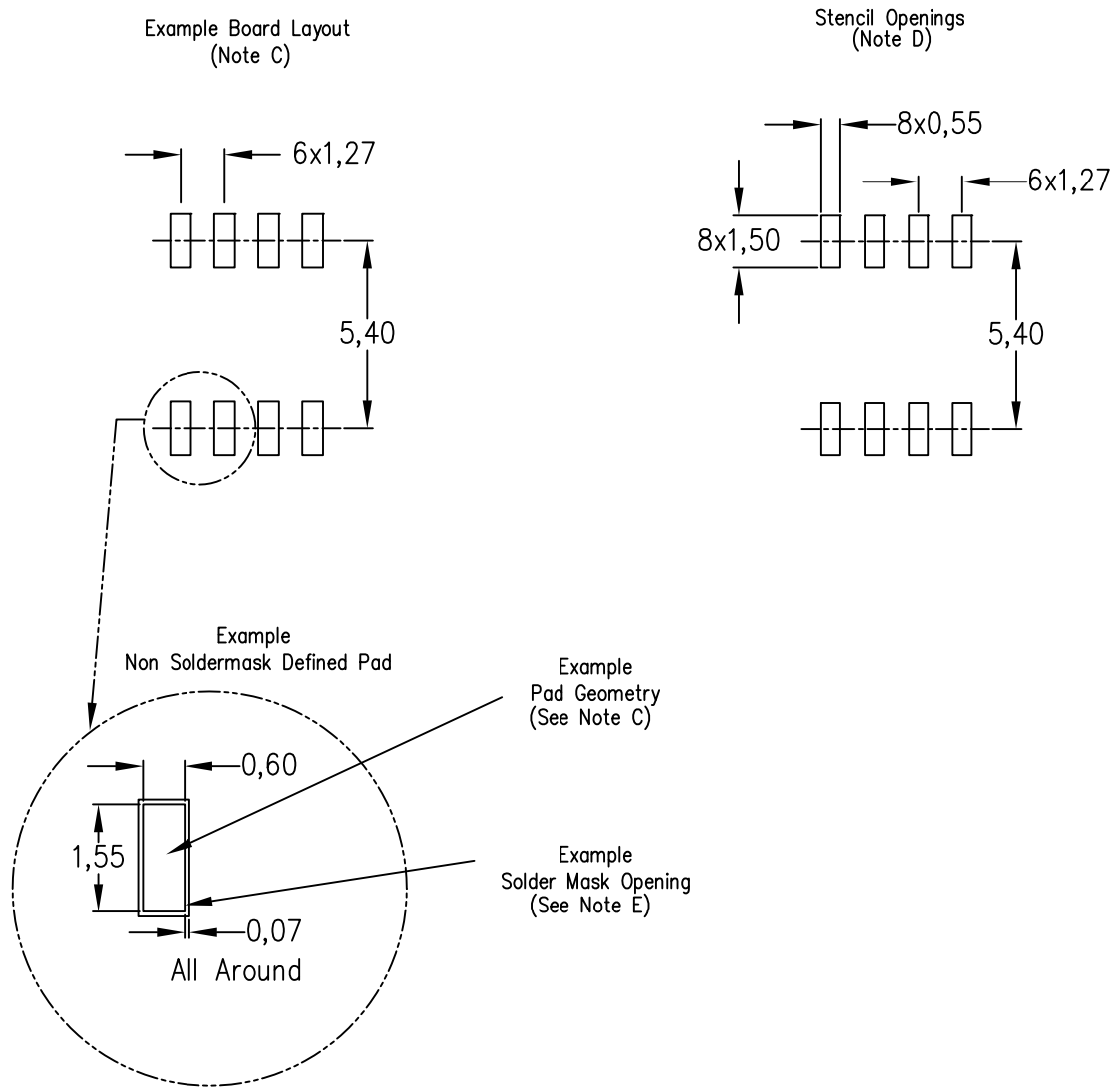
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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