OPA373, OPA2373
OPA374
OPA2374, OPA4374

SBOS279E − SEPTEMBER 2003 − REVISED MAY 2008

6.5MHz, 585μA, Rail-to-Rail I/O CMOS Operational Amplifier

FEATURES

- LOW OFFSET: 5mV (max)
- LOW I_B: 10pA (max)
- HIGH BANDWIDTH: 6.5MHz
- RAIL-TO-RAIL INPUT AND OUTPUT
- SINGLE SUPPLY: +2.3V to +5.5V
- SHUTDOWN: OPAx373
- SPECIFIED UP TO +125°C
- *Micro*SIZE PACKAGES: SOT23-5, SOT23-6, SOT23-8 and DFN-10

APPLICATIONS

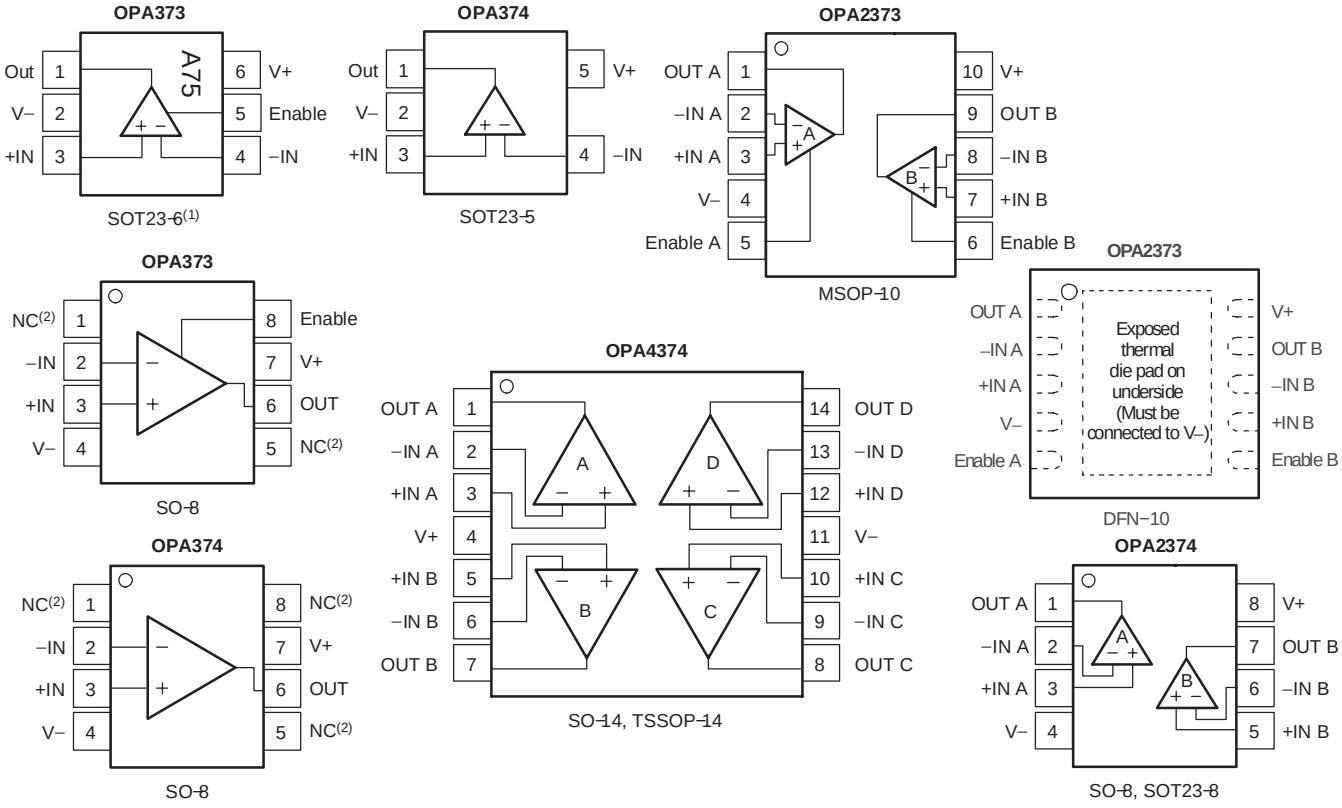
- PORTABLE EQUIPMENT
- BATTERY-POWERED DEVICES
- ACTIVE FILTERS
- DRIVING A/D CONVERTERS

DESCRIPTION

The OPA373 and OPA374 families of operational amplifiers are low power and low cost with excellent bandwidth (6.5MHz) and slew rate (5V/μs). The input range extends 200mV beyond the rails and the output range is within 25mV of the rails. The speed/power ratio and small size make them ideal for portable and battery-powered applications.

The OPA373 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is less than 1μA.

The OPA373 and OPA374 families of operational amplifiers are specified for single or dual power supplies of +2.7V to +5.5V, with operation from +2.3V to +5.5V. All models are specified for −40°C to +125°C.



(1) Pin 1 of the SOT23-6 is determined by orienting the package marking as shown.
(2) NC indicates no internal connection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown						
OPA373	SOT23-6	DBV	−40°C to +125°C	A75	OPA373AIDBVT	Tape and Reel, 250
″	″	″	″	″	OPA373AIDBVR	Tape and Reel, 3000
OPA373	SO-8	D	−40°C to +125°C	OPA373A	OPA373AID	Rails, 100
″	″	″	″	″	OPA373AIDR	Tape and Reel, 2500
OPA2373	MSOP-10	DGS	−40°C to +125°C	AYO	OPA2373AIDGST	Tape and Reel, 250
″	″	″	″	″	OPA2373AIDGSR	Tape and Reel, 2500
OPA2373	DFN-10	DRC	−40°C to +125°C	OCEQ	OPA2373AIDRCT	Tape and Reel, 250
″	″	″	″	″	OPA2373AIDRCR	Tape and Reel, 3000
Non-Shutdown						
OPA374	SOT23-5	DBV	−40°C to +125°C	A76	OPA374AIDBVT	Tape and Reel, 250
″	″	″	″	″	OPA374AIDBVR	Tape and Reel, 3000
OPA374	SO-8	D	−40°C to +125°C	OPA274A	OPA374AID	Rails, 100
″	″	″	″	″	OPA374AIDR	Tape and Reel, 2500
OPA2374	SOT23-8	DCN	−40°C to +125°C	ATP	OPA2374AIDCNT	Tape and Reel, 250
″	″	″	″	″	OPA2374AIDCNR	Tape and Reel, 3000
OPA2374	SO-8	D	−40°C to +125°C	OPA2374A	OPA2374AID	Rails, 100
″	″	″	″	″	OPA2374AIDR	Tape and Reel, 2500
OPA4374	SO-14	D	−40°C to +125°C	OPA4374A	OPA4374AID	Rails, 58
″	″	″	″	″	OPA4374AIDR	Tape and Reel, 2500
OPA4374	TSSOP-14	PW	−40°C to +125°C	OPA4374A	OPA4374AIPWT	Tape and Reel, 250
″	″	″	″	″	OPA4374AIPWR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7.0V
Signal Input Terminals, Voltage(2)	−0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA373, OPA2373, OPA374, OPA2374, OPA4374 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		1	5	mV
over Temperature					**6.5**	**mV**
Drift	**dV_{OS}/dT**			**3**		**µV/°C**
vs Power Supply	PSRR	V_S = 2.7V to 5.5V, V_{CM} < (V+) − 2V		25	100	µV/V
over Temperature		**V_S = 2.7V to 5.5V, V_{CM} < (V+) − 2V**			**150**	**µV/V**
Channel Separation, DC				0.4		µV/V
f = 1kHz				128		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2		(V+) + 0.2	V
Common-Mode Rejection Ratio	CMRR	(V−) − 0.2V < V_{CM} < (V+) − 2V	80	90		dB
over Temperature		**(V−) − 0.2V < V_{CM} < (V+) − 2V**	**70**			**dB**
		V_S = 5.5V, (V−) − 0.2V < V_{CM} < (V+) + 0.2V	66			dB
over Temperature		**V_S = 5.5V, (V−) − 0.2V < V_{CM} < (V+) + 0.2V**	60			**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±10	pA
Input Offset Current	I_{OS}			±0.5	±10	pA
INPUT IMPEDANCE						
Differential				10^{13} ||3		Ω ||pF
Common-Mode				10^{13} ||6		Ω ||pF
NOISE		V_{CM} < (V+) − 2V				
Input Voltage Noise, f = 0.1Hz to 10Hz				10		μV_{PP}
Input Voltage Noise Density, f = 10kHz	e_n			15		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 10kHz	i_n			4		$fA/\sqrt{Hz}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_S = 5V, R_L = 100kΩ, 0.025V < V_O < 4.975V	94	110		dB
over Temperature		**V_S = 5V, R_L = 100kΩ, 0.025V < V_O < 4.975V**	**80**			**dB**
		V_S = 5V, R_L = 5kΩ, 0.125V < V_O < 4.875V	94	106		dB
over Temperature		**V_S = 5V, R_L = 5kΩ, 0.125V < V_O < 4.875V**	**80**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ		18	25	mV
over Temperature		**R_L = 100kΩ**			**25**	**mV**
		R_L = 5kΩ		100	125	mV
over Temperature		**R_L = 5kΩ**			**125**	**mV**
Short-Circuit Current	I_{SC}		See Typical Characteristics			
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
Open-Loop Output Impedance		f = 1MHz, I_O = 0		220		Ω
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW			6.5		MHz
Slew Rate	SR	G = +1		5		V/µs
Settling Time, 0.1%	t_S	V_S = 5V, 2V Step, G = +1		1		µs
0.01%		V_S = 5V, 2V Step, G = +1		1.5		µs
Overload Recovery Time		V_{IN} • Gain > V_S		0.3		µs
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.0013		%
ENABLE/SHUTDOWN						
t_{OFF}				3		µs
t_{ON}				12		µs
V_L (shutdown)			V−		(V−) + 0.8	V
V_H (amplifier is active)			(V−) + 2		V+	V
Input Bias Current of Enable Pin				0.2		µA
I_{QSD} (per amplifier)				< 0.5	1	µA

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

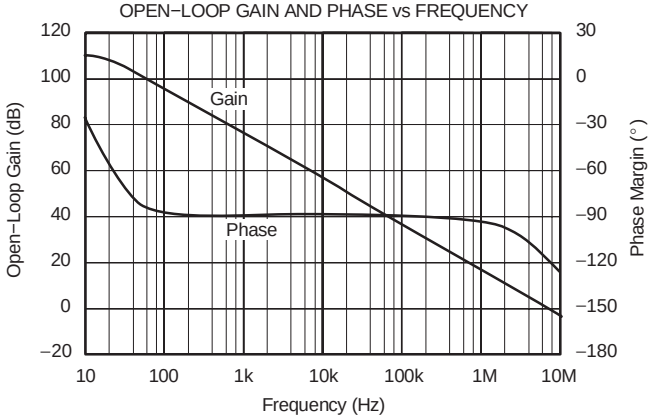
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA373, OPA2373, OPA374, OPA2374, OPA4374 MIN	TYP	MAX	UNIT
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Operating Voltage Range				2.3 to 5.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		585	750	µA
over Temperature					**800**	µ**A**
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−55		+150	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5, SOT23-6, SOT23-8				200		°C/W
MSOP-10, SO-8				150		°C/W
SO-14, TSSOP-14				100		°C/W
DFN-10		JEDEC High-K Board		56		°C/W

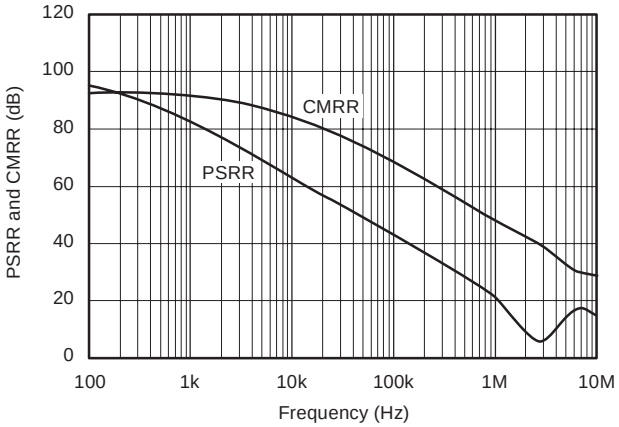
TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

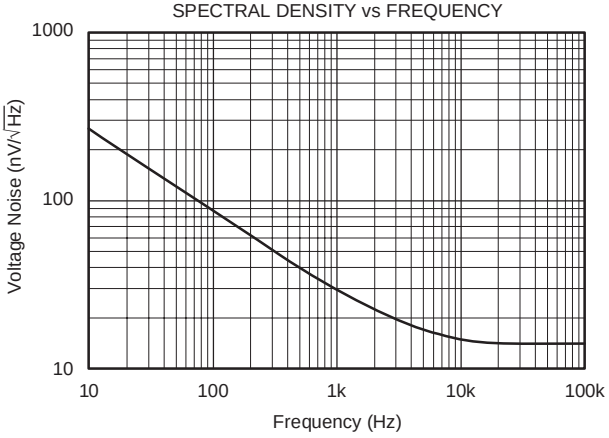
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



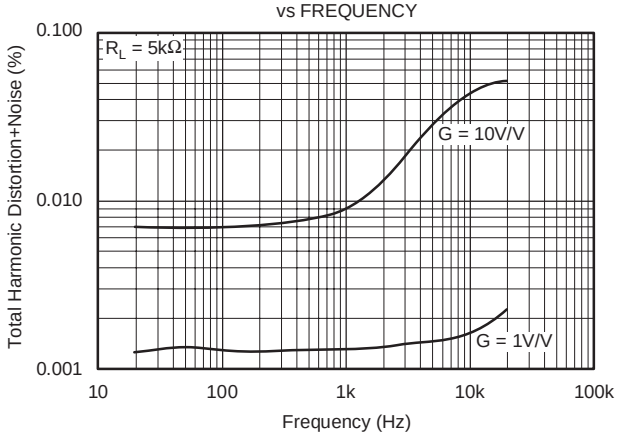
POWER−SUPPLY AND COMMON−MODE REJECTION RATIO vs FREQUENCY



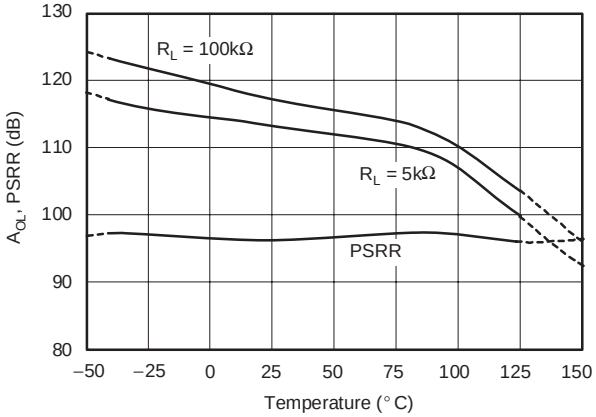
INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



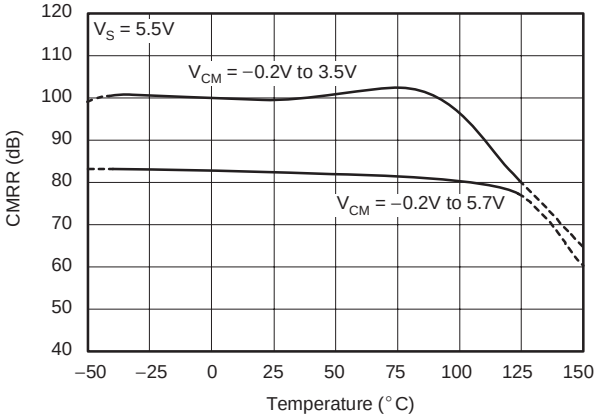
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



OPEN−LOOP GAIN AND POWER−SUPPLY REJECTION RATIO vs TEMPERATURE



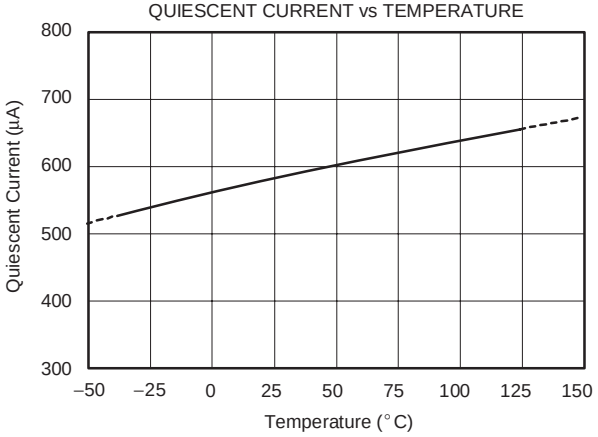
COMMON−MODE REJECTION RATIO vs TEMPERATURE



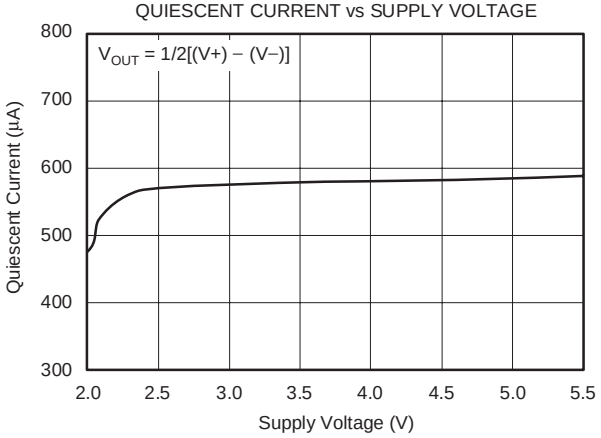
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

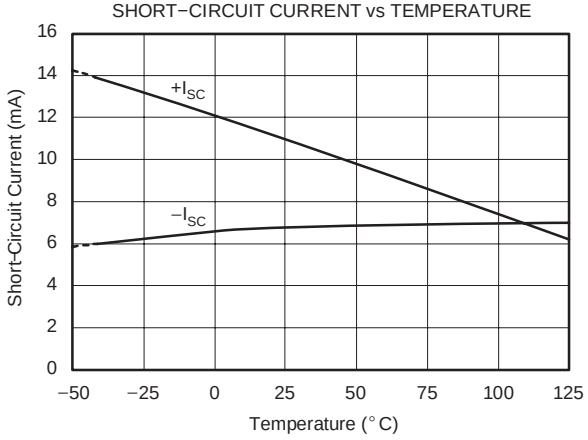
QUIESCENT CURRENT vs TEMPERATURE



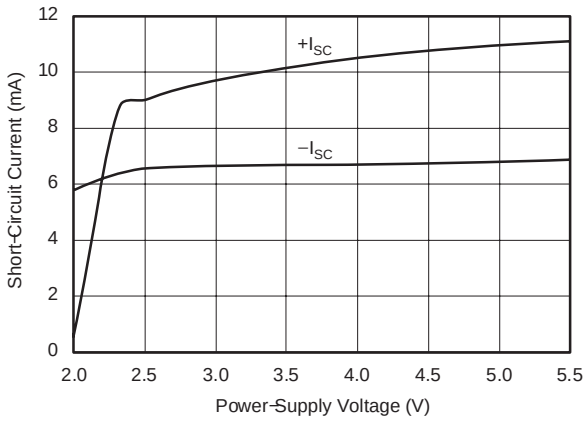
QUIESCENT CURRENT vs SUPPLY VOLTAGE



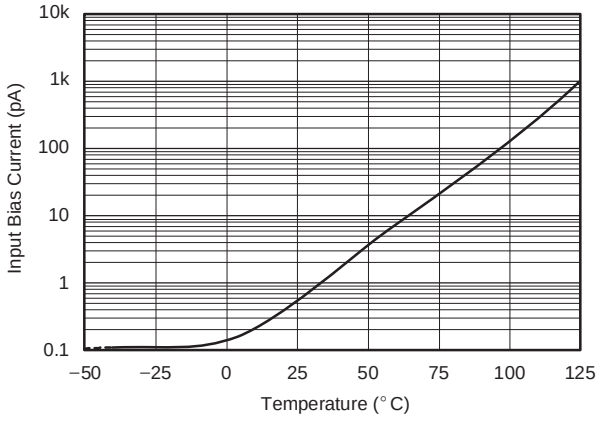
SHORT−CIRCUIT CURRENT vs TEMPERATURE



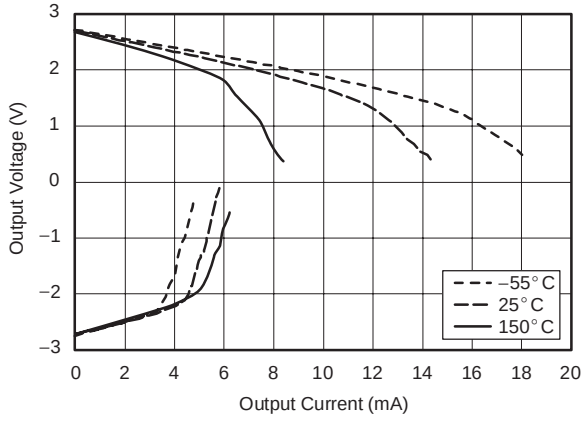
CONTINUOUS SHORT−CIRCUIT CURRENT vs POWER−SUPPLY VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



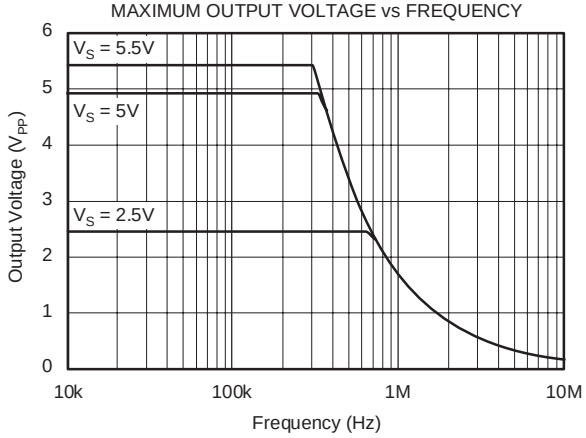
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



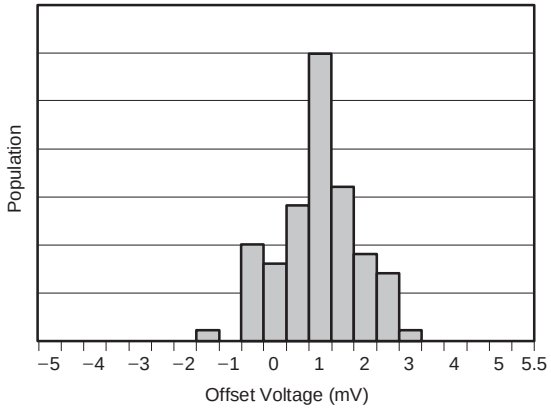
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

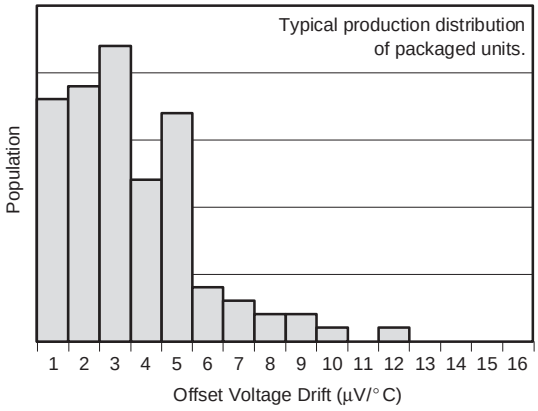
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



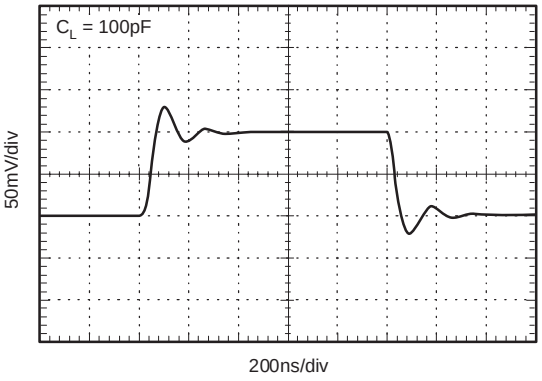
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



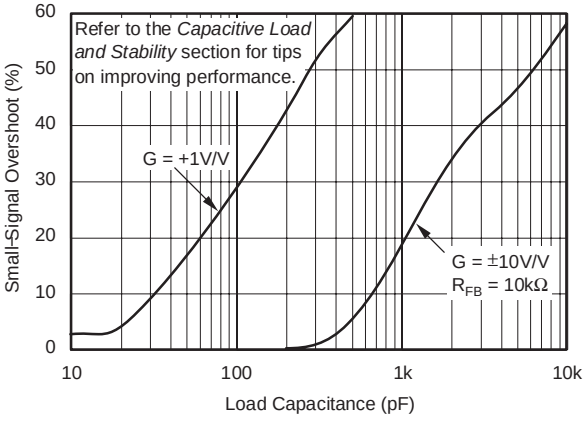
OFFSET VOLTAGE DRIFT MAGNITUDE
PRODUCTION DISTRIBUTION



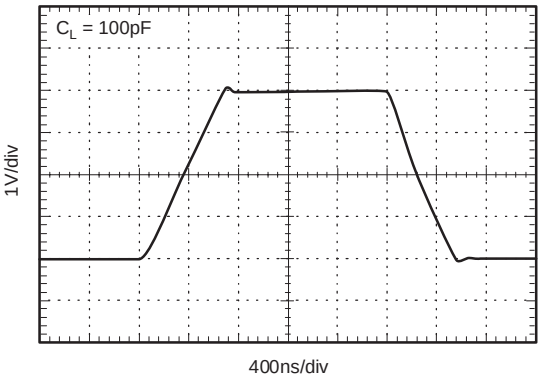
SMALL−SIGNAL STEP RESPONSE



SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



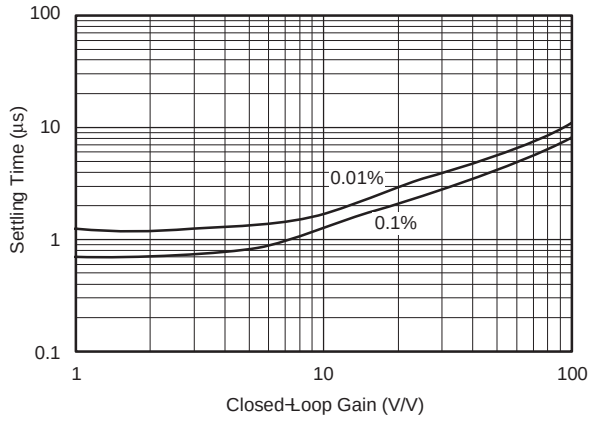
LARGE −SIGNAL STEP RESPONSE



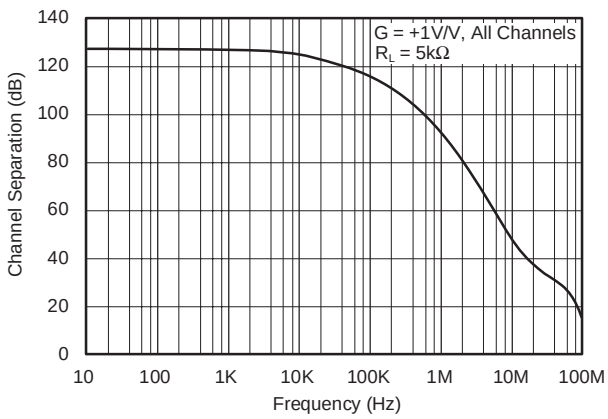
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

SETTLING TIME vs CLOSED−LOOP GAIN



CHANNEL SEPARATION vs FREQUENCY



APPLICATIONS

The OPA373 and OPA374 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input and output make them ideal for driving sampling Analog-to-Digital Converters (ADCs). Excellent ac performance makes them well-suited for audio applications. The class AB output stage is capable of driving 100kΩ loads connected to any point between V+ and ground.

The input common-mode voltage range includes both rails, allowing the OPA373 and OPA374 series op amps to be used in virtually any single-supply application up to a supply voltage of +5.5V.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications.

Power-supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA373 and OPA374 op amps are specified and tested over a power-supply range of +2.7V to +5.5V (±1.35V to ±2.75V). However, the supply voltage may range from +2.3V to +5.5V (±1.15V to ±2.75V). Supply voltages higher than 7.0V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA373 and OPA374 series extends 200mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.65V to 200mV above the positive supply, while the P-channel pair is on for inputs from 200mV below the negative supply to approximately (V+) − 1.65V. There is a 500mV transition region, typically (V+) − 1.9V to (V+) − 1.4V, in which both pairs are on. This 500mV transition region, shown in Figure 1, can vary ±300mV with process variation. Thus, the transition region (both stages on) can range from (V+) − 2.2V to (V+) − 1.7V on the low end, up to (V+) − 1.6V to (V+) − 1.1V on the high end. Within the 500mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

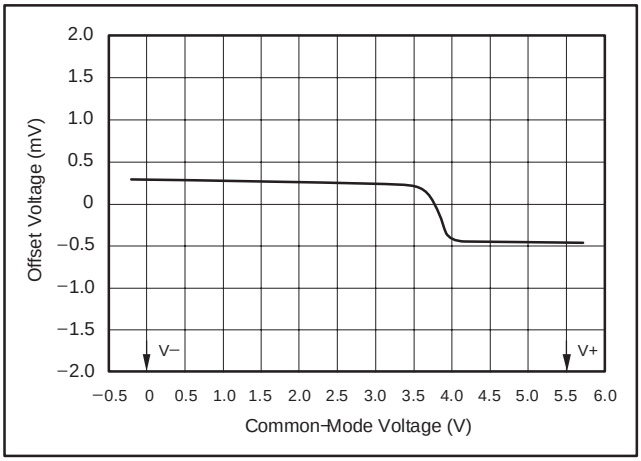


Figure 1. Behavior of Typical Transition Region at Room Temperature

RAIL-TO-RAIL INPUT

The input common-mode range extends from (V−) − 0.2V to (V+) + 0.2V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op amp. Unlike some other op amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 2.

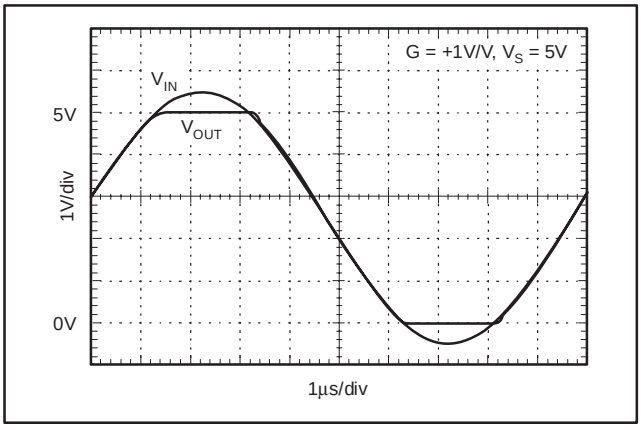


Figure 2. OPA373: No Phase Inversion with Inputs Greater Than the Power-Supply Voltage

Normally, input bias current is approximately 500fA; however, input voltages exceeding the power supplies by more than 500mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor; see Figure 3. (Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.)

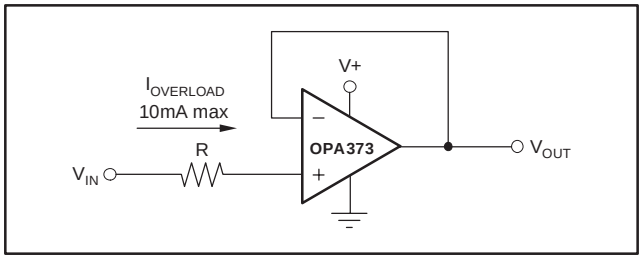


Figure 3. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 100kΩ), the output voltage can typically swing to within 18mV from the supply rails. With moderate resistive loads (5kΩ to 50kΩ), the output can typically swing to within 100mV from the supply rails and maintain high open-loop gain. See the Typical Characteristic curve, *Output Voltage Swing vs Output Current*, for more information.

CAPACITIVE LOAD AND STABILITY

OPA373 series op amps can drive a wide range of capacitive loads. However, under certain conditions, all op amps may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. The OPA373 series op amps perform well in unity-gain configuration, with a pure capacitive load up to approximately 250pF. Increased gains allow the amplifier to drive more capacitance. See the Typical Characteristics curve, *Small-Signal Overshoot vs Capacitive Load*, for further details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 4. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. When there is a resistive load in parallel with the capacitive load, R_S must be placed within the feedback loop as shown to allow the feedback loop to compensate for the voltage divider created by R_S and R_L.

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. However, when large valued resistors cannot be avoided, a small (4pF to 6pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 5. This significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance and printed circuit board (PCP) parasitic capacitance.

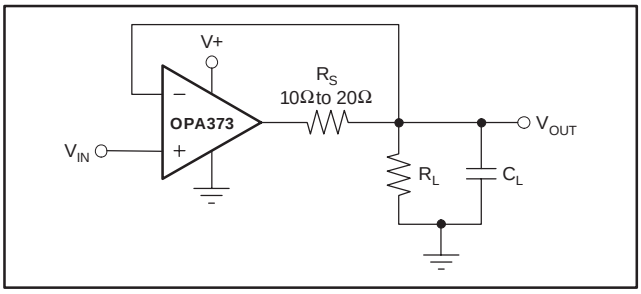


Figure 4. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

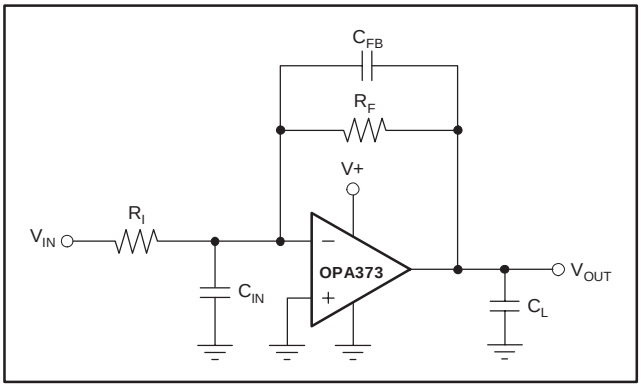


Figure 5. Improving Capacitive Load Drive

For example, when driving a 100pF load in unity-gain inverter configuration, adding a 6pF capacitor in parallel with the 10kΩ feedback resistor decreases overshoot from 57% to 12%, as shown in Figure 6.

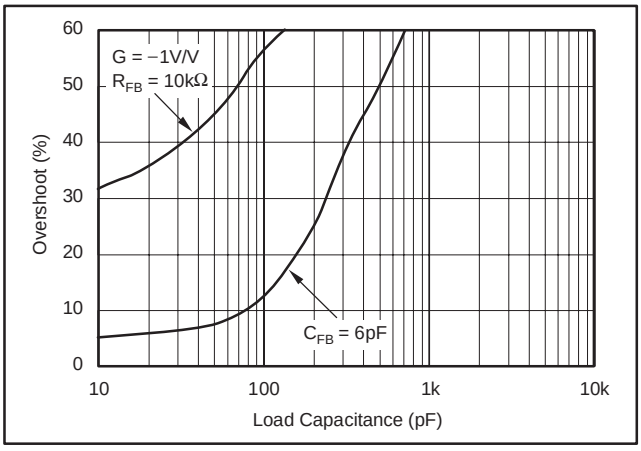


Figure 6. Improving Capacitive Load Drive

DRIVING ADCs

The OPA373 and OPA374 series op amps are optimized for driving medium-speed sampling ADCs. The OPA373 and OPA374 op amps buffer the ADC input capacitance and resulting charge injection, while providing signal gain.

The OPA373 is shown driving the ADS7816 in a basic noninverting configuration, as shown in Figure 7. The ADS7816 is a 12-bit, *Micro*Power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA373, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide anti-aliasing filtering.

Figure 8 shows the OPA373 driving the ADS7816 in a speech band-pass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with V_S = 2.7V to 5V.

The OPA373 is shown in the inverting configuration described in Figure 9. In this configuration, filtering may be accomplished with the capacitor across the feedback resistor.

ENABLE/SHUTDOWN

OPA373 and OPA374 series op amps typically require 585µA quiescent current. The enable/shutdown feature of the OPA373 allows the op amp to be shut off in order to reduce this current to less than 1µA.

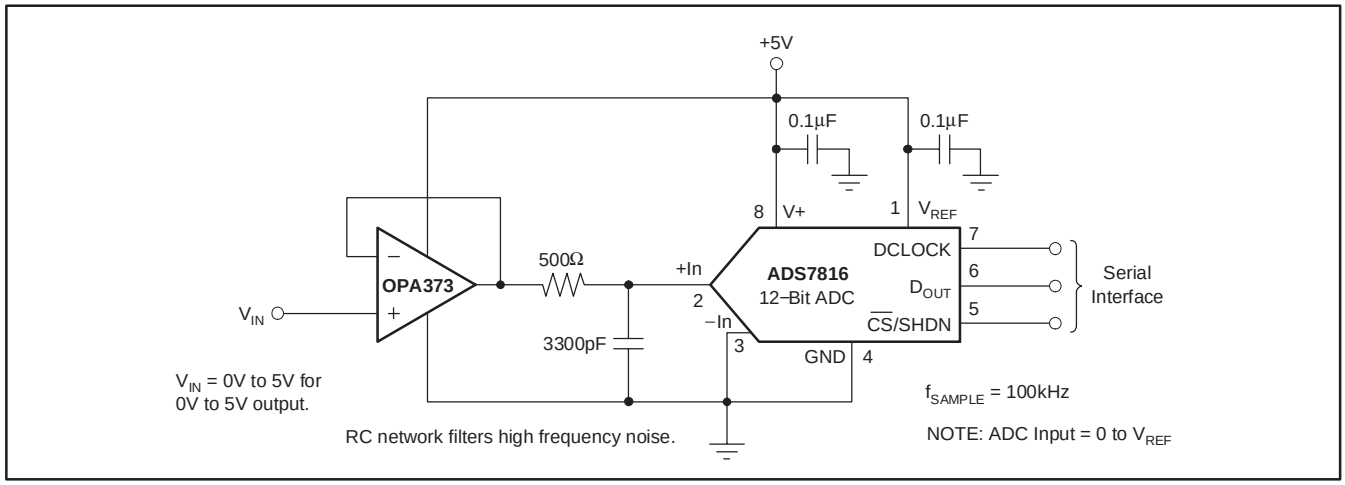


Figure 7. The OPA373 in Noninverting Configuration Driving the ADS7816

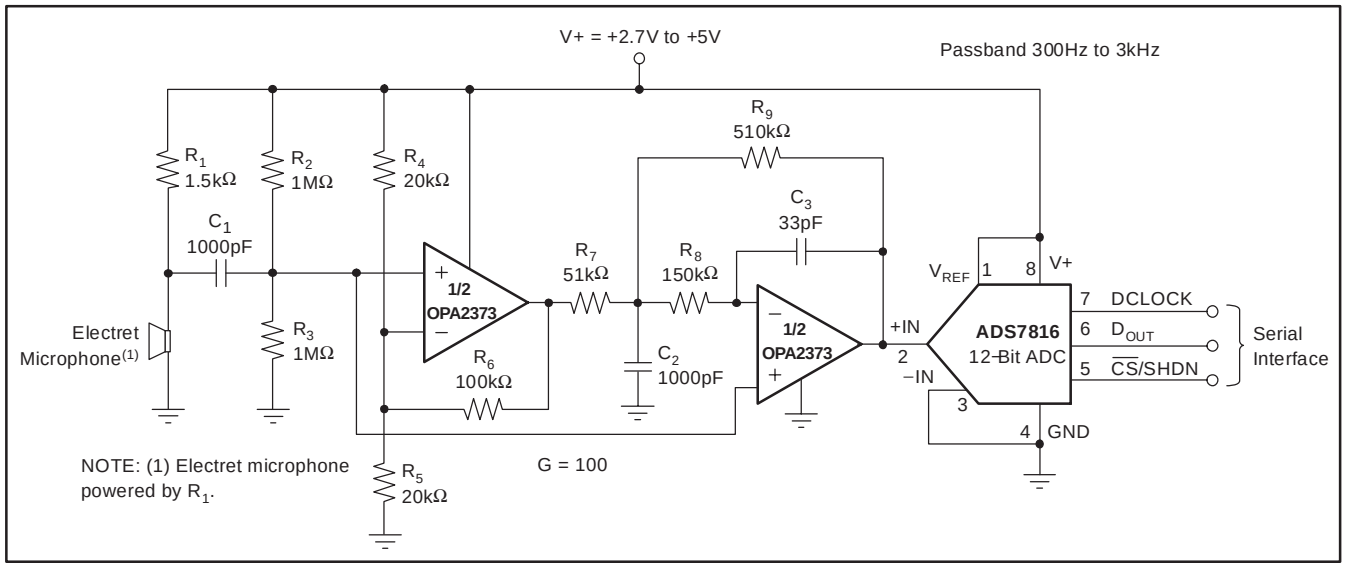


Figure 8. The OPA2373 as a Speech Bypass Filtered Data Acquisition System

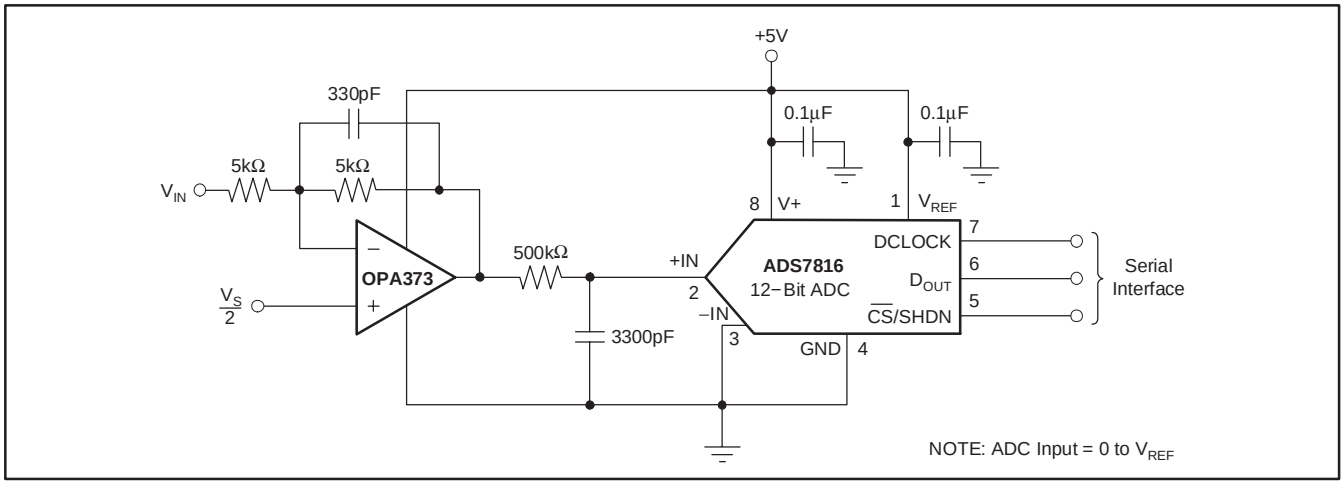
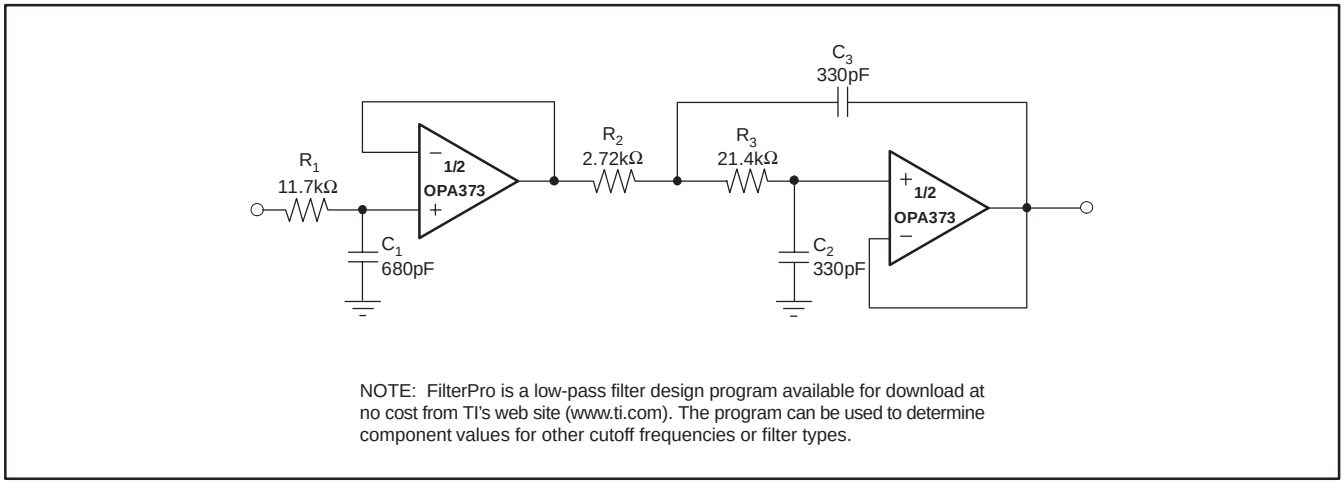


Figure 9. The OPA373 in Inverting Configuration Driving the ADS7816



NOTE: FilterPro is a low-pass filter design program available for download at no cost from TI's web site (www.ti.com). The program can be used to determine component values for other cutoff frequencies or filter types.

Figure 10. Three-Pole Sallen-Key Butterworth Low-Pass Filter

DFN PACKAGE

The OPA2373 is available in a DFN-10 package (also known as SON), which is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad. DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard PCP assembly techniques. See Application Note, QFN/SON PCB *Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V−.

LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements.

Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB. Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests.

Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2373AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	AYO	Samples
OPA2373AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	AYO	Samples
OPA2373AIDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2373AIDRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2373AIDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2374AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A	Samples
OPA2374AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A	Samples
OPA2374AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2374A	Samples
OPA2374AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2374A	Samples
OPA373AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA373AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA374AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA4374AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples
OPA4374AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4374AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples
OPA4374AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

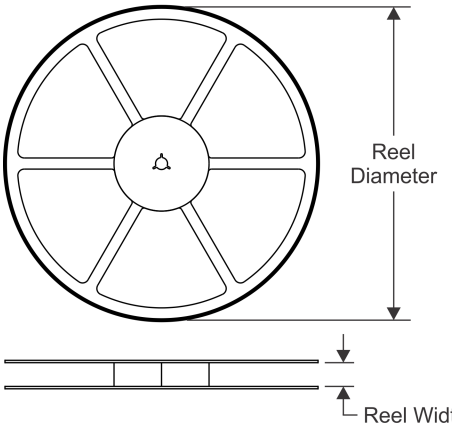
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

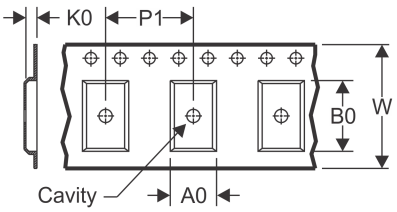
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

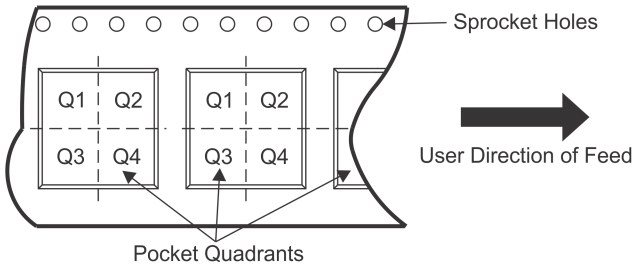


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

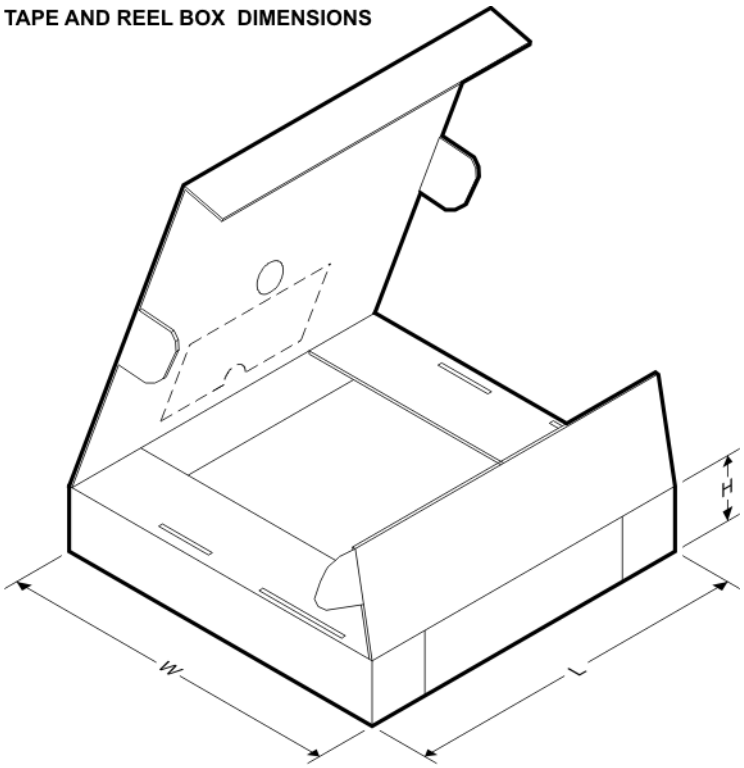
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2373AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2373AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2373AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2373AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2374AIDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA2374AIDCNT	SOT-23	DCN	8	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA2374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA373AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA374AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4374AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4374AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4374AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

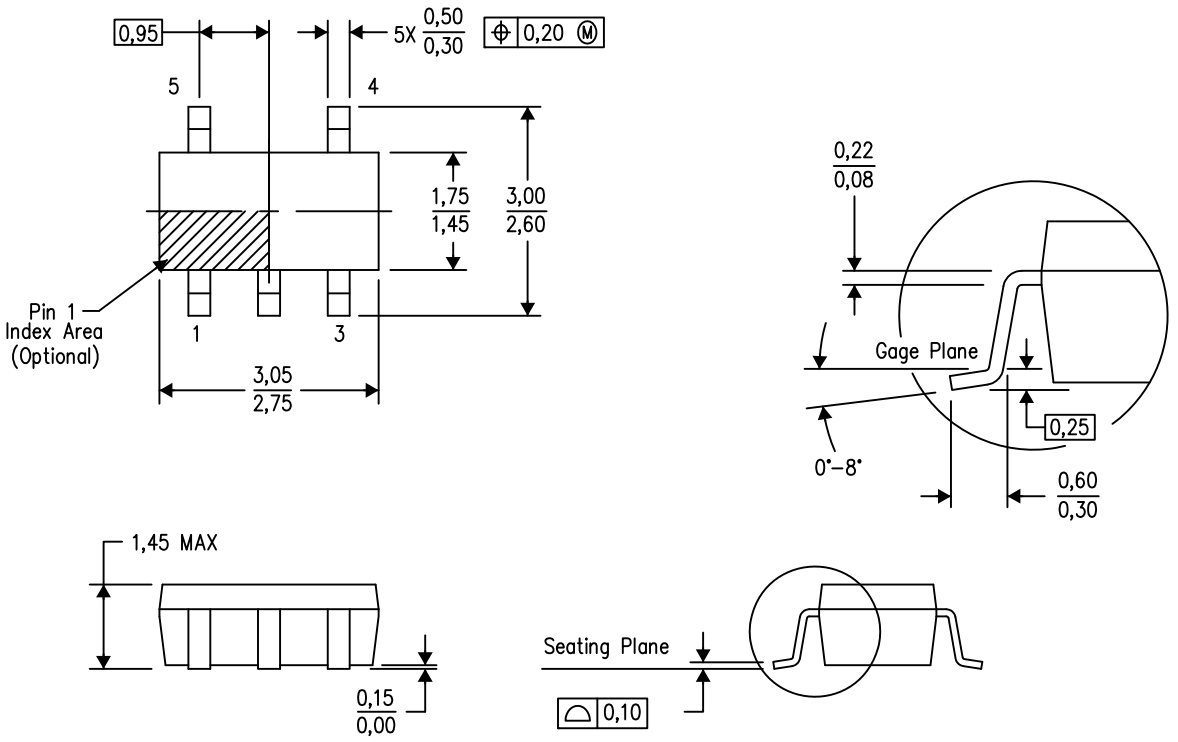
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2373AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2373AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2373AIDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
OPA2373AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0
OPA2374AIDCNR	SOT-23	DCN	8	3000	210.0	185.0	35.0
OPA2374AIDCNT	SOT-23	DCN	8	250	210.0	185.0	35.0
OPA2374AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA373AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA374AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA374AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA374AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4374AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4374AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4374AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

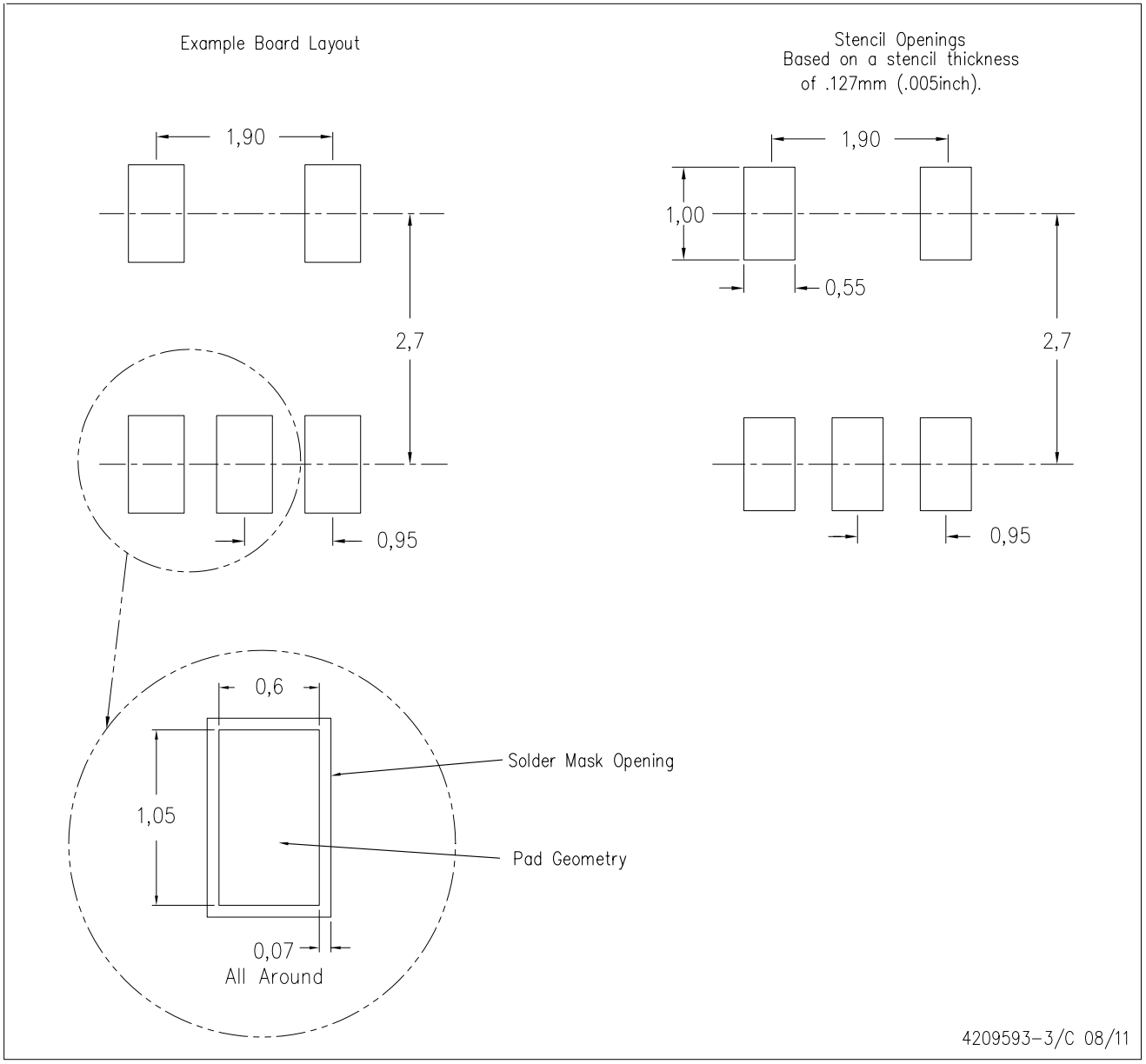
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

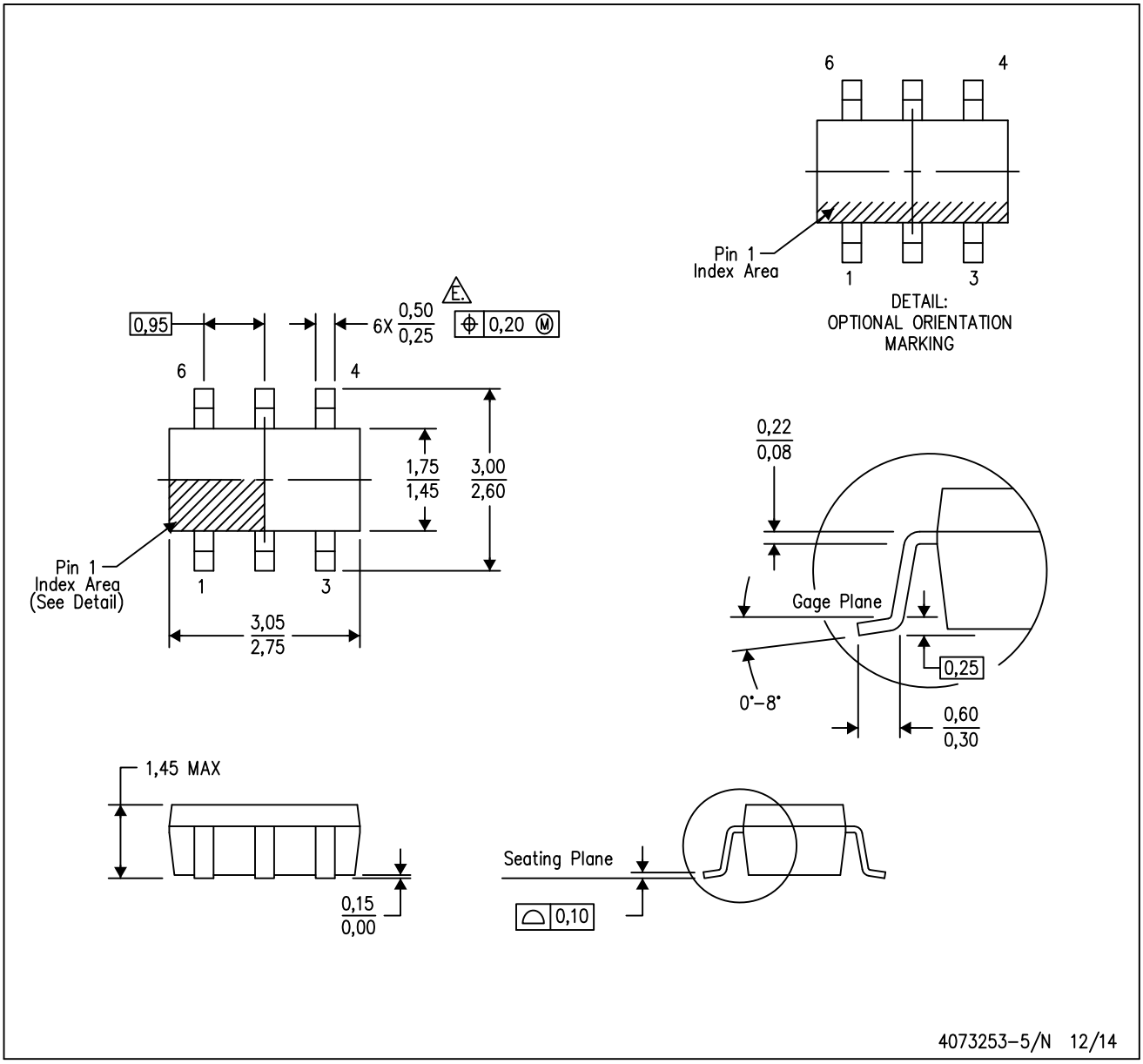
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



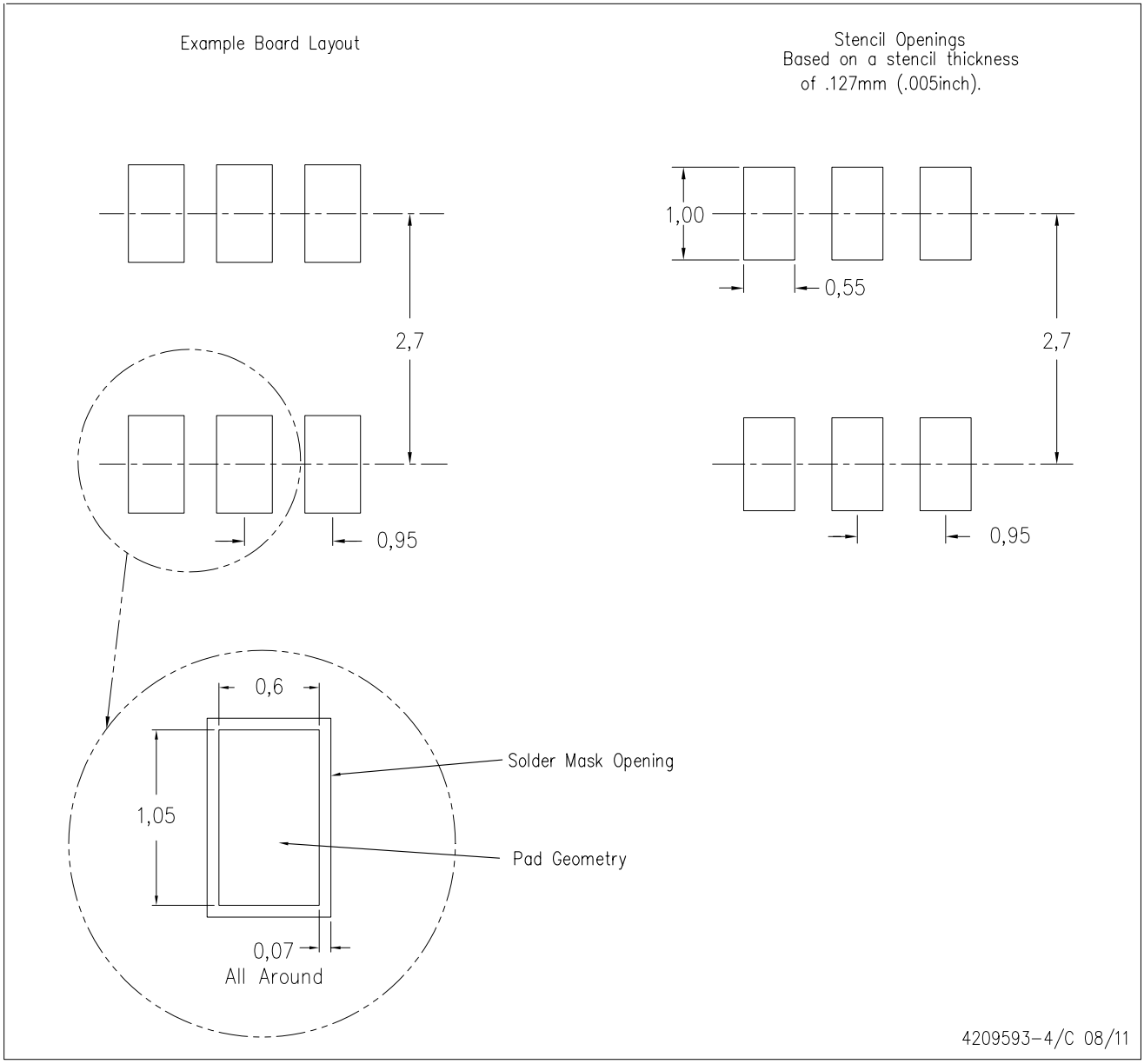
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



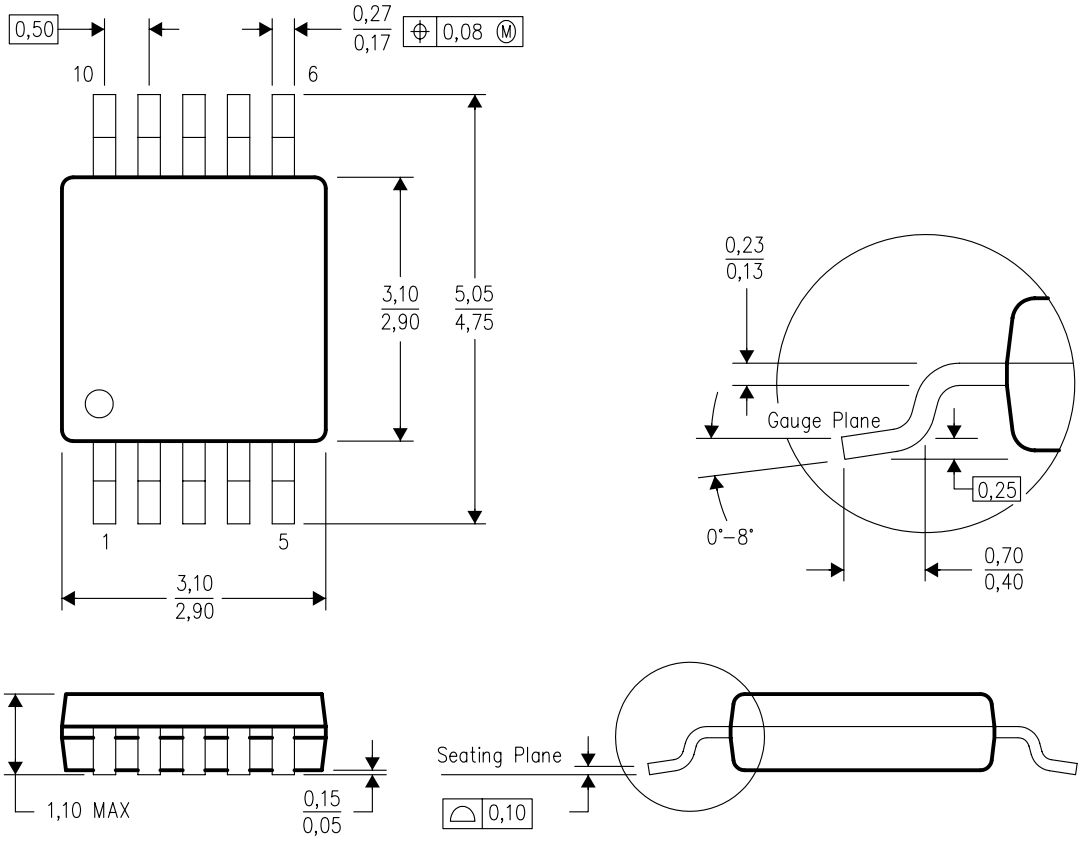
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

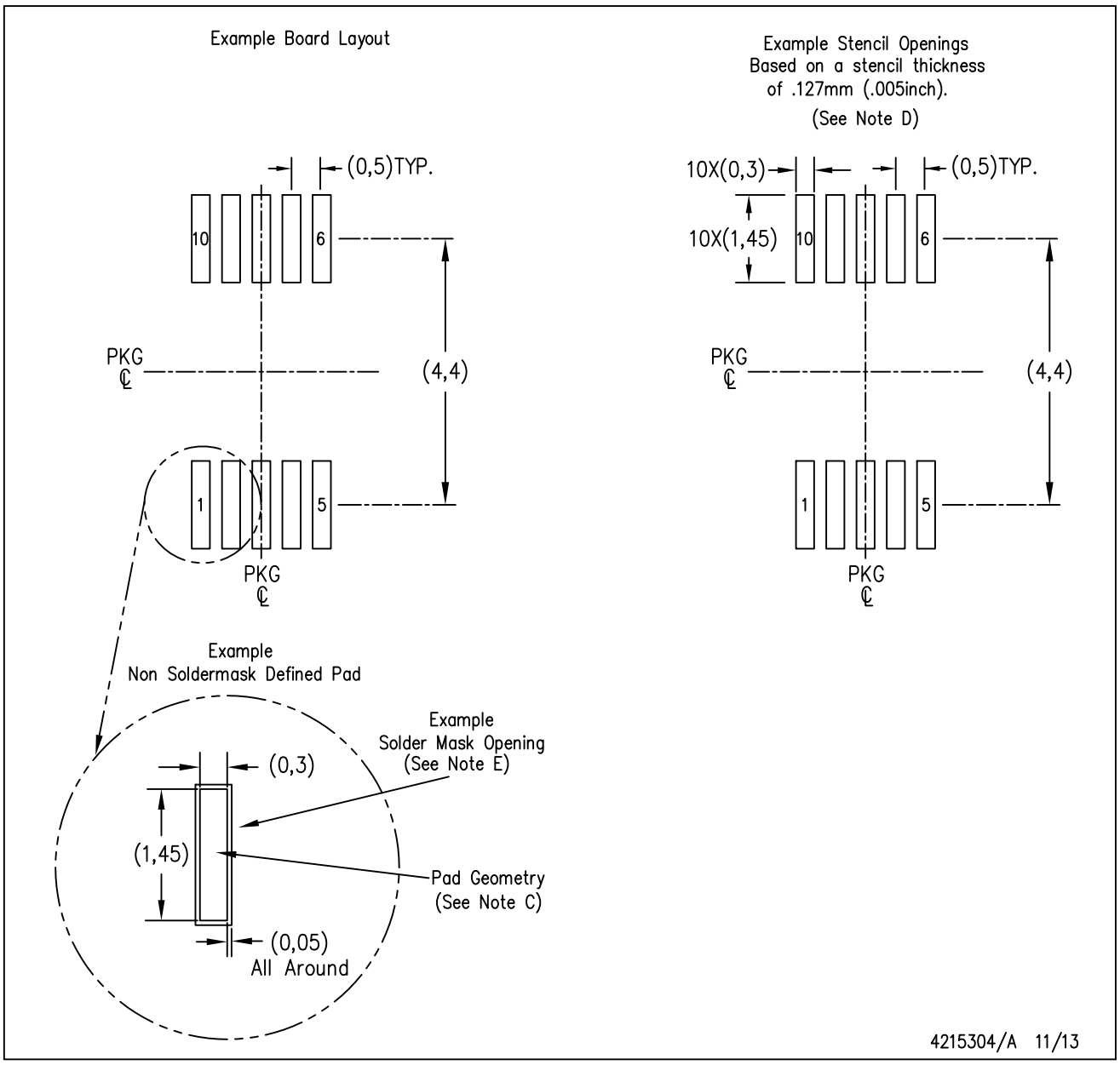
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

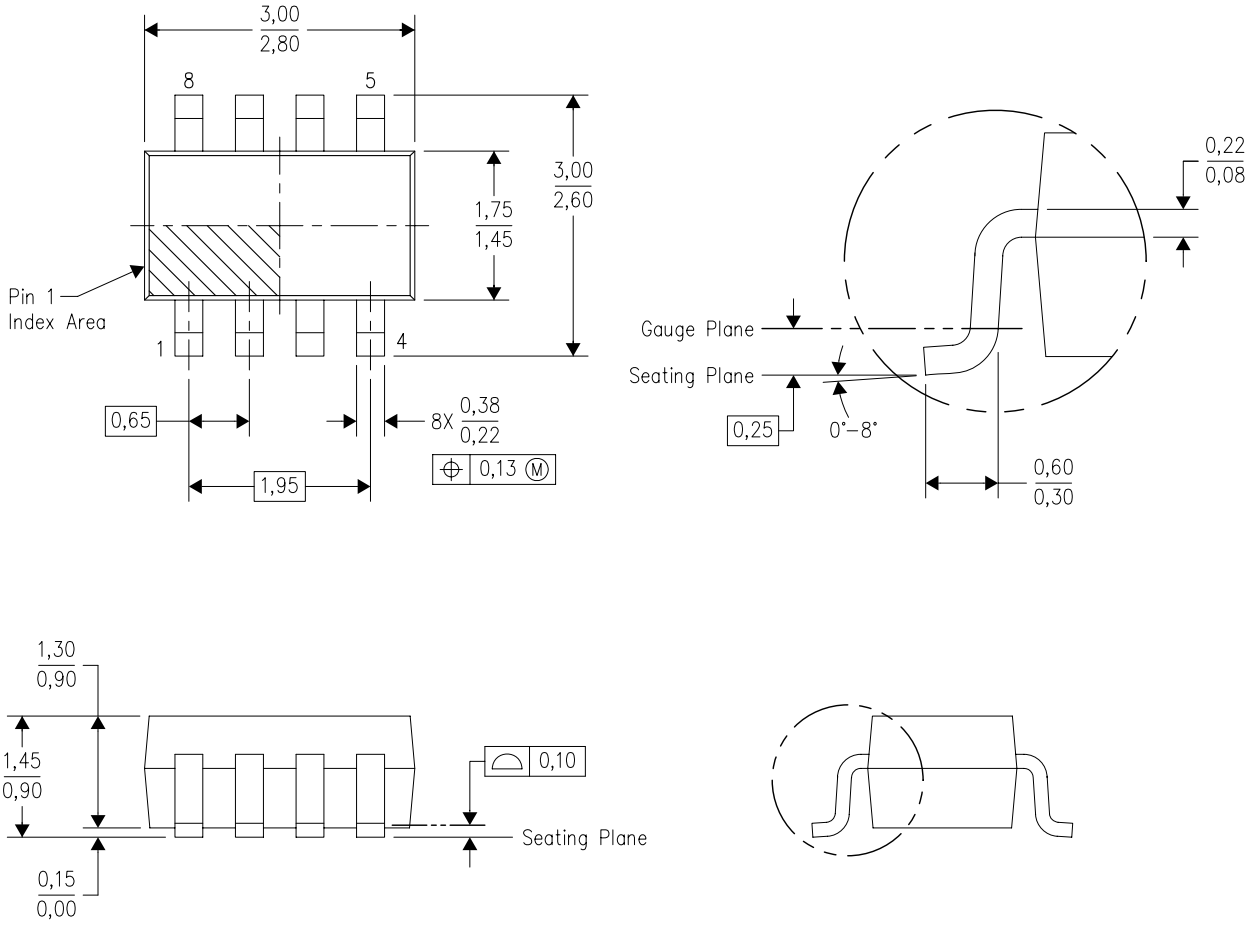
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



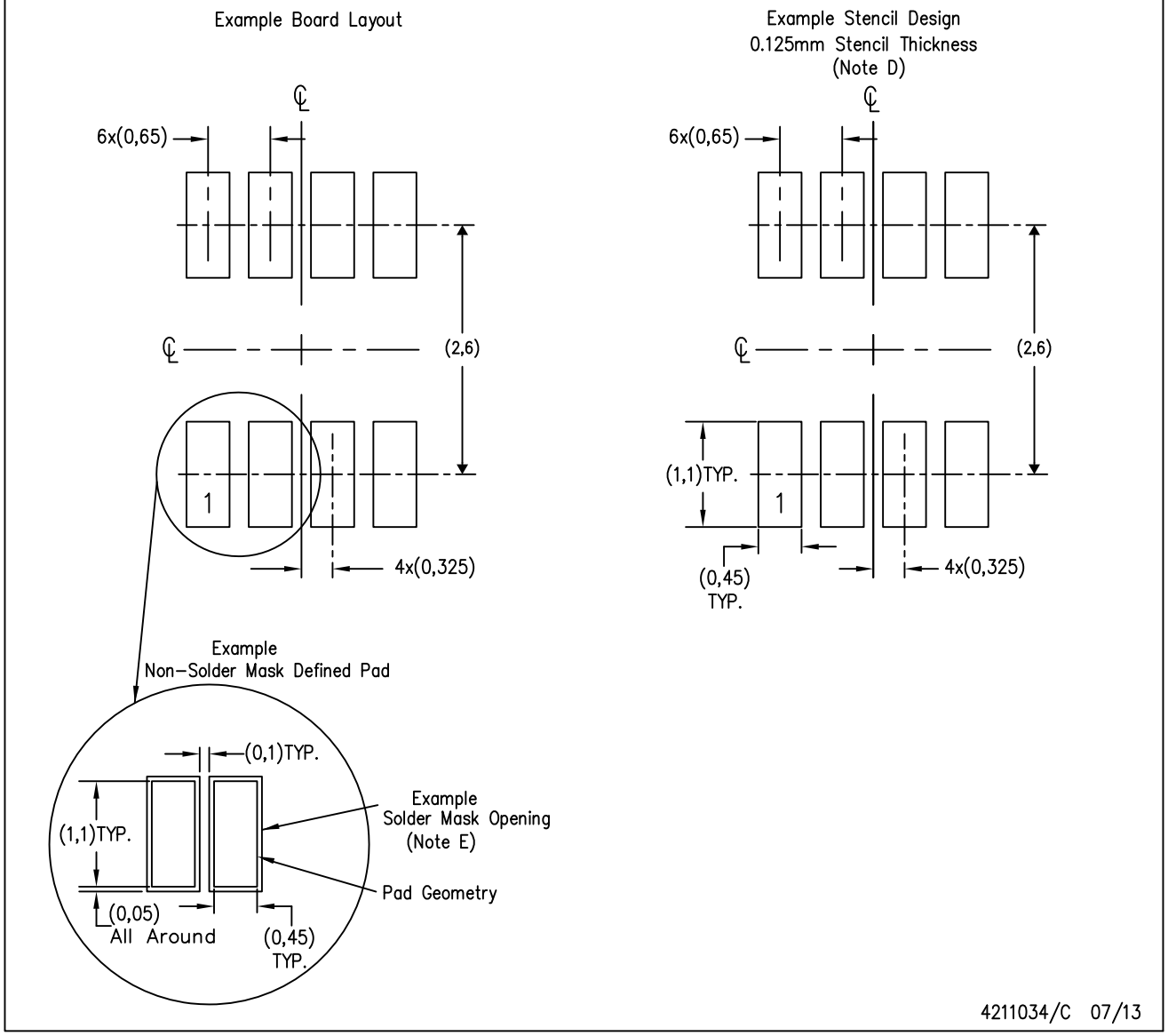
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



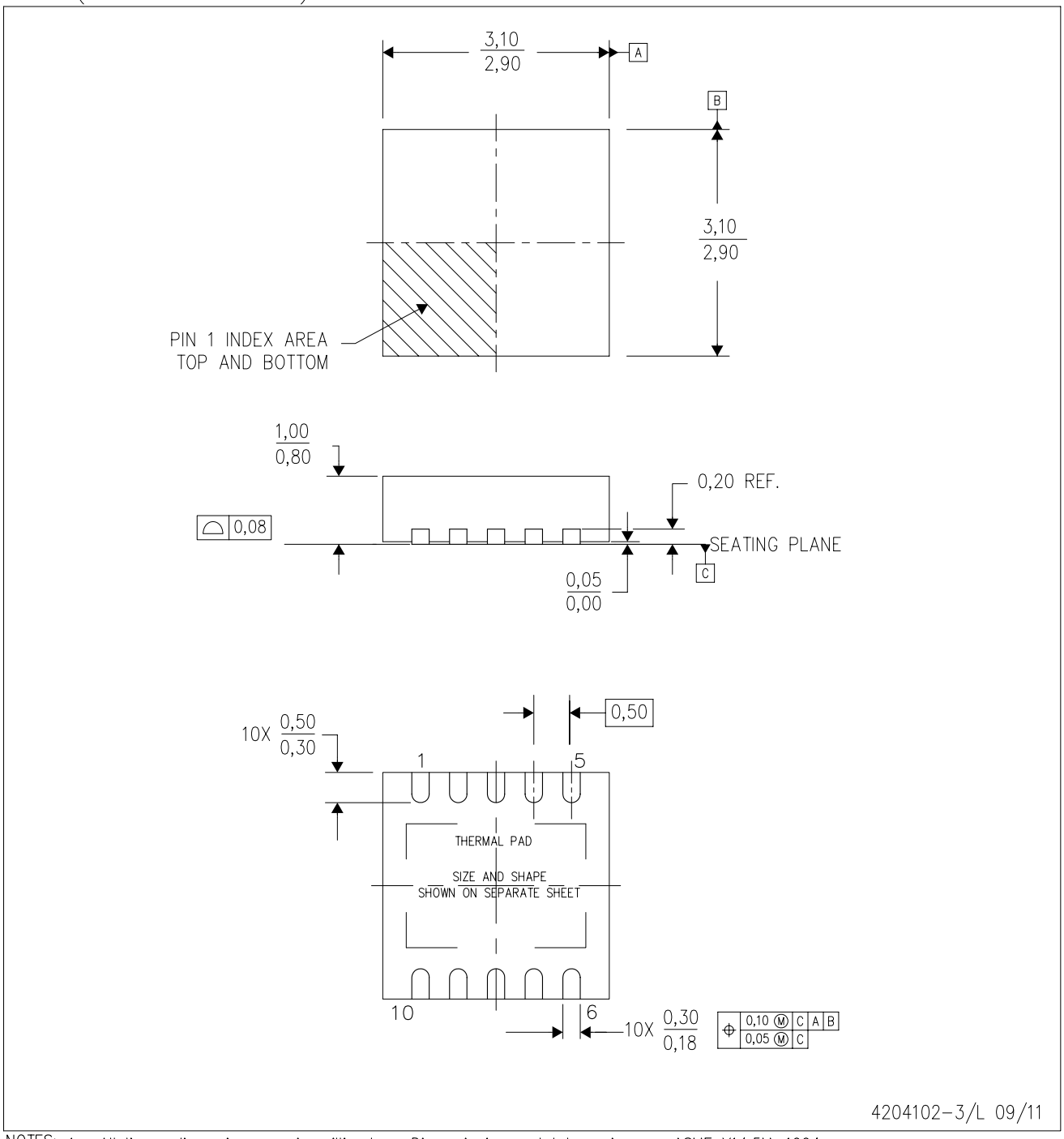
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

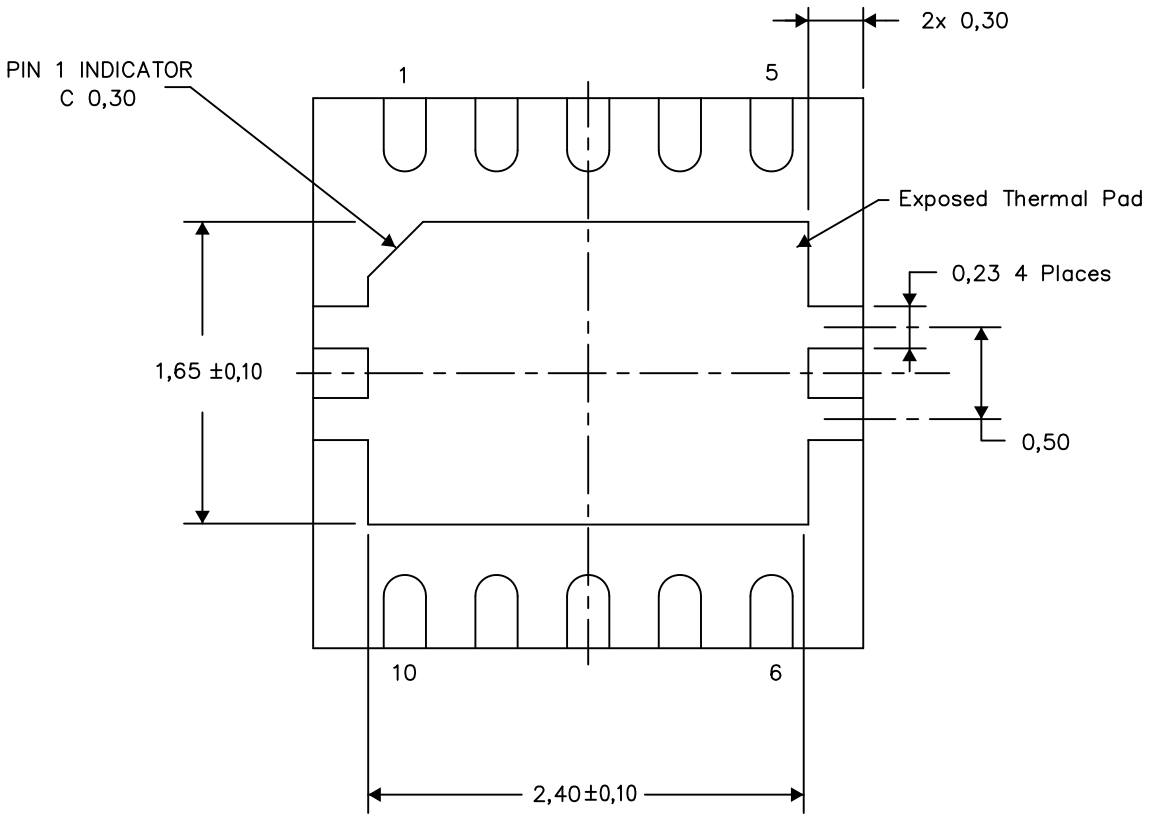
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



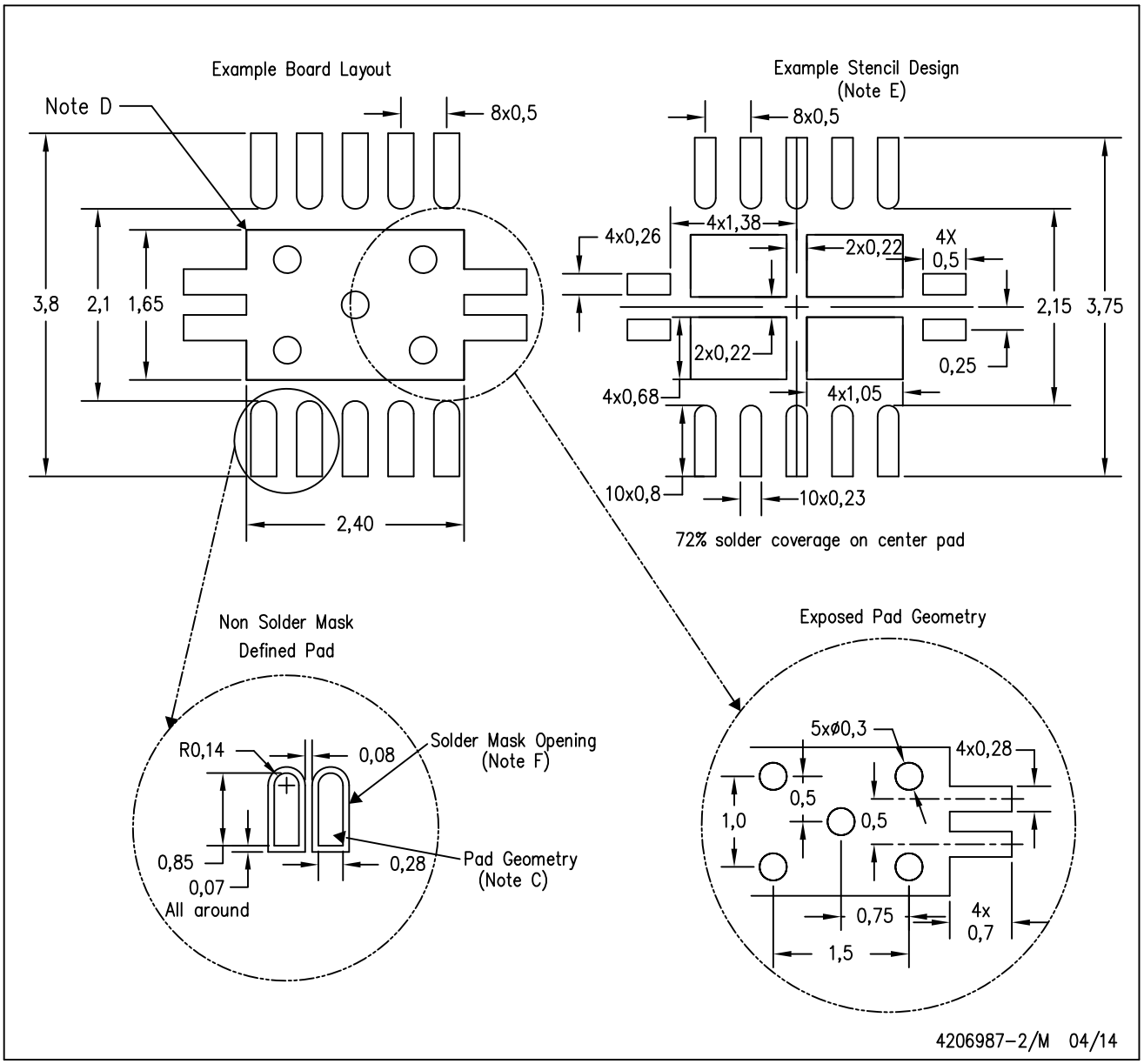
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/U 04/14

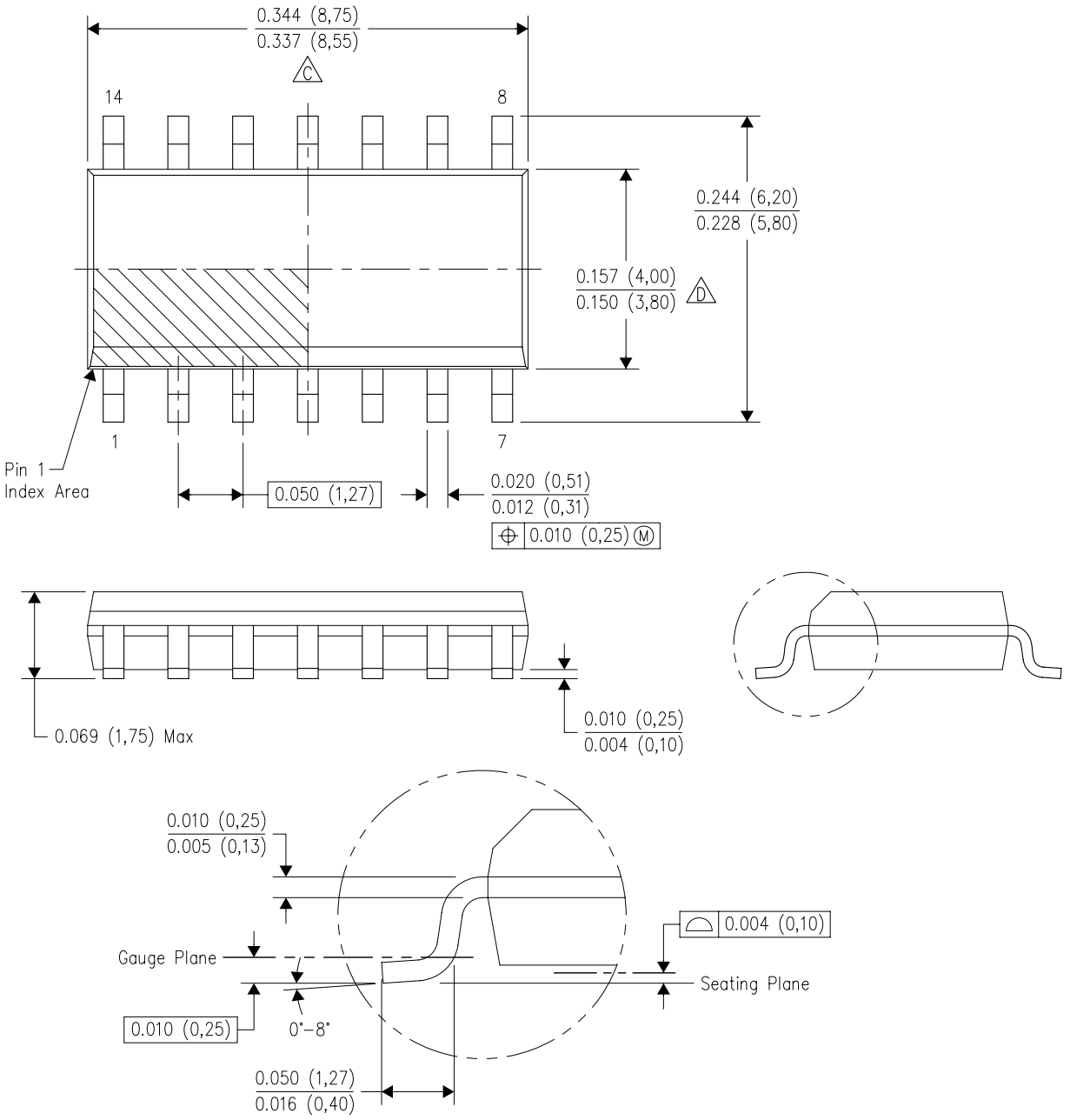
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

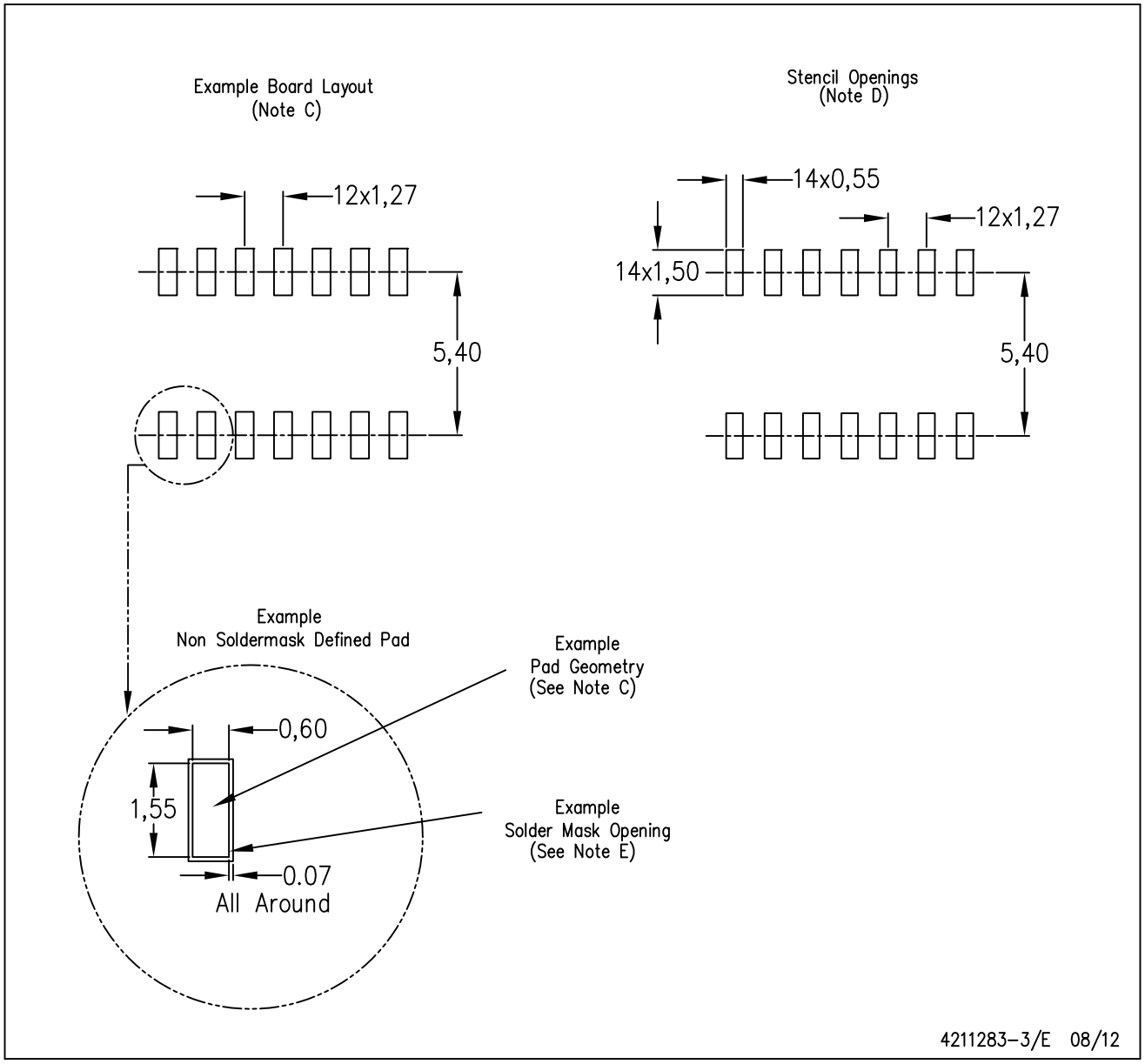
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

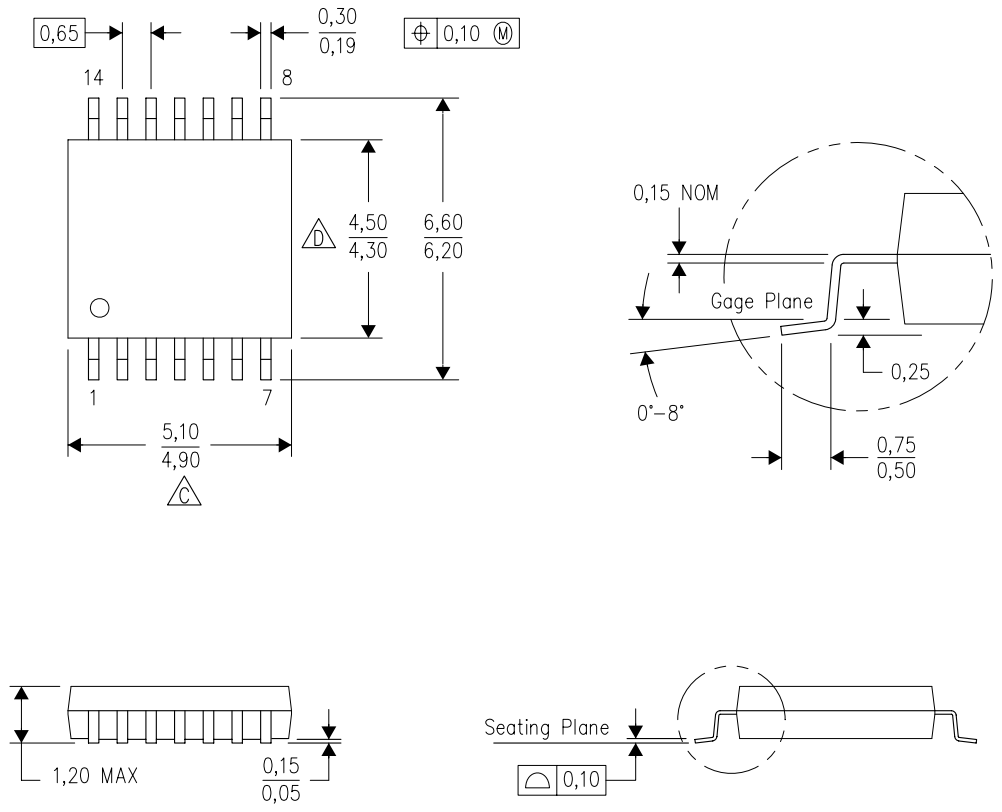
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

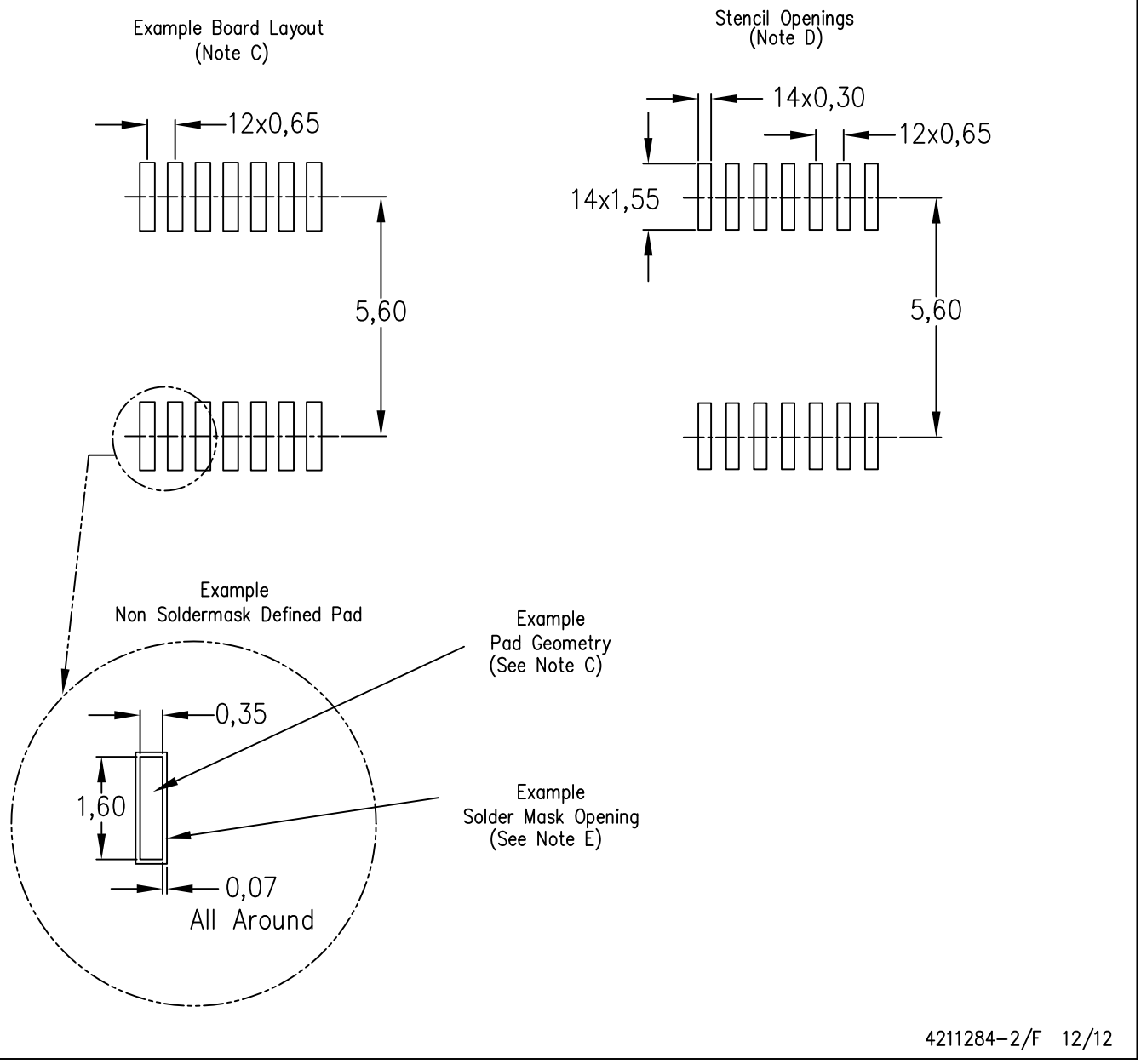
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

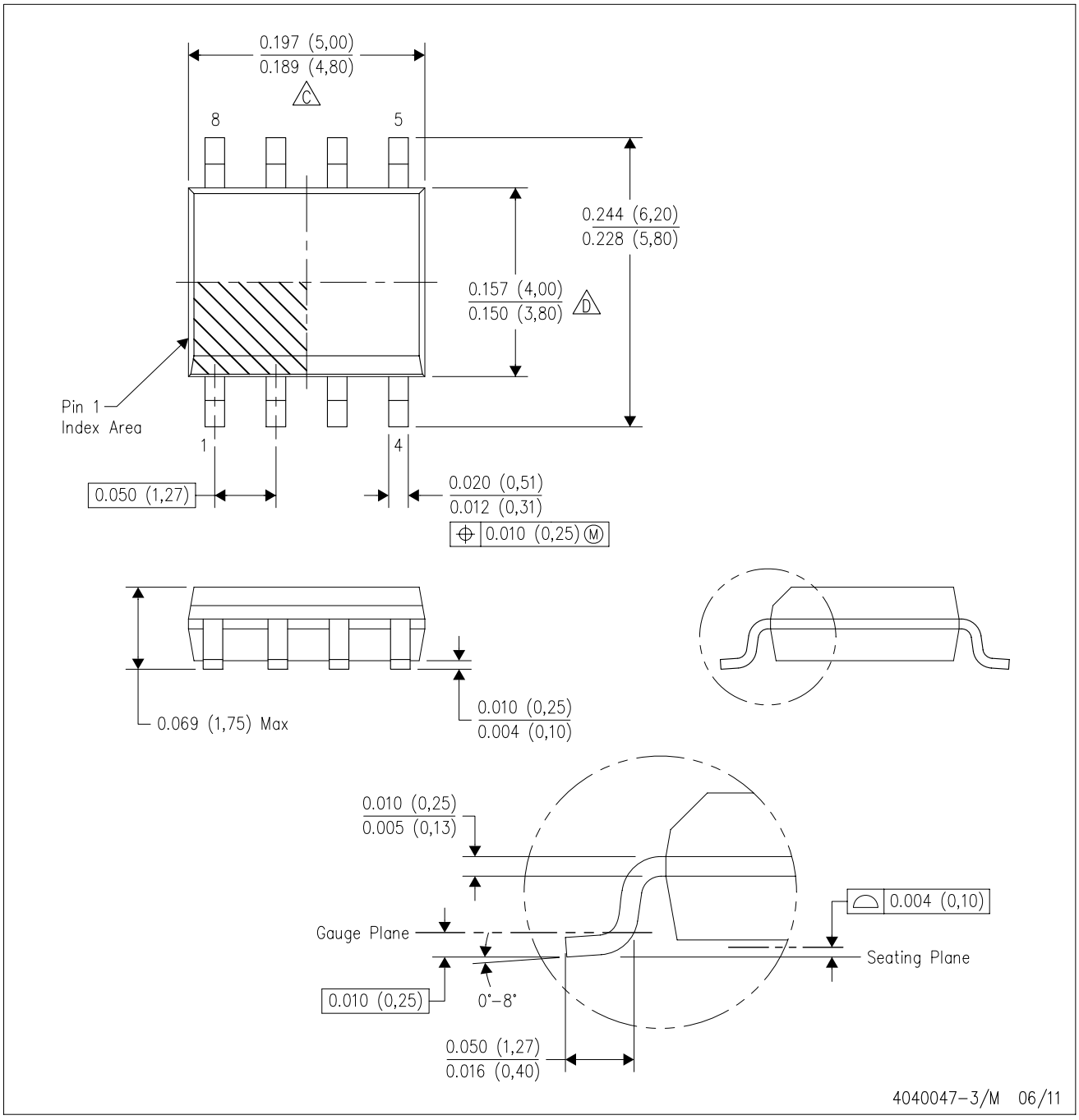
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



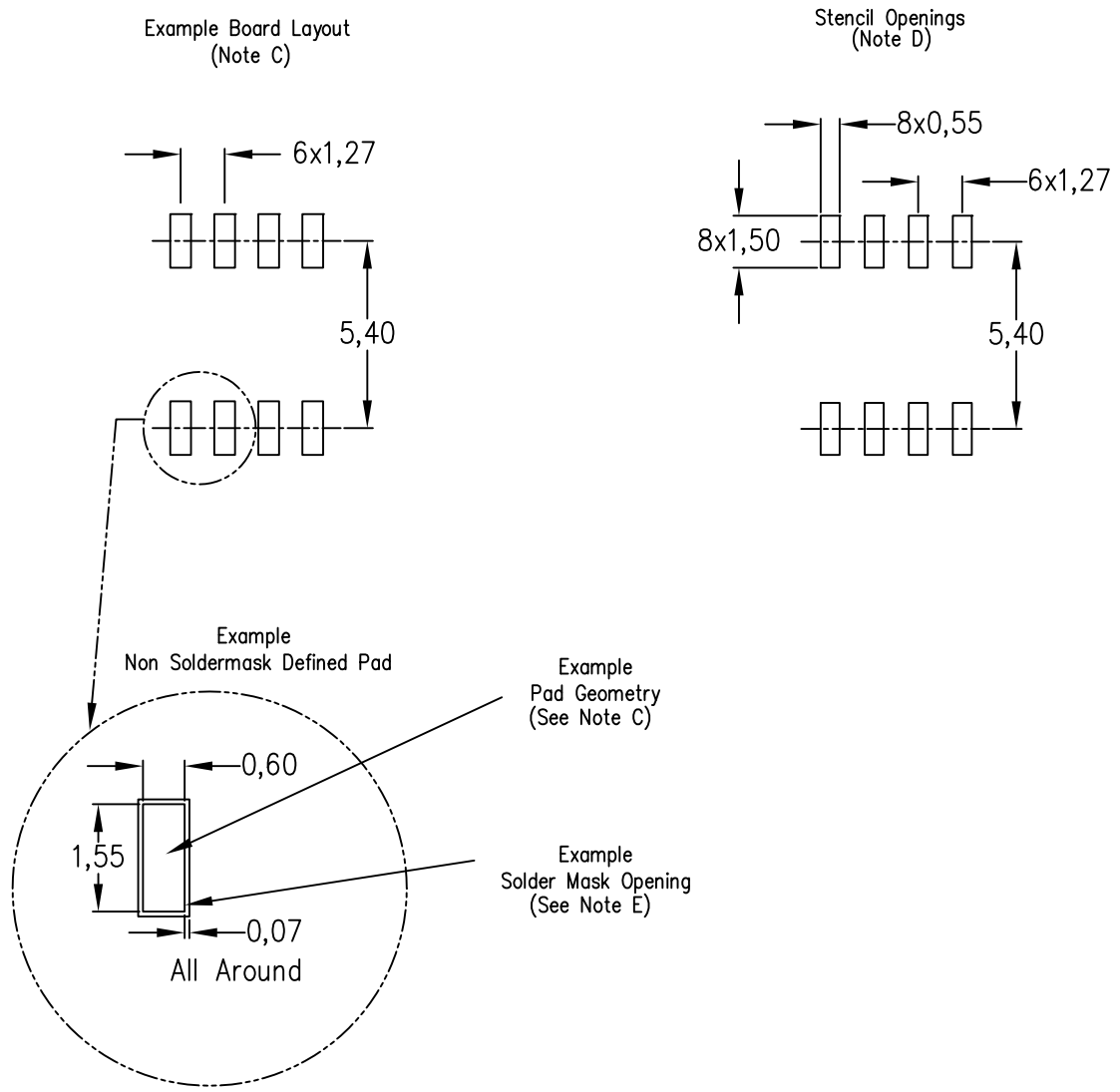
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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