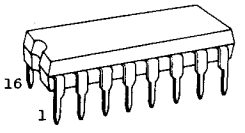
TC5051P, TC5052P

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5051P 4 DIGIT DECADE COUNTER WITH BLANKING CONTROL
TC5052P 4 DIGIT DECADE COUNTER WITH CLOCK ENABLE

TC5051P and TC5052P are four digit decimal up counters. The contents of counter are dynamically output digit by digit in sequence from the higher-order digit to BCD OUTPUT. When the content of counter reaches "9999", CARRY OUT is output with "H" level, and it holds "L" level for other counter contents.
TC5051P has BLANKING CONTROL input which facilitates the leading zero suppress operation for higher order digits than arbitrary digit position. And TC5052P is capable to inhibit CLOCK by means of CLOCK ENABLE input.

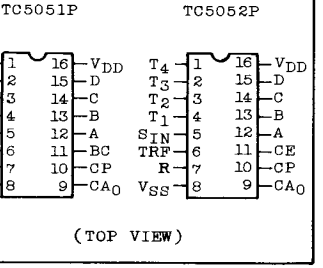


DIP 16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

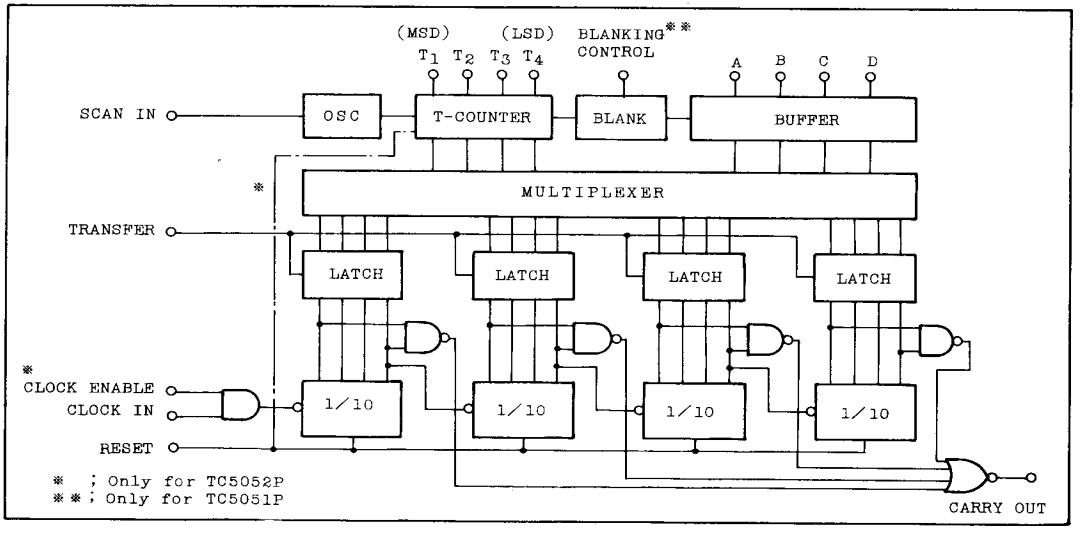
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+14	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



* ; Only for TC5052P
** ; Only for TC5051P

DESCRIPTION OF PIN FUNCTION

PIN No.	SYMBOL	NAME	FUNCTION
1	T_4	DIGIT SELECT 4	Outputs to select the digit of BCD OUT (Output signal) and correspond in ascending order from T_1. "H" level is shifted from T_1, T_2, T_3 then T_4 in sequence for every eight clocks of S_{IN}. In the case of TC5052P, when RESET is set to "H", all of T_1~T_4 become "L" and when RESET falls the scan is always started from T_1. T_1~T_4 are not affected by RESET for TC5051P.
2	T_3	DIGIT SELECT 3	
3	T_2	DIGIT SELECT 2	
4	T_1	DIGIT SELECT 1	
5	S_{IN}	SCAN INPUT	T-COUNTER CLOCK input. The clock can be generated by connecting a capacitor between this terminal and GND.
6	TRF	TRANSFER	H: Decimal counter outputs are transferred to the multiplexer as they are. L: The counter outputs at the falling edge of TRF are latched.
7	R	RESET	The counter is reset to "0000" by "H" level input. TC5052P establishes the synchronism of T-counter by means of CLEAR input.
8	V_{SS}	V_{SS}	(GND)
9	CA_O	CARRY OUT	"H" level is output as long as the counter holds "9999". This becomes "L" level for all other counts.
10	CP	CLOCK INPUT	First stage decimal counter clock, which triggers at the falling edge.
11	CE	CLOCK ENABLE (TC5052P)	Clock input is inhibited by "L" level
	BC	BLANK CONTROL (TC5051P)	All digits are displayed by "H" level, leading zero suppress can be achieved by "L" level and zero suppress for higher order digits than a specific digit position can be achieved by connecting T output to BC.
12	A	BCD OUT A	BCD outputs of decimal counter. When T_1="H", the highest order digit (4th digit) is output. When T_2="H", 3rd digit is output, when T_3="H", 2nd digit is output and when T_4="H", 1st digit is output. If zero suppress is activated, all the outputs become "H" level.
13	B	BCD OUT B	
14	C	BCD OUT C	
15	D	BCD OUT D	
16	V_{DD}	V_{DD}	V_{DD} Power Supply (3 - 12 volts)

OPERATING CONSIDERATION

* Count and Reset Operations

When RESET input is set at "H" level, the counter is reset to "0000". If pulse is applied to CLOCK input after returning RESET input to "L", the counter advances its count up to "9999" at the falling edge of clock providing CLOCK ENABLE to be "H". If CLOCK ENABLE is "L", CLOCK is inhibited. CARRY OUT is output with "H" level only when the count is "9999".

* Latch Operation - When TRANSFER input is set to "H", the counter output is transferred to the multiplexer as it is and output dynamically to BCD OUT in synchronism with S_{IN}. When TRANSFER input is changed from "H" to "L", the counter content at the falling edge of TRANSFER is stored in the latch and BCD OUT is not varied even if the count changes.

*Scan Operation - BCD output of each digit is output on common A_{OUT}~D_{OUT} on time sharing basis and switching of digit is achieved by connecting a capacitor between SCAN IN input and V_{SS}(GND)(internal oscillation) or by supplying external clock from SCAN IN.

OPERATING CONSIDERATION

Capacitance of approximately 1000pF is recommended for the internal oscillation.

Switching of digit is in synchronism with the timing outputs of T_1 - T_4. When T_1 is "H" thousand's digit is output to BCD OUT, when T_2 is "H" hundred's digit is output, when T_3 is "H" ten's digit is output, and when T_4 is "H" unit's digit is output.

* Blanking Operation (TC5051P)

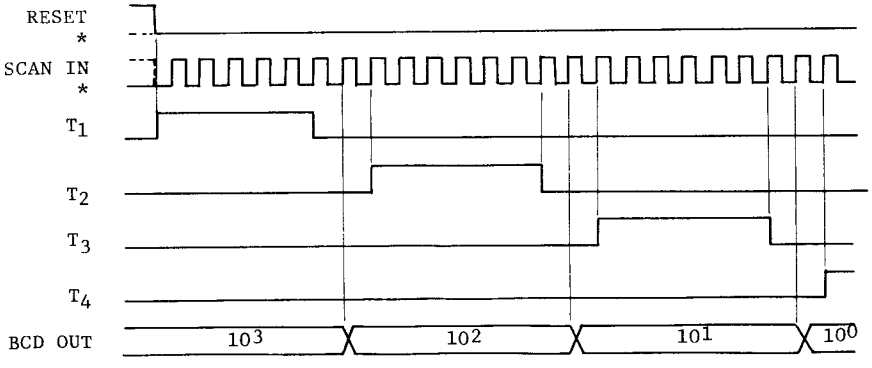
By controlling BLANKING CONTROL, leading zero suppress of higher order digit positions than a specific digit position can be achieved by the function of internal circuit.

BLANKING CONTROL	= V_{SS}	Zero Suppress for all digits *
"	= V_{DD}	No Zero Suppress
"	= T_2	Zero Suppress for only thousand's digit *
"	= T_3	Zero Suppress for thousnad's and hundred's digits *
"	= T_4	Zero Suppress for all except unit's digit *

When blanking is activated, all of A_{OUT} - D_{OUT} become "H".

* (Note) When a carry occurs from the counter and during one cycle of T counter, normal output may not be seen.

TIMING CHART



* ..... TC5051P, — TC5052P

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	12	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
S_{IN} Connecting Capa.	C_{EXT}		50	-	30000	pF
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

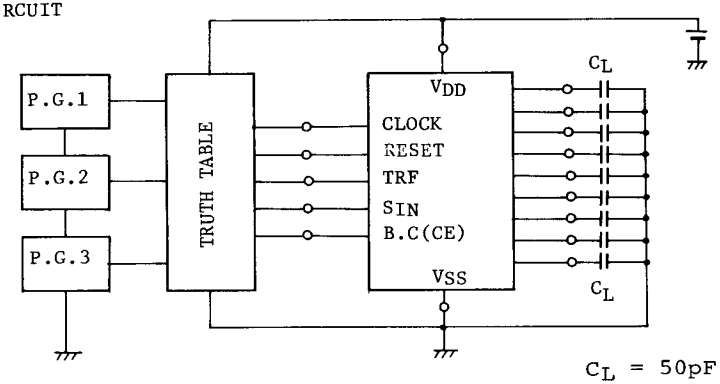
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5 10	4.95 9.95	-	4.95 9.95	5.00 10.00	-	4.95 9.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5 10	-	0.05 0.05	-	0.00 0.00	0.05 0.05	-	0.05 0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V V_{OH}=9.5V $V_{IN}=V_{SS},V_{DD}$	5 10	-0.2 -0.5	- -	-0.16 -0.4		- -	-0.12 -0.3	- -	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V V_{OL}=0.5V $V_{IN}=V_{SS},V_{DD}$	5 10	0.52 1.3	-	0.44 1.11		- -	0.36 0.9	-	mA
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V $\|I_{OUT}\|<1\mu A$	5 10	3.5 7.0	-	3.5 7.0	2.75 5.5	- -	3.5 7.0	-	V
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V $\|I_{OUT}\|<1\mu A$	5 10	-	1.5 3.0	-	2.25 4.5	1.5 3.0	-	1.5 3.0	V
High Level Input Current (other than S_{IN})	I_{IH}	V_{IH}=12V	12	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Low Level Input Current (other than S_{IN})	I_{IL}	V_{IL}=0V	12	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
High Level Input Current (S_{IN})	I_{IH}	V_{IH}=12V	12	-	-	50	-	200	-	-	μA
Low Level Input Current (S_{IN})	I_{IL}	V_{IL}=0V	12	-	-	1.5	-	6	-	-	mA
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS},V_{DD}$	5 10	- -	- -	200 500	- -	200 500	- -	500 1000	μA

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
Output Fall Time	t_{THL}		5	-	100	200	ns
			10	-	50	100	
Propagation Delay Time (CLOCK-BCD_{OUT})	t_{pLH} t_{pHL}	T_4="H"	5	-	1200	2500	ns
			10	-	450	1000	
Propagation Delay Time (CLOCK-CARRY)	t_{pLH} t_{pHL}		5	-	900	2000	ns
			10	-	400	800	
Propagation Delay Time (S_{IN} - T_n)	t_{pLH} t_{pHL}		5	-	1200	2500	ns
			10	-	450	1000	
Propagation Delay Time (S_{IN} -BCD_{OUT})	t_{pLH} t_{pHL}		5	-	1600	2500	ns
			10	-	700	1400	
Propagation Delay Time (CLEAR-BCD_{OUT})	t_{pHL}		5	-	900	2000	ns
			10	-	350	800	
Min. RESET Pulse Width	t_w (RESET)		5	-	700	1500	ns
			10	-	350	750	
Min. Transfer Pulse Width	t_w (TRANSFER)		5	-	140	500	ns
			10	-	50	250	
Max. Clock Frequency	f_{CL}		5	1.0	1.5	-	MHz
			10	2.0	3.5	-	
Max. Scan Frequency	f_{CL} (SCAN)		5	0.5	1.0	-	
			10	1.0	2.0	-	
Min. Removal Time (RESET - COLOCK)	t_{rem}		5				ns
			10				
Min. Set Up Time (TRANSFER-CLOCK)	t_{SU}		5				ns
			10				
Min. Set Up Time (TRANSFER-CLEAR)	t_{SU}		5				
			10				
Max. Clock Rise Time	t_{rCL}		5	20	-	-	μs
Max. Clock Fall Time	t_{fCL}		10	2.5	-	-	
Input Capacitance	C_{IN}						pF

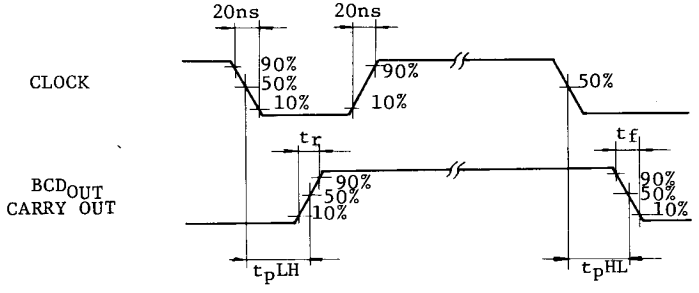
SWITCHING TIME TEST CIRUIT

TEST CIRCUIT



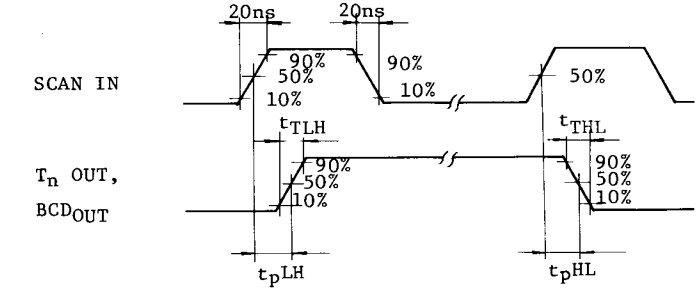
SWITCHING TIME TEST WAVEFORMS

WAVEFORM 1.



RESET="L"
CE(TC5052P)="H"
B.C.(TC5051P)="H"
TRF="H"
SIN : Any Pulses

WAVEFORM 2.



RESET="L"
CE,(B.C.)="H"
TRF="H"
CLOCK : Any Pulses

SWITCHING TIME TEST WAVEFORMS

WAVEFORM 3.