GD4024B
7-STAGE BINARY COUNTER

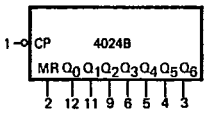
DESCRIPTION – The 4024B is a 7-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and seven fully Buffered Parallel Outputs (Q_0–Q_6). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0–Q_6) LOW, independent of the Clock Input ($\overline{CP}$).

- **TYPICAL COUNT FREQUENCY OF 30 MHz AT V_{DD} = 10 V**
- **CLOCK TRIGGERED ON THE HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

PIN NAMES

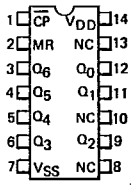
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input
Q_0–Q_6	Buffered Parallel Outputs

LOGIC SYMBOL



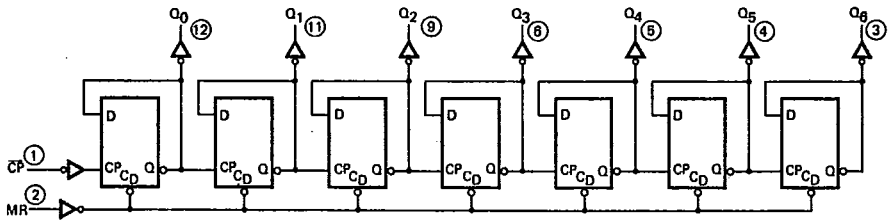
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13
○ = Pin Number

GS CMOS · GD4024B

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		100	200		45	90		30	72	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			97	195		40	80		25	64	ns	
t_{PHL}	Propagation Delay, MR to Q_n		130	260		50	100		35	80	ns	
t_{TLH}	Output Transition Time		60	130		30	70		25	45	ns	
t_{THL}			60	130		30	70		25	45	ns	
$t_W\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	90	45		35	17		28	13		ns	
t_WMR	MR Minimum Pulse Width	80	40		30	15		24	12		ns	
t_{rec}	MR Recovery Time	60	30		25	12		20	9		ns	
f_{MAX}	Input Count Frequency (Note 3)	6	12		15	30		18	36		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

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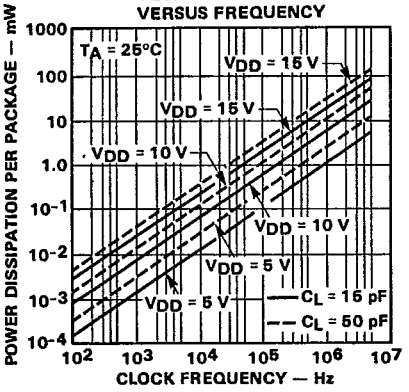
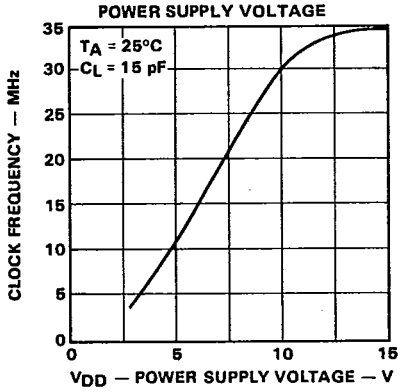
TYPICAL ELECTRICAL CHARACTERISTICS

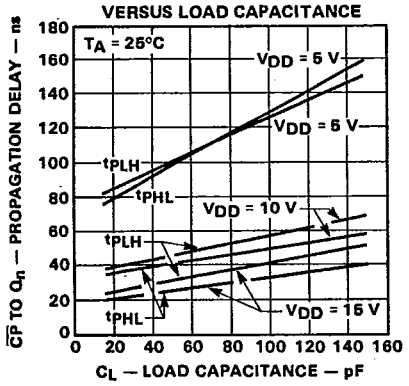
POWER DISSIPATION VERSUS FREQUENCY



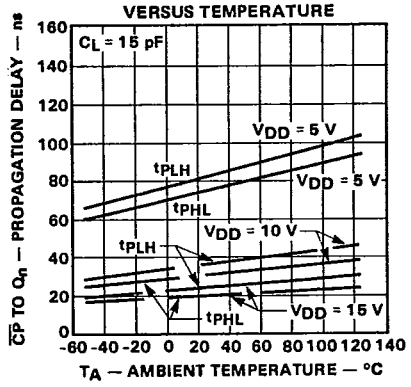
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



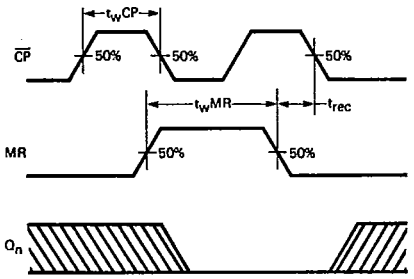
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



SWITCHING WAVEFORMS



MINIMUM PULSE WIDTH FOR $\overline{CP}$ AND MR AND MR RECOVERY TIME